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Issues in Building Large RSFQ Circuits

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Recently, there has been a great advancement in Rapid Single Flux Quantum (RSFQ) logic circuit development on the single chip level. These circuits include analog-to-digital (A/D) converters, digital-to-analog (D/A) converters, time-to-digital converters, network switches, etc. The performance of these circuits is superior to circuits implemented with other technologies because of the ultra-low power dissipation and high-speed operation of Josephson junctions. However, Practical implementation of the SFQ technology in most applications will require more than single-chip-level circuit complexity. Multiple chips have to be integrated with a technology that is reliable at cryogenic temperatures and supports an inter-chip data transmission speed of tens of GHz. In this work we have studied three basic issues in building large RSFQ circuits. The first is the reliable inter-chip SFQ pulse transfer technique using MCM technology. By noting that the energy contained in an SFQ pulse is less than an attojoule, it is not very surprising that the direct transmission of a single SFQ pulse through MCM solder bump connectors can be difficult and an innovative technique is needed. The second is the recycling of the bias currents. Since RSFQ circuits are dc current biased the large RSFQ circuits need a serial biasing. The third is the clock distribution among the chips. Synchronization of the clock signals in various chips is critical.

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