대한기계학회 2001년도 춘계학술대회논문집 C pp. 22~35 강연07

Simulation Based Design Optimization

June 28, 2001

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Executive Vice President
Samsung Advanced Institute of Technology

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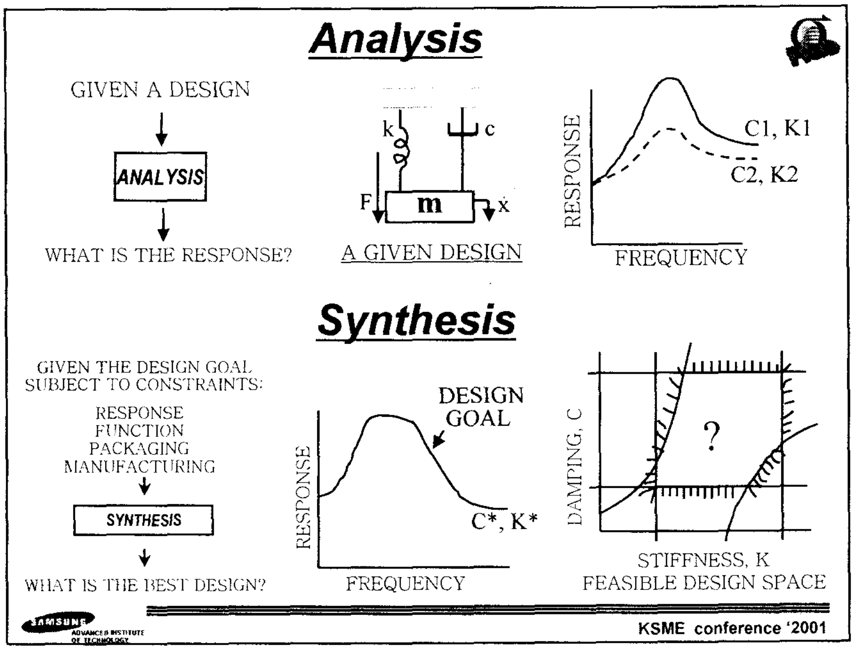
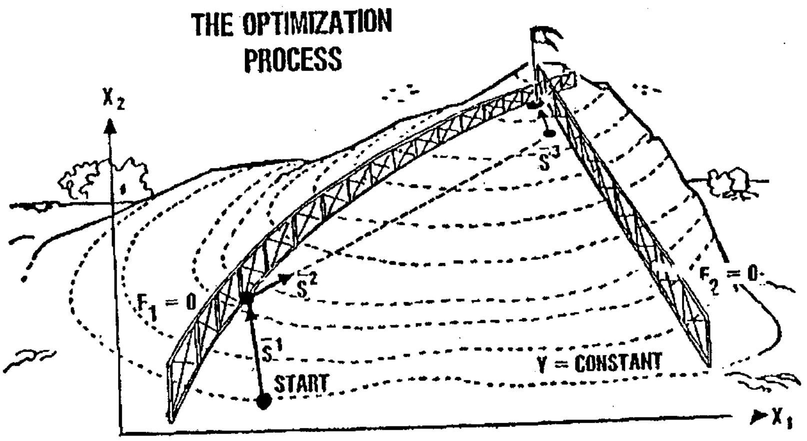
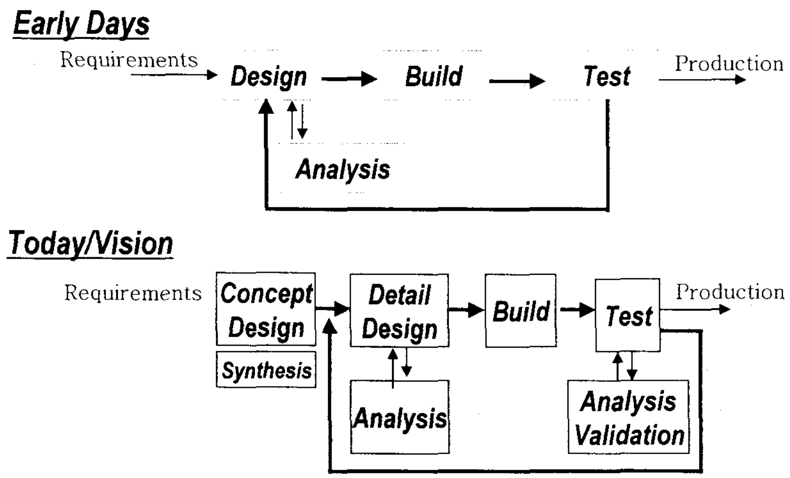




$$\bar{X}^{q+1} = \bar{X}^{q} + \alpha \bar{S}^{q}$$

G.N. Vanderplaats

CAE Evolution



Synthesis/Integration	***Analysis***
Upstream	**Downstream**
Simple Model	**Detailed Model**
Problem Prevention	**Problem Solving**
Incomplete Information	**Accurate Information**
System Oriented	**Component Oriented**
Leading Design	**Following Design**

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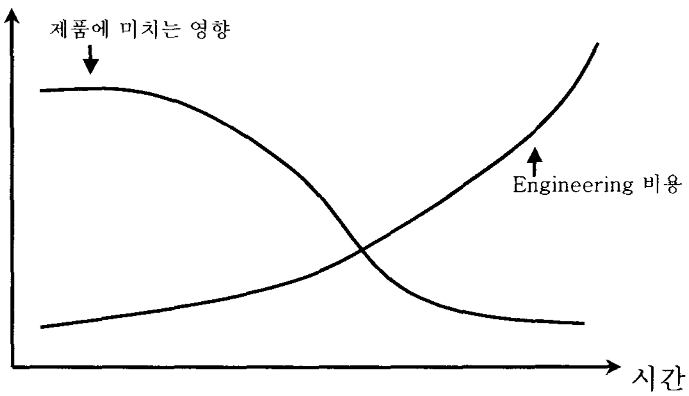
개발 효율 함수



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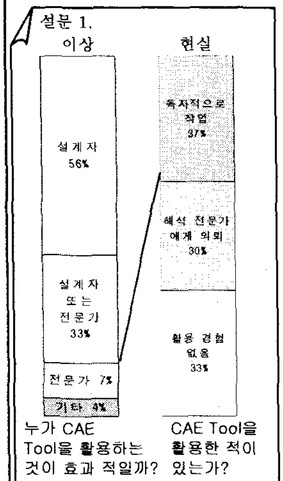
시뮬레이션 적용이 부진한 이유

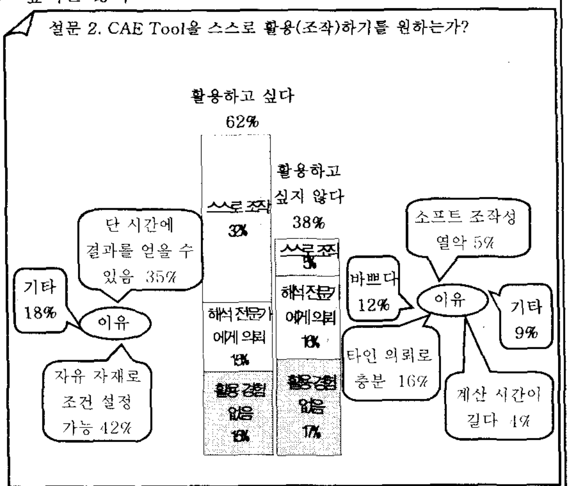
- 경영층의 이해 부족
- 응용의 미숙
- HW / SW 의 미비
- 설계 PROCESS 미흡

일본 기업의 CAE 활용실태 조사

(2000.4.일본 Digital Engineering 보고서)

1. 효과는 인정하지만 사용하고 싶지는 않다





Aerospace Application

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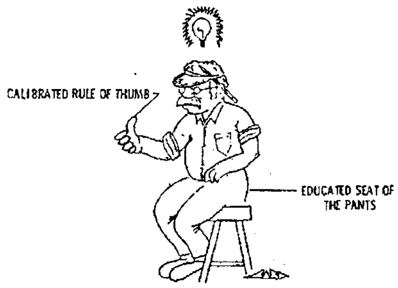
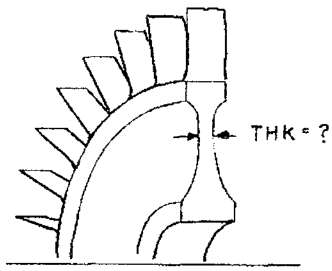
BACKGROUND

We need to recognize at least two stages in the design process.





CENCEPTUAL : "I think a disk will do the job."

OPTIMUM SIZING : "What size should I make it?"

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THE OPTIMIZATION PROCESS

The optimization process is most easily understood in terms of a magic box speaking to the engineer.

"TELL ME YOUR PROBLEM"

MAGIC BOX

ANALIZ (analysis)	COPES (control)	CONMIN (optimizer)
"TELL ME WHAT TO RUN"	"I WILL DIRECT TRAFFIC"	"TELL ME THE ANALYSIS RESULTS"

"THIS IS THE BEST SOLUTION THAT I CAN FIND"
"DO YOU APPROVE?"

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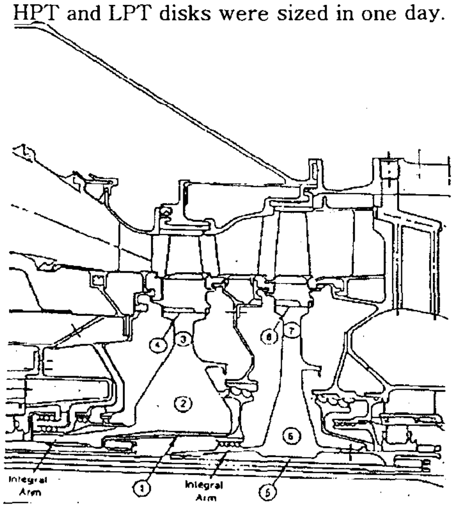
AUTODISK IMPROVES PRODUCTIVITY

The PW3005 HPT and LPT disks were sized in one day.



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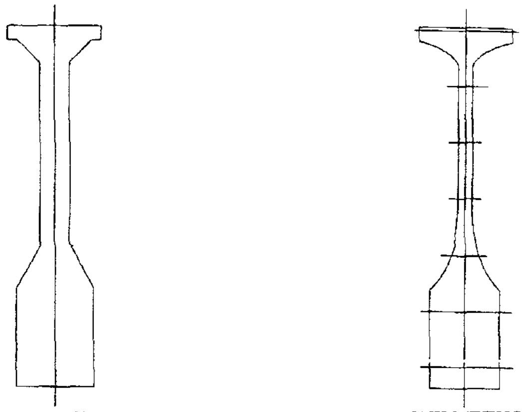
AUTODISK IMPROVES PRODUCTIVITY & QUALITY

A 25% weight reduction was realized in the STJ562 3rd stage LPC disk.

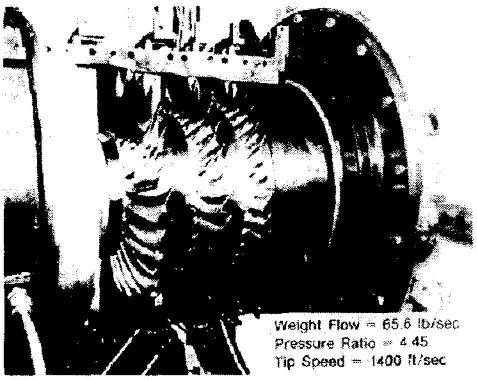


OLD METHOD :

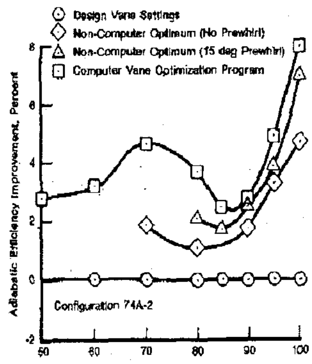
WT - 31.1 lb

NEW METHOD :

WT - 23.3 lb



Three-stage core compressor



Percent Design Speed

$$\Delta f \simeq \nabla f^{T} \cdot \Delta \bar{x} + \frac{1}{2} \Delta \bar{x}^{T} [H] \Delta \bar{x}$$

Automotive Application

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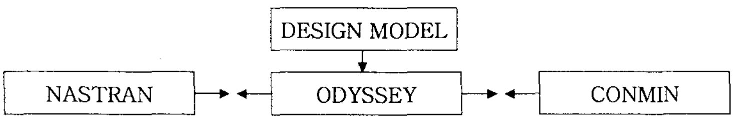
ODYSSEY FUNCTIONALITY PROVIDES;

1. DESIGN **INTERFACE** THROUGH DESIGN PARAMETERS
   (GAGE, WIDTH, HEIGHT, ETC.)
2. **BRIDGE** BETWEEN THE DESIGN MODEL, THE ANALYSIS SYSTEM
   (*NASTRAN*) AND THE OPTIMIZER (*CONMIN*)
3. **APPROXIMATE** NASTRAN **ANALYSIS** DURING OPTIMIZATION (REDUCE $)
4. **CONTROL** OF DESIGN, MANUFACTURING AND PRACTICALITY **REQUIREMENTS**
5. **MULTIPLE** ANALYSIS **SOLUTIONS** UNDER MULTIPLE LOADING CONDITIONS



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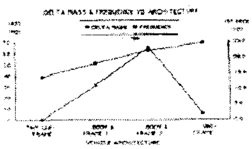
VEHICLE STRUCTURE OPTIMIZATION

PURPOSE — TO OBTAIN THE MOST MASS EFFICIENT BODY STRUCTURE WHICH MEETS THE ESTABLISHED STIFFNESS REQUIREMENTS

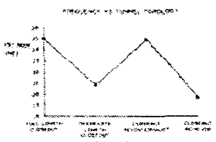
METHOD — 1) IDENTIFY THE BEST OVERALL VEHICLE ARCHITECTURE
2) IDENTIFY KEY TOPOLOGY ATTRIBUTES AND ASSESS ALTERNATIVES

PAYOFFS — SYNTHESIZED BODY STRUCTURE DESIGN ENABLING ALL VEHICLE LEVEL RIDE SPECIFICATIONS TO BE ACHIEVED WITHOUT EXCEEDING MASS REQUIREMENTS (C.A.F.E., ACCELERATION, ETC.)AND PACKAGING BOUNDARIES(ENTRY, EGRESS, ETC.)

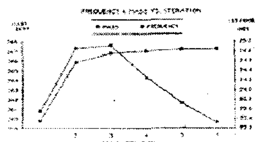
1) VEHICLE ARCHITECTURE



2) STRUCTURAL TOPOLOGY



3) SECTION/GAGE OPTIMIZATION



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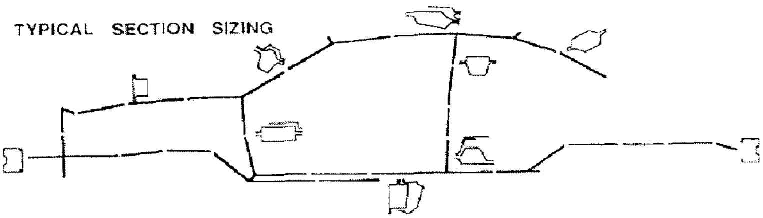
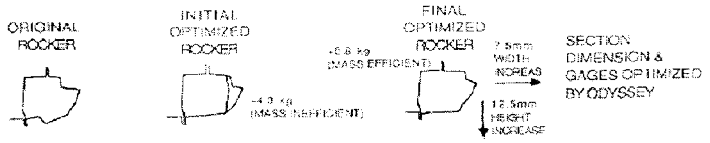
VEHICLE STRUCTURAL OPTIMIZATION

TYPICAL SECTION SIZING



TYPICAL OPTIMIZED SECTION



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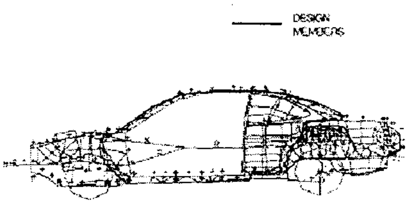
VEHICLE STRUCTURAL OPTIMIZATION

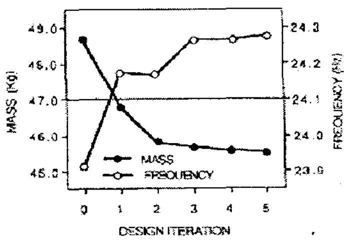
PURPOSE: TO OPTIMIZE GLOBAL BODY STRUCTURE SUBJECT TO VEHICLE PERFORMANCE REQUIREMENTS

PAYOFFS: BALANCED DESIGN (EFFICIENT MASS. PART REDUCTION)
DESIGN TIME REDUCTION & TIMELY DESIGN FEEDBACK

EXAMPLE:



BODY STRUCTURE OPTIMIZATION MODEL



MASS&FREQUNCY VS. DESIGN INTERAC

REAR UPPER CONTROL ARM SHAPE OPTIMIZATION STUDY

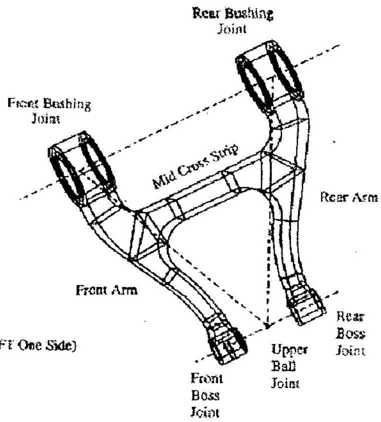
Objective:

Minimize Total RUCA Mass

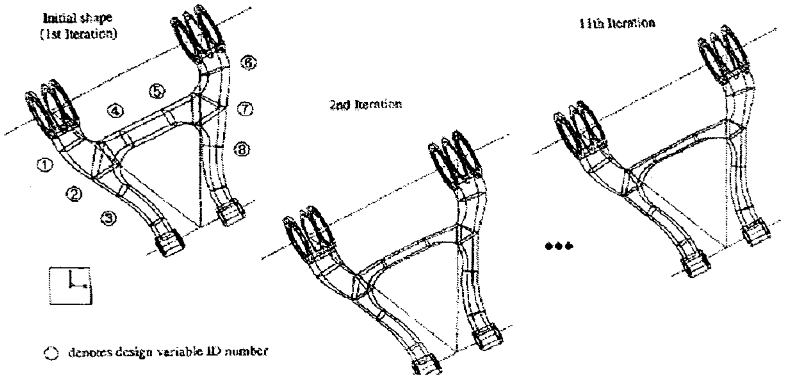
Subject to:

1. Packaging Size
2. Max. σ_{vm} < 205 Mpa (or 172 Mpa)
3. Frequency λ_i < 220 Hz
   or 250 Hz < λ_i , for all $i \in N$

Note: i. Apply pot hole loading (6.5G Bump Vertical + 2G AFT One Side) for stress analysis.
ii. Include bushing rate for modal analysis.



REAR UPPER CONTROL ARM RECTANGULAR X-SEC. SHAPE HISTORY



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Semiconductor Application

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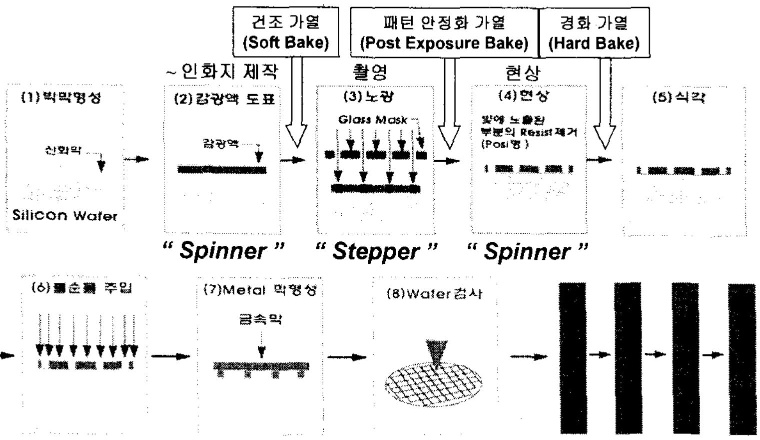
반도체 제조 공정

- ***Spinner*** : 감광액 도포, 감광액 건조, 현상
- ***Stepper*** : 회로 패턴 촬영



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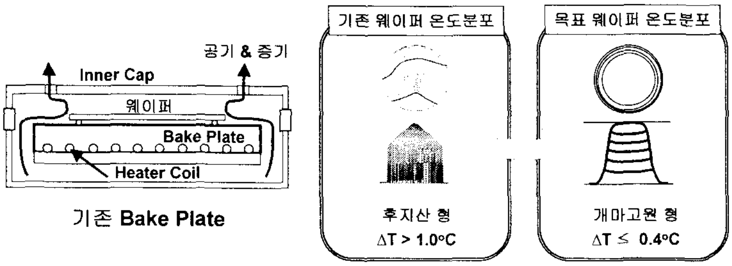
배 경

- **Deep-UV Lithography 공정 Spinner Bake Unit**
  - 웨이퍼 온도편차가 회로선폭 변화를 유발시켜 생산성 감소 발생
- 기존 통판형 구조 **Bake Plate**
  - 웨이퍼 온도 균일도 유지 한계 **(현재, 온도편차 1.1°C)**
  - **Giga DRAM** 및 **300mm** 웨이퍼 공정 적용 불가



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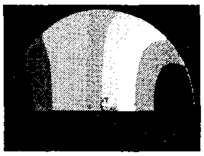
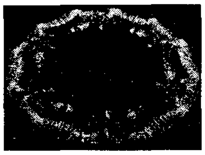
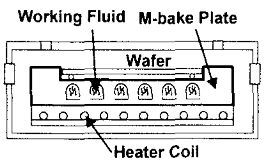
Heat Pipe 방식 Bake Plate 개발

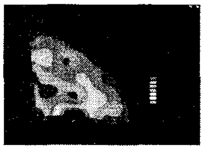
- 웨이퍼 수평도 유지 방안 제시 및 **Bake Unit** 내부 공기유동 제어
- 가존 통판형 **Bake Plate** 한계 극복

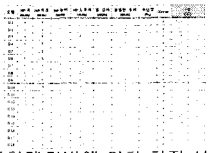
  → **Heat Pipe 방식 Bake Plate 개발 (M-bake Plate)**





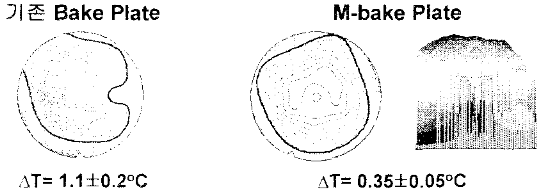


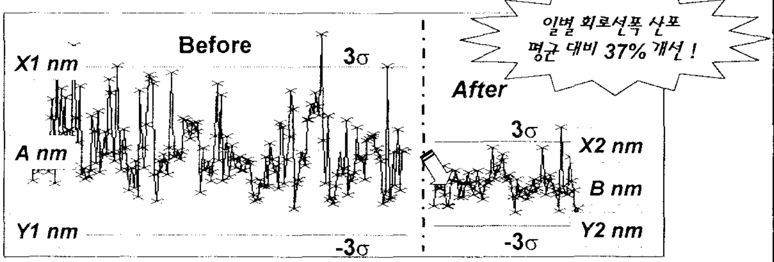




실험계획법에 의한 최적 설계

웨이퍼 온도분포 및 M-bake 적용 전후





성공적 적용을 위한 제안

- 경영층의 충분한 이해
- 충분한 초기투자/지속적인 관리
- 지속적인 교육 (OJT)
  - Modeling Know-How 개발
  - Process에 맞는 응용
- 설계 Process에서 CAE 적용의 의무화

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