# VLSI design of a shared multibuffer ATM Switch for throughput enhancement in multicast environments

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# 멀티캐스트 환경에서 향상된 처리율을 갖는 공유 다중 버퍼 ATM 스위치의 VLSI 설계

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## Abstract

This paper presents a novel multicast architecture for shared multibuffer ATM switch, which is tailored for throughput enhancement in multicast environments. The address queues for multicast cells are separated from those for unicast cells to arbitrate multicast cells independently from unicast cells. Three read cycles are carried out during each cell slot and multicast cells have chances to be read from shared buffer memory(SBM) in the third read cycle provided that the shared memory is not accessed to read a unicast cell. In this architecture, maximum two cells are queued at each fabric output port per time slot and output mask choose only one cell.

Extensive simulations are carried out and it shows that the proposed architecture has enhanced throughput comparing with other multicast schemes in shared multibuffer switch architecture.

## I. Introduction

Recently, applications emerge such as video conference and video-on demand which need the point-to-multipoint support in the ATM switch system. The support of multicast function at ATM switch level is essential in order to implement a high-efficiency ATM switch system for those applications. In this paper, a novel multicast scheme is proposed in which the addresses of unicast cells and multicast cells are stored in different address queues and a multicast cell is read from a shared buffer memory(SBM) in the last third read cycle, only if the SBM is not used to read a unicast cell. In the proposed scheme, the multicast cells do not affect the HOL blocking of unicast cells and the utilization of output ports increases because both unicast and multicast cells have the opportunity to be read for each output port.

## II. Switch architecture for enhanced throughput in multicast environments

The shared multi-buffer switch architecture is designed as shown in Figure 3.1. Incoming valid cells are written into the shared buffer memories(SBMs) in parallel directed by the SBM write controller. The SBM write controller gives write priority to the SBMs in the order of amount of vacant cell space of SBMs. The less filled SBM is given higher priority for cell write. Thus, the multiple memories can be regarded as a single large shared memory. The address queues are maintained separately for unicast cells and multicast cells. The address queues store the SBM-numbers and the SBM-addresses where the corresponding cells are written. The queues for unicast cells are configured as FIFOs dedicated for output ports.

A multicast address queue is maintained for each MCI(Multicast Connection Identifier). An MCI is assigned when a multicast connection is set up and used to identify each multicast cell.

To cope with the throughput aggravation originating from the HOL(Head Of Line) blocking, three consecutive read cycles are carried out for SBMs. During the first two read operations, only unicast cells are read from SBMs and multicast cells are given chance to be read in the third read cycle. Each multicast cell which is scheduled to be read for each output port, is read from the corresponding SBM only if the SBM is not used to read a unicast cell in the third read cycle. When both a unicast cell and a multicast cell arrive at an output port, the cell whose queue length is longer is sent through the output port.

In this architecture, the utilization rate of the output port increases because both a unicast cell and a multicast cell have the opportunity to be read for each output port. Moreover, the HOL blocking that unicast cells experience is not augmented by multicast cells, which gives the enhanced throughput in multicast environments.

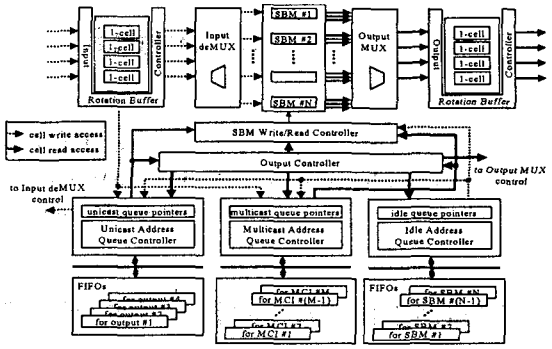


Figure 2.1. The architecture of designed shared multibuffer ATM switch

## III. Proposed multicast architecture

One write operation and three read operations are carried out for the shared memories during one cell time slot to cope with the throughput aggravation originating from HOL blocking. Multicast cells are read from shared memories which are not used to read unicast cells in the third read cycle so that the increased multicast traffic does not affect the HOL blocking among unicast cells.

Address queues for multicast cells are separated from those for unicast cells. Address queues for unicast cells are maintained for each output port and the cells in the head of line in unicast address queues are scheduled to be read out from shared memories. To resolve the order of read for unicast cells involved in HOL blocking, queue lengths of the unicast cells are compared and the unicast cell that has the longer queue length occupies the higher read priority. Multicast cells are identified by their multicast connection identifier(MCI). Address queues for multicast cells are maintained separately, for each MCI. Multicast cells are read out separately for their

destination ports to enhance the throughput of multicast cells. Accordingly, read pointers in a multicast address queue are supported for its destination output ports. The multicast cell whose queue length is longest for each output port is scheduled to be read out from shared memories in the third read cycle. The queue lengths of unicast cells and multicast cells that are scheduled to be read from shared memories are compared at output ports and the cells whose queue length is longer, are read out from shared memories and sent out through output ports. The utilization rate of output port is increased because a unicast cell and a multicast cell each has a chance to be read out for each output port.

Figure 4.1 shows the proposed multicast scheme. In the figure, unicast cells destined for output port #1, #2 and #4 reside in the same SBM and the HOL blocking occurs among the cells. In the first read cycle, access to the SBM #4 is made to read a unicast cell for output port #3 and the cell whose destination port is #1, is read from SBM#2 because the cell has the highest read prioirty among the cells involved in the HOL blocking. The cell destined for output port #2 is read from SBM#2 in the second read cycle. The multicast cell whose destination port is #2 has the highest read priority among the multicast cells. However, the multicast cell is not read because the SBM#2 is used to read a unicast cell in the third read cycle. The multicast cells destined for output port #1 and #3, respectively, are read in the third read cycle.

The performance of the shared multibuffer ATM switch architecture developed in this paper is evaluated for its cell loss rate, throughput and average queue length through extensive simulations. The performance evaluation is carried out for the random load and the burst load in unicast traffic mode and in mixed traffic mode, respectively. Fanouts of multicast cells and the arrival rate of multicast cells are used as variables for the performance evaluation. The shared multibuffer ATM switch developed in this paper shows enhanced performance compared with that of shared multibuffer ATM switch employing address copy multicast scheme for all simulation conditions.

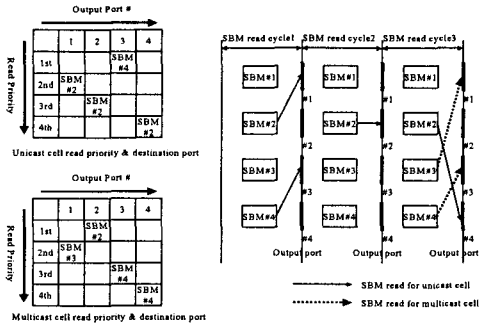


Figure 3.1. An example for the proposed multicast scheme

## IV. Simulation Results

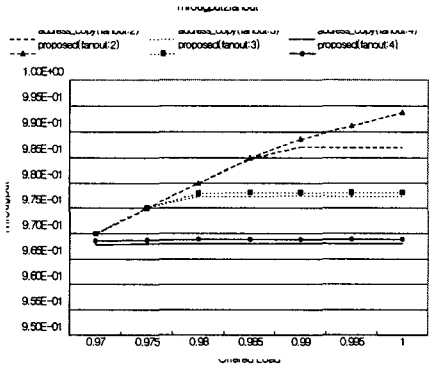


Figure 4.1. Comparison of Throughput between the Proposed Architecture and the Address Copy Multicast Architecture for Fanouts of Multicast Connections in Random Mixed Traffic (Multicast Cell Arrival Rate : 0.01)

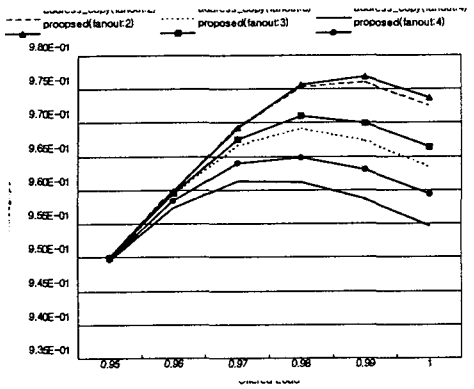


Figure 4.2. Comparison of Throughput between the Proposed Architecture and the Address Copy Multicast Architecture for Arrival Rate of Multicast Cells in Bursty Mixed Traffic (Offered Load : 0.99, Fanout : 3)

## V. VLSI Design

The developed ATM switch architecture is designed in VLSI. The switch is configured to have 4 x 4 ports, has 8 shared memories and accommodates 128 cells per port. The circuit is synthesized in 0.6um CMOS triple metal single poly process and gate simulation is carried out with worst case operating conditions. The switch contains about 640,000 transistors and the critical path lies in the write path of input rotation buffer. The maximum operating frequency is 20MHz and the power dissipation of the switch is 834.4mWatt at 20MHz with 3.3Vdd. The switch supports 155.52Mbps STM-1 source rate per port.

## VI. Conclusion

In this paper, a shared multibuffer ATM switch architecture is proposed. The switch shows enhanced throughput in multicast environments. Multicast cells are identified by multicast connection identifier(MCI) and read pointers are maintained for each output port as well as for each MCI(or for each multicast address queue) because multicast cells are read separately for each destination port. Multicast cells are read only in the third read cycle from shared memories when there remains no head-of-line unicast cells unread in the shared memories.

The performance of the proposed switch architecture is evaluated by extensive simulations. The performance of the switch is compared with that of the shared multibuffer ATM switch adopting the address-copy multicast scheme.

The switch is designed in VLSI to have 4 x 4 input/output links. The switch can accommodates 155.52Mbps STM-1 input/output links. The power dissipation is estimated to 834.4mWatt at 20MHz.

## 참고문헌(또는 Reference)

[1] JongIck Lee, JongMoo Sohn and MoonKey Lee, "Throughput Enhancement of Shared Multi-buffer ATM Switch in Multicast Environments," IEICE Transactions on Communications, Vol.E82-B, No.12, pp.2153~2159, Dec., 1999

[2] JongIck Lee, JongMoo Sohn and MoonKey Lee, "Design of a Shared Multi-Buffer ATM Switch with Enhanced Throughput in Multicast Environments," 대한 전자공학회 논문지, 제36권 S편 4호, pp.1-11, 4월, 1999

[3] N. K. Sharma, "Review of recent shared memory based ATM switches," *Computer Communications*, vol. 22, pp. 297-316, 1999