BGA to CSP to Flip Chip – Manufacturing Issues

By;

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Abstract

The BGA package has been the area array package of choice for several years. Recently, the transition has been to finer pitch configurations called Chip Scale Packages (CSP). Several of these package types are available at 0.5 mm pitch, requiring surface mount assemblers to evaluate and optimize various elements of the assembly process. This presentation describes the issues associated with making the transition from BGA to CSP assembly.

Areas addressed will include the accuracy of pick and place equipment, printed wiring board lines and spaces, PWB vias, in-circuit test issues, solder paste printing, moisture related factors, rework and reliability. The transition to 0.5 mm pitch requires careful evaluation of the board design, solder paste selection, stencil design and component placement accuracy. At this pitch, ball and board pad diameters can be as small as 0.25 mm and 0.20 mm respectively. Drilled interstitial vias are no longer possible and higher ball count packages require micro-via board technology.

The transition to CSP requires careful evaluation of these issues. Normal paste registration and BGA component tolerances can no longer achieve the required process levels and higher accuracy pick and place machines need to be implemented.

This presentation will examine the optimization of these critical assembly operations, contrast the challenges at 0.5 mm and also look at the continuation of the process to incorporate smaller pitch flip chip devices.

Key Words: Ball Grid Array (BGA), Chip Scale Package (CSP),

Introduction

As array area components continue their trend toward smaller pitches they present new design opportunities and manufacturing challenges. Typical Ball-Grid-Array (BGA) devices having 1.27 or 1.00 mm pitch and fine pitch BGAs having 0.8 to 0.75 mm pitch were able to be incorporated into the standard Surface Mount Technology (SMT) manufacturing flow quite easily. As the device pad pitch reduced to 0.5 mm multiple issues with respect to design, materials, manufacturing, inspection and rework became evident. Figure 1 contrasts these issues.

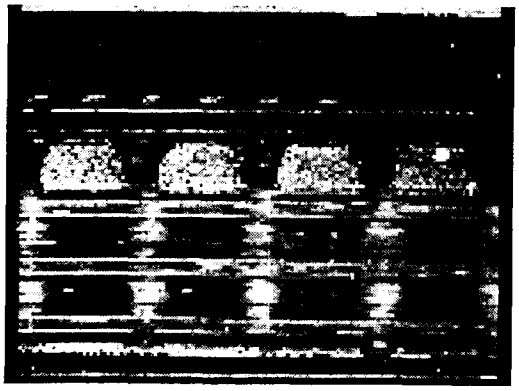
BGA assemblers and component suppliers frequently used standard design rules when incorporating these devices into circuit board configurations. Although ball compositions, package structures and materials differed, excellent assembly defect levels (<20 ppm) and board level reliability were routinely obtained. Chip-Scale-Packages (CSP) required new circuit routing, component placement accuracy, solder paste printing, cleaning and rework methodologies. Figure 2 are pictorials of the cross sections of a 1.27 mm PBGA and a 0.5 mm CSP shown at identical magnifications, illustrating the circuit routing challenges presented by CSP assembly.

Figure 1: 50 mil BGA & 0.5 mm CSP

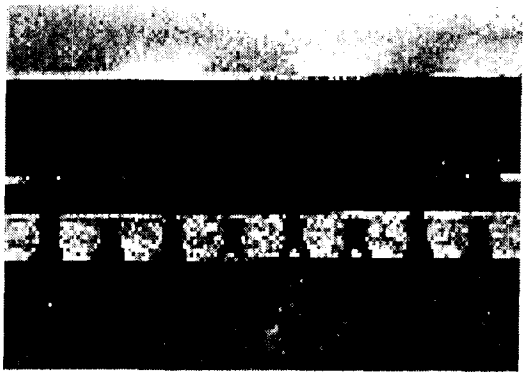
Process	BGA	CSP
P & P Accuracy	Drop In	Drop In ...
PWB L & S	Drop In	Fine Line
PWB Vias	Drop In	Photo Vias
In-Ckt Test	Drop In	Extinction?
Printing	Drop In	Pushes Art
P & P Vision	Pushes Limits	Exceeds Limits
Moisture	Tight Controls	Tight Controls
Rework	Major Change	Major Issue

Figure 2. Cross Sections of 1.27mm PBGA and 0.5 mm CSP

PBGA



CSP



Board Design

Typical BGA board design with 1.27 mm pitch devices use 0.64 mm diameter etch-defined pads, which easily accommodate 0.13 mm line/space and interstitial vias with capture pads. Below 1.0 mm pitch, however, any full array larger than 6x8 requires more costly board design parameters. As Table 1 shows, 0.75 mm pitch requires a reduction in both the CSP pad and the via capture pad, and also requires the board fabrication facility to maintain tighter copper-to-copper clearances. The small CSP pad also creates difficulties in the solder paste printing operation.

With single channel routing, at any pitch, a full array of n rows and m columns can be routed without interstitial vias if the condition of equation 1 is met:

$2(m+n-2) \geq (m-2) \times (n-2)$ Equation (1)

At 0.65 mm pitch, any required interstitial vias are 0.20 mm in 0.45 mm pads, suggesting that cost-competitive microvia-in-pad designs may be a better solution for high pin count arrays. Finally, at 0.5 mm pitch, microvia technology becomes essential except for small arrays satisfying Equation 1. Solder Mask Defined (SMD) CSP pads reduce the risk of exposed traces from typical solder mask misregistrations which could introduce shorts during subsequent assembly. Some packages exhibit reduced accelerated thermal cycling life with SMD pads. Anti-pads for internal voltage and ground planes are generally larger than external via capture pads (0.5 mm over drill diameter versus 0.3 mm). Such power and ground via clearances can affect the integrity of the internal planes at pitches of 0.8 mm and below, resulting in reduced board manufacturability and/or compromised electrical performance when using drilled interstitial through-vias. Board technology selection is also influenced by the overall wiring density, cost, and form factor requirements of the final design.

Board surface finish becomes significant at tighter pitches. Although solder leveled, immersion Ni-Au, and OSP copper finishes have all been used successfully with CSP assemblies, hot air solder level is not recommended due to the inherent non-planarity in the finished surface. This can be a problem at 0.5 mm pitch where the combination of reduced CSP ball diameters (around 0.3 mm) and printed paste

volumes create instabilities during CSP placement and reflow.

Solder Paste Printing

BGAs are typically printed using stencil apertures of similar size to those of the board attachment pads. Extending this guideline from 0.635 mm pads at 1.27 mm pitch to 0.30 mm pads at 0.50 mm pitch causes reduced assembly yields. When a the CSP pad is reduced to 47% of the BGA pad diameter, the theoretical CSP paste volume (using a 0.125 mm foil) is reduced to just 22% of that of the BGA. This presents several problems. First, the Area Aspect Ratio (AAR) of the stencil aperture becomes so small that the printing efficiency is reduced, producing releases as low as 50% of theoretical. The AAR is defined as the area of the aperture divided by the aperture wall area; for circular apertures the AAR is defined by equation 2:

Area Aspect Ratio = D / 4t Equation 2

Table 1: Board Design Parameters at Different CSP Pitches

	ARRAY PITCH (mm)					
Parameter	**1.00**	**0.80**	**0.75**	**0.65**	**0.50 with microvia in pad [a]**	**0.50 with no vias [b]**
Pad diameter (NSMD except where noted)	0.45	0.35	0.30	0.26	0.36	0.30
Pad type [c]	NSMD				SMD	
Microvia in pad ?	Optional			Preferred	Yes	No
Solder mask diameter (around pad)	0.58	0.48	0.43	0.39	0.26	0.25
Stencil aperture (contact side)	0.45	0.40	0.35	0.31	0.30	0.30
Line width (escape traces)	0.13	0.13	0.13	0.13	no line	0.07
Interstitial vias?	Yes				No	
Via capture pad diameter	0.64	0.51	0.51	0.45		
Solder mask (on capture pad)	0.43	0.38	0.38	0.38		
Finished hole	0.30	0.25	0.25	0.20		
Resultant Cu to Cu clearance	0.162	0.136	0.125	0.105	0.140	0.065

(a) Preferred 0.5 mm routing: Microvia in pad with no escape routing between pads.
(b) Alternate 0.5 mm routing: for footprints route-able without interstitial vias.
(c) SMD = solder mask defined, NSMD = etch defined

where D = aperture diameter and t = foil thickness. Critical AAR values depend on paste mesh size and foil thickness, but AARs below 0.8 typically require careful printing optimization: typical CSP apertures fall in the range of 0.6 to 0.9. For a 0.5 mm pitch CSP printed with a 0.3 mm aperture in a 0.125 mm foil, the AAR is 0.6. Second, any off-set of the paste print combined with the poor release, produces a significantly reduced tack area (see Pick & Place below). Finally, many in-line solder paste measurement systems are not able to accurately measure such low paste volumes, creating the risk of sporadic, unpasted pads continuing through the assembly process. Higher cost paste inspection equipment is needed at 0.5 mm pitch.

Solutions to these printing challenges include the use of laser-cut trapezoidal apertures below 1.0 mm pitch, and the use of more costly nickel build-up stencils for 0.5 mm pitch; the latter offer improved print quality and up to 70% more paste release at 0.5 mm pitch than traditional stencils. Solder paste particle size can also be changed from the typical Type III pastes (max. particle size 53 microns) to the finer grain Type IV or V pastes. Some benefits are found with Type IV at 0.5 mm pitch printing, but Type III typically exhibits less slumping, improved flux activity for other SMDs, and works well for CSP pitches of 0.75mm and greater. Care should be taken in evaluating pastes for fine pitch CSP applications:

printing characteristics and activity vary greatly between the major paste suppliers. Frequently, small CSP pads are over-printed larger than the pad size (e.g. 0.35 mm diameter print on 0.30 mm pad) to improve the process capability indices.

Classically, the attachment of conventional SMT devices has followed the guidelines of IPC-610C with respect to the amount of the component lead that can be off the pad and yet result in a successfully bonded solder joint. When this same guideline is applied to CSP devices a failure condition can occur as a result of the paste print being off slightly in one direction, while the device placement is slightly off in the opposite direction. An open can occur due to the misalignment of the two elements of the manufacturing process. Figure 3 illustrates this issue and clearly depicts the "Fallacy" that CSPs can be solder reflowed using the same parameters as more conventional devices. Clearly the same level of misalignment allowed for fine pitch flat pack devices will result in a no connect with CSPs. Figure 4 is a pictorial of a screen printed site for a 0.4 mm component and an X-ray of the site after placement of a component.

Figure 3: The 0.5 mm Fallacy

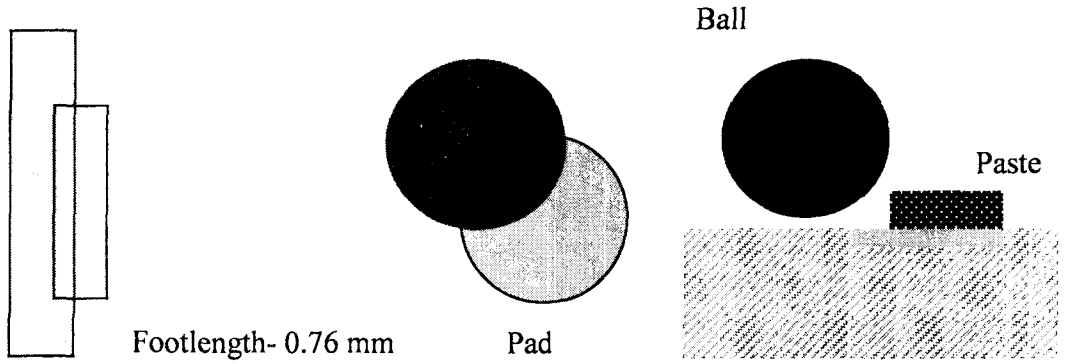


Figure 4: Screen Print and X-Ray of 0.4 mm pitch flip chip device on wet paste

Pick and Place Accuracy

Given the choice of CSP shipping media: trays or embossed tape & reel, many prototype and early volumes of evaluation parts are supplied by the manufacturer in trays or waffle packs. This allows parts to be easily removed manually for inspection, test, or sampling, but reduces the assembly rates. Fine pitch placement machines usually have the ability to pick directly from trays but small parts in large tray arrays can be problematic. One challenge occurs when the depth of the pocket is significantly greater than the part height. Some machines can not be programmed to descend into the pocket to retrieve

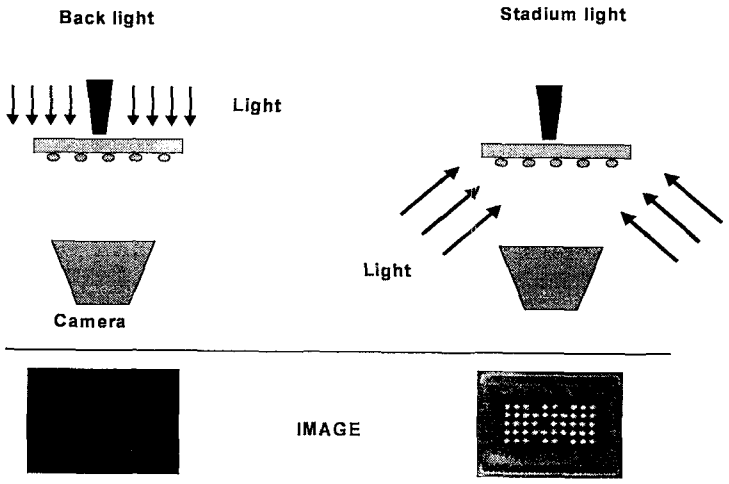
the CSP part. Another challenge can be the 'run-out' of the part location in the tray. The effect of reduced placement speed should also be considered when using trays. Multi-functional placement machines are usually capable of handling parts from tape and reel or trays, when the options are installed, but part placement from tray is significantly slower than from tape & reel.

Tape and reel also offers the advantage that part misorientation can not occur from the reel being loaded incorrectly into the machine. Tape and reel would be the preferred shipping medium for CSPs for a combination of these reasons. Actual speeds depend on the tool manufacturer and it's configuration, but flash memory CSPs at 0.75 mm pitch can be placed approximately four times faster than their 0.5 mm pitch TSOP equivalent. The degree of sophistication of the placement tool vision systems and package type affects the component placement accuracy and the frequency of false rejects. Back lighting is suitable for CSP pitches down to 0.75 mm only when the combination of ball array to part edge tolerance and the placement accuracy, is acceptable.

0.5 mm pitch parts require more accurate registration and are generally placed using a fine pitch placement tool, either using edge recognition or stadium lighting for ball inspection, Figure 5.

A brief analysis of tack area illustrates the importance of establishing the printing and placement tolerances: The tack area (reference Figure 3) represents the projected intersectional area of the ball and solder paste for a worse case paste release of 0.25 mm diameter, and component placement error of 0.038 mm. When the 0.13 mm thick paste is misregistered by just 0.05 mm, the tack area for the CSP ball is only one-fifth that of a 1.27 mm pitch BGA. If the combined paste-to-part registration exceeds this, in addition to a poor print, there is virtually no tack area to retain the part during assembly or promote self-alignment during reflow.

Figure 5: Front versus back lighting



Inspection and Rework

As with BGAs, x-ray inspection of assemblies is rarely done in-line but such instruments are essential for process development and in-process audits, allowing defects such as non-wets, shorts, and missing balls to be detected. In contrast to traditional BGAs, CSPs preclude visual inspection of the outer perimeter row of balls due to the small stand-off and frequent proximity of adjacent parts. Double-sided CSP assembly is routine and solder joint fillet geometries and reliability data are indistinguishable between top and bottom sides. Conventional X-ray technology is effective in identifying shorts under area array devices, however, they are not very suitable for identifying opens. X-ray laminography is a methodology that permits the identification of such defects.

Hot nitrogen rework is performed using processes analogous to those used for BGA rework, but site

paste re-printing is not practical at 0.5 mm pitch, requiring tacky flux to be used instead of solder paste. On dense assemblies, reflow of adjacent components is often unavoidable but reworked assemblies subjected to accelerated reliability testing have exceeded application requirements; again, the results are very package-specific.

BGA devices can also be re-balled so that the component can be salvaged and if necessary, reused. The process is quite simple. The device is removed from the circuit board using the hot nitrogen system. The device is cleaned and all residual solder is removed from the pads on the base of the device. The pads are filled with a specific volume of solder paste, replacement balls are added via a stenciling process, and the unit is reflowed. This is not yet possible with CSPs as the replacement balls are not produced in the diameters needed for the smaller pitch components. This issue should be eliminated in the near future.

Below 0.5 mm

Device pitch continues to get smaller. In fact flip chip devices are currently being used in volume manufacturing. These devices, at 0.3 to 0.4 mm pitch contend with the same manufacturing issues created by CSPs. Figure 6 illustrates the pad structure for a small device of this nature.

Figure 6a: 0.4 mm Flip Chip compared with an 0805 chip resistor

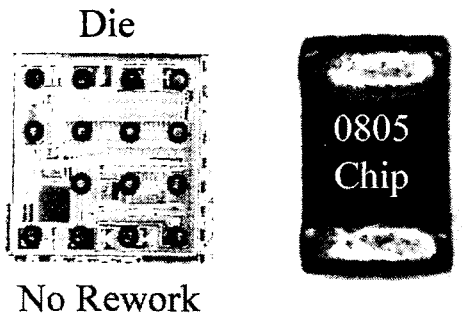
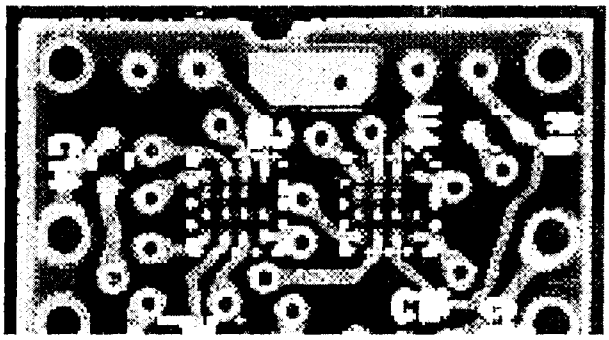


Figure 6b: 0.4 mm footprints for die in 6a.



Reliability

The major issues associated with the reliability characteristics of BGA and CSP device types is directly related to their smaller size and structure. Several consortia projects are in progress to assess board level reliability, but new packages continue to evolve as processes are modified to improve CSP reliability while simultaneously reducing costs. The CSPs reduced stand-off height and reduced Coefficient of Thermal Expansion (CTE), as compared to PBGAs, are an unfavorable combination for thermal reliability. However, optimized board design and a correct package can result in a long field life, with most achieving in excess of 1000 cycles of –55 to +125 C.

Conclusions

Much work remains to be done to effectively implement CSPs into the mainstream of manufacturing technology. The progress to date has resolved many of the issues associated with design and pad geometries. Continued research on the rework issue is neede to be able to effectively replace CSP devices. Adherence to the verified guidelines can lead the designer to the correct methods of optimization for assembly, test and rework that culminate in a reliable and cost effective implementation.

Acknowledgements

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