The 3rd Korea – Japan Advanced
Semiconductor Package Technology Seminar
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Micro-Fabrication Technologies Supporting Advanced Packages

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Contents

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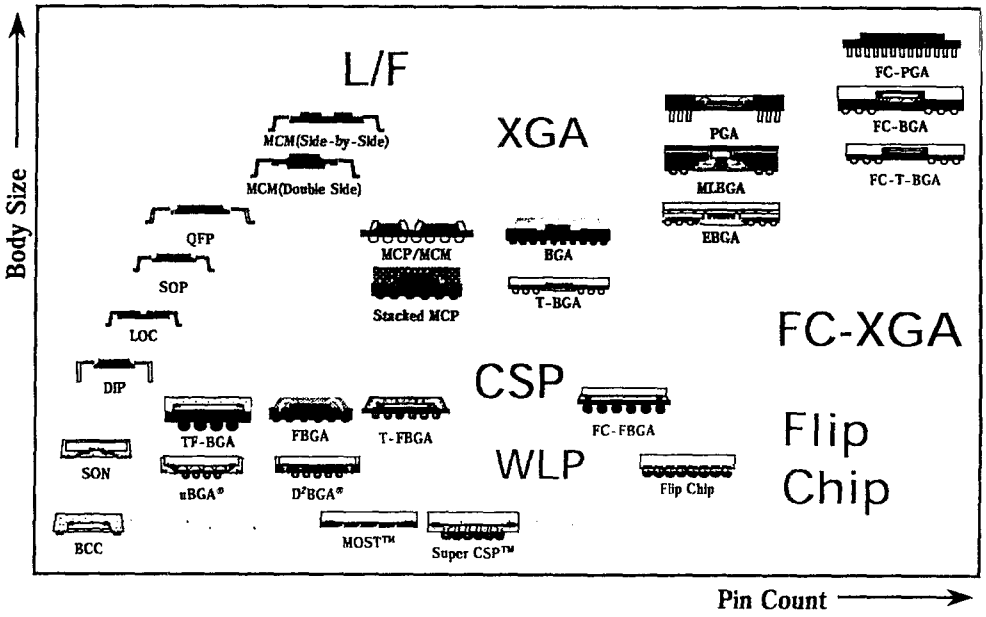
Packaging Family



Two Main Packaging Streams

Firm Package ? Light Package ?

★Package for MPU

①Stable Power Supply
②High Frequency Signal Transmission
③High Thermal Dissipation

★ Package for Flash,SRAM

①Small and Light Package as CSP、WLP
② Thin Silicon and 3D Stacking

at Reasonable Cost
With considering friendly environment

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Technology Transition in MPU Package

★Material Change

Ceramics to Plastic

★Package Type Change

PGA to Cartridge, and then to PGA

★Chip Bonding Technology Change

Wire Bond to Flip Chip Bond

High Density and High Performance PKG

Package for Memories

- Flash, SRAM and etc.

Relatively Large Chips with Small Pin Counts such as CSP, WLP etc.

Technology Requirements

①Bumping by

②Thin Film and Fine Line Patterning

③Micro Assembly

Microfablication Tech. Will Be Essential

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Technology Domain of Microfabrication

1 *fabrication of micro shapes*

fabricate micro electrode (bump etc.), probe, via, etc.
...Electrochemistry, Laser technology, Photolithography

2 fabrication of micro and nano structure

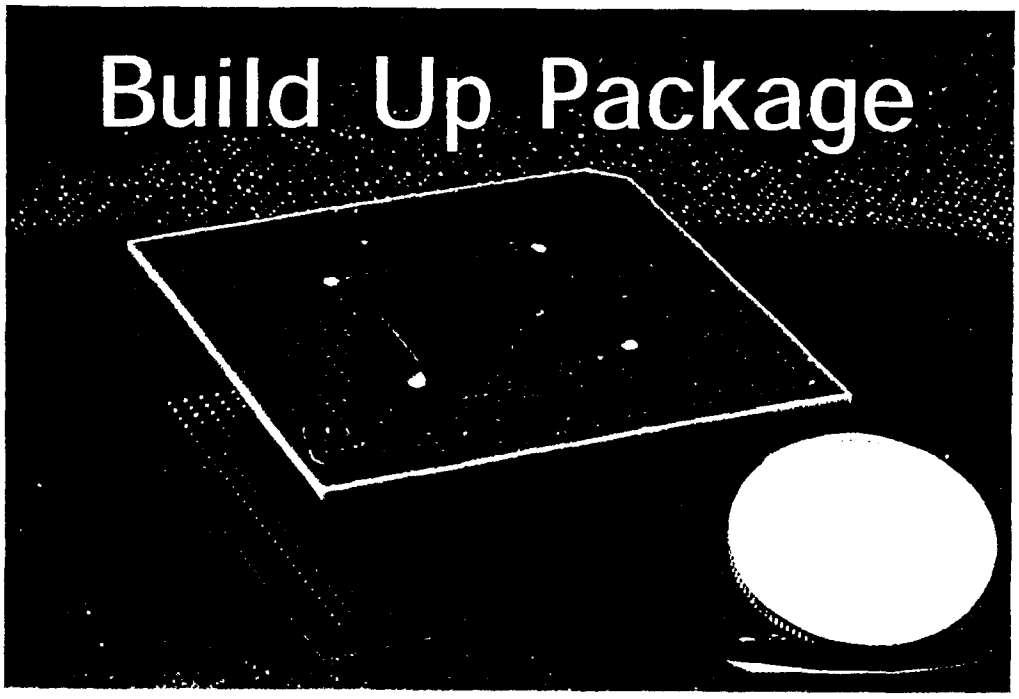
fabricate bumps with gradient structure,nano scale multi-layers controlled in lattice structure by super
...Electrochemistry (pulse plating)

3 fabrication and assembly of micro parts, structure and systems

fabricate L,C,R in build-up substrate
micro bonding (micro soldering, interconnect)
...Electrochemistry, Laser technology, Photolithography

4 Preparation the materials and processes for microfabrication

...Die tooling, Stumping, Laser technology, Simulation



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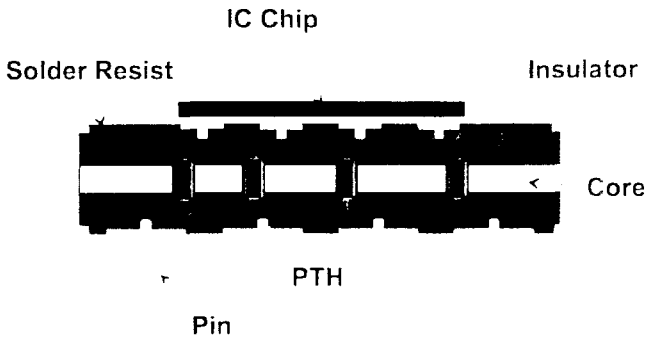
Road Map on Semiconductor Chip and Package

Years of production	*1999*	*2000*	*2001*	*2004*	*2008*	*2011*
technology node	*0.18um*		*0.13um*	*0.09um*	*0.06um*	*0.04um*
Performance: on chip/MHz						
Cost-performance	600	693	800	1100	1522	1925
High-performance	1200	1386	1600	2000	2655	3190
Chip pad count						
Cost-performance	370-740	400-821	432-912	544-1247	740-1893	932-2589
High-performance	1600	1792	2007	2820	4437	6234
Flip chip pad pitch/mμ	200	200	175	150	115	110
Line width mμ	40	30	23	16	11	8

Package structure



Flip Chip Pin Grid Array (FC-BGA)

Features:
- Vacuum lamination
- PTH plugging
- Cu plating on PTH
- Laser via
- Stacked via (via on PTH)
- Skipped via (L1-L3)

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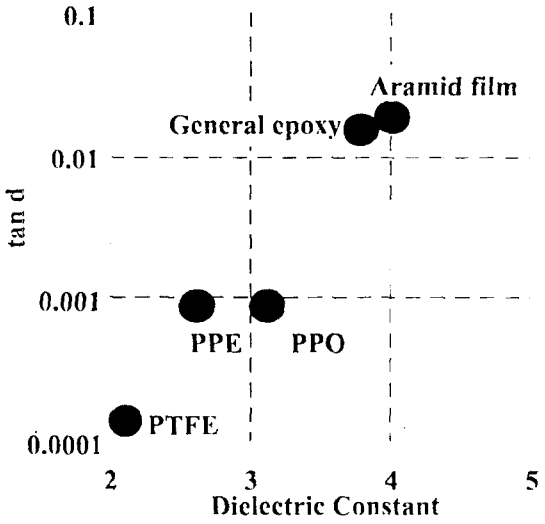
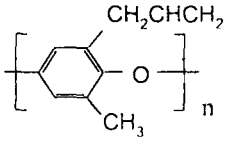
Dielectric Material

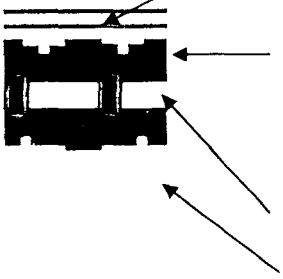
Dielectric Material Properties on Dielectric Constant and Dielectric Loss



PPE : Poly-Phenylene Ether



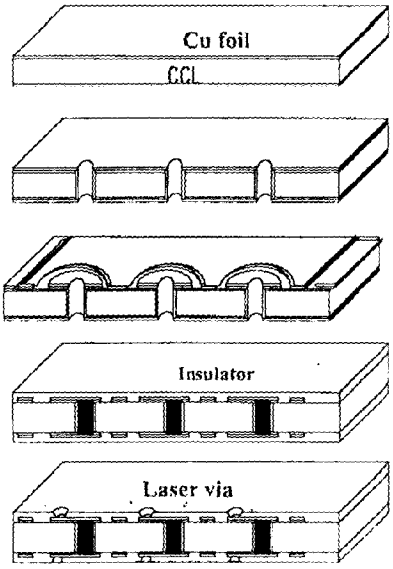
Package Design Guide



	Description	Year		
		2001	2003	2005
Flip chip pad	Pad pitch	200	180	150
	Pad opening size	120	100	80
	Mask clearance	20	18	15
Build up layer	Line/space	30	25	20
	Via size (CO2)	70	65	60
	Via land (CO2)	140	130	120
	Via size (YAG)	45	40	35
	Via land (YAG)	115	105	90
	Cu thickness	15-25	15-25	12-25
	Bu layer thick.	30-50	25-50	20-50
Core layer	Line/space	70	60	50
	PTH pitch	400-600	⇨	Coreless
Pin pitch	Pin pitch	1.27	1.27	1

unit (mm)

Package Fabrication Process



Core Material

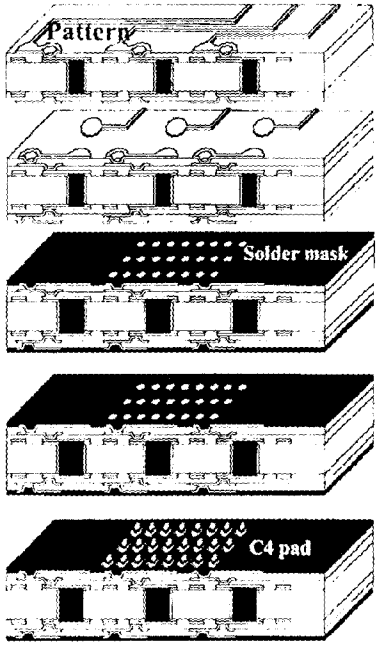
PTH drilling
PTH plating

Patterning
(Subtractive process)

1st Bu. layer lamination

Laser drilling
on 1st BU layer

Package Fabrication Process



Plating and patterning
on 1st BU layer

2nd Bu. Layer lamination
Plating and patterning
on 2nd BU layer

Solder resist formation

Ni/Au plating on FC pad

Pre-solder coat on FC pad

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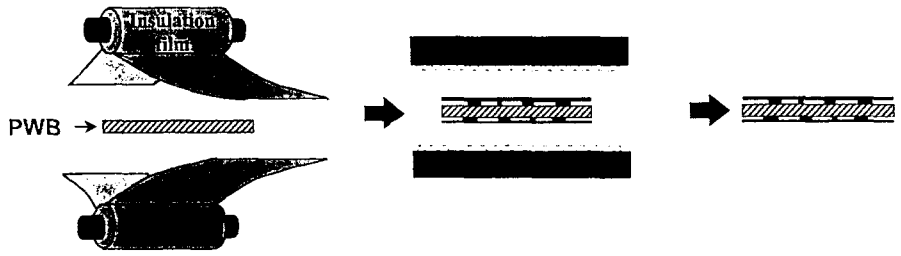
Specialized Process

1, BU Insulation lamination process



Film attach | Vacuum lamination | Complete

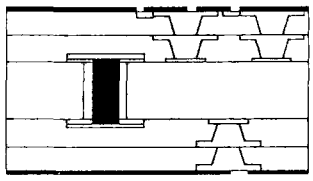
2, Via filling process

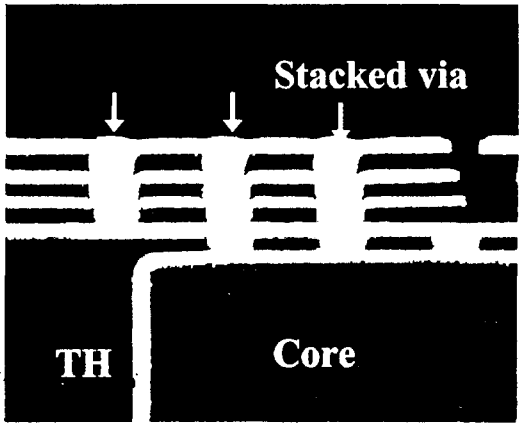
Using additives, both types of DC and PPR current are applicable.

Advanced Technology

- ✧Stacked vias filled with copper plating
- ✧New core structure Package
- ✧Embedded passive component

Stacked vias
filled with copper plating

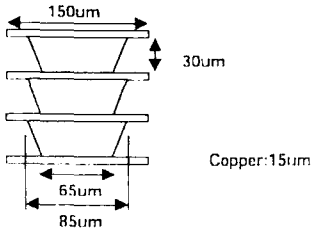




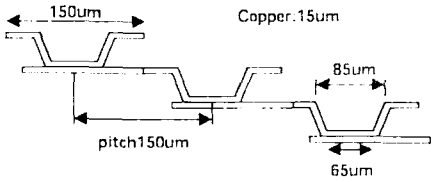
Stacked Vias

Simulation of Inductance on Stacked Vias

Model1 (Stacked Via)



Model2



Inductance

Model1	*46.9pH*
Model2	*191pH*

Stacked viaとStagger viaとでは約 4倍の違いが出ている
よって PWR/GNDのLoop Lを減らすためにはStacked viaは有効な方法

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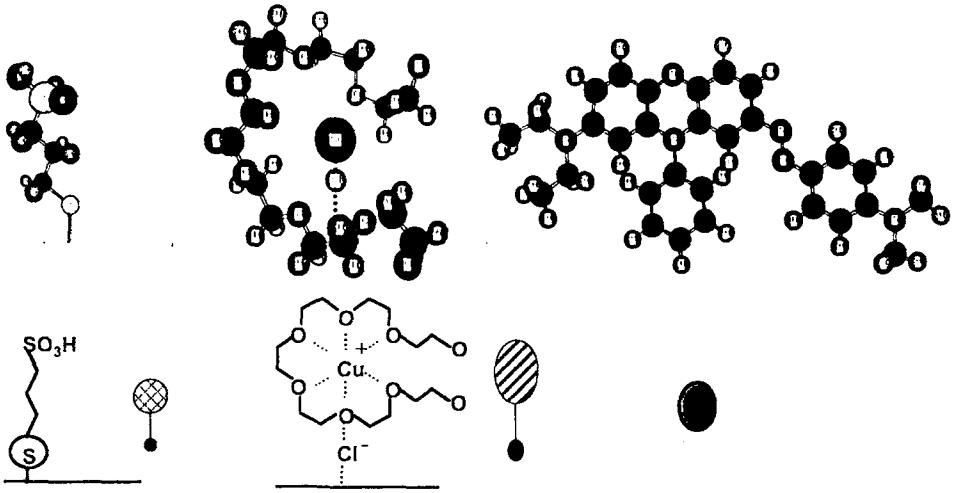
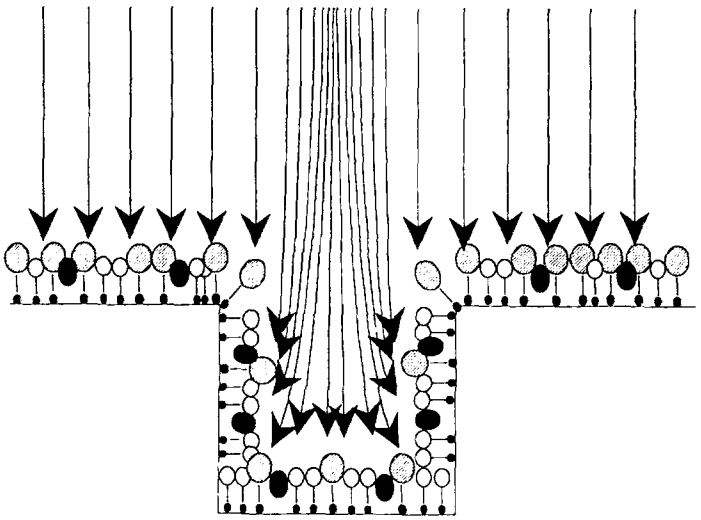
Structures of Additives



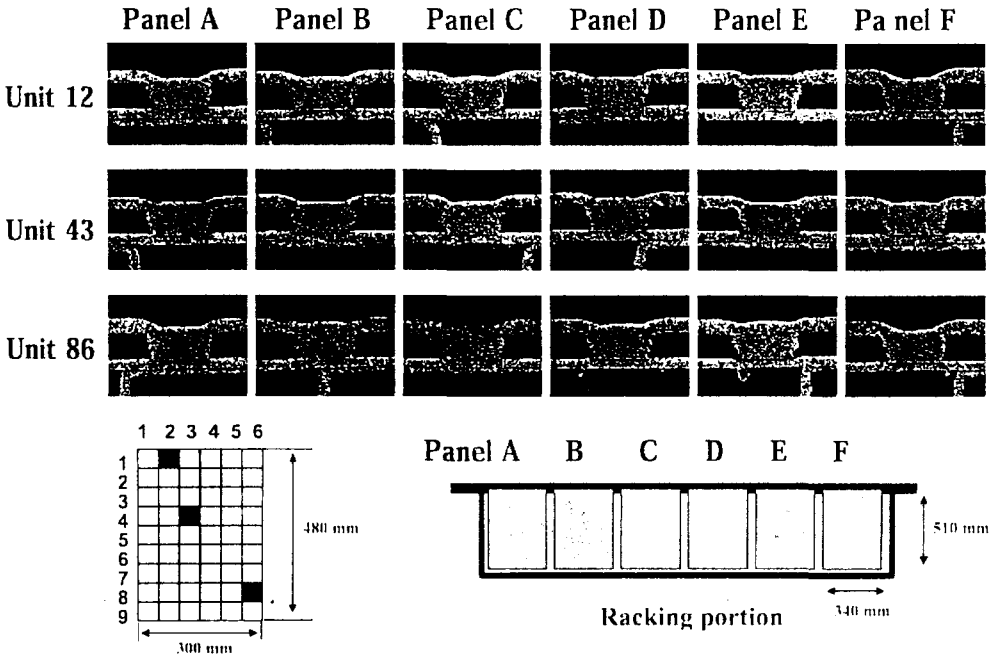
Chemical adsorption Physical adsorption

Brightener Polymer Dye

Current Distribution Model for Via Filling

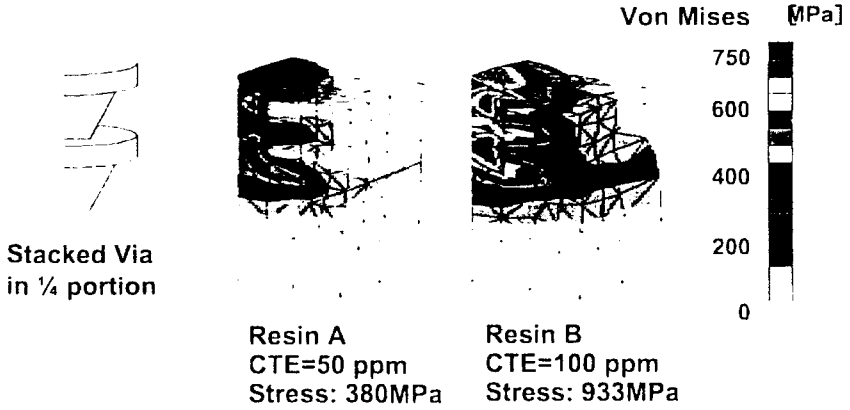


Variation of via fill uniformity



Stress distribution around stacked via with liner static analysis

» Large CTE material induces large stress around stacked via



Stress distribution analysis

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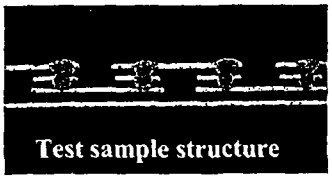
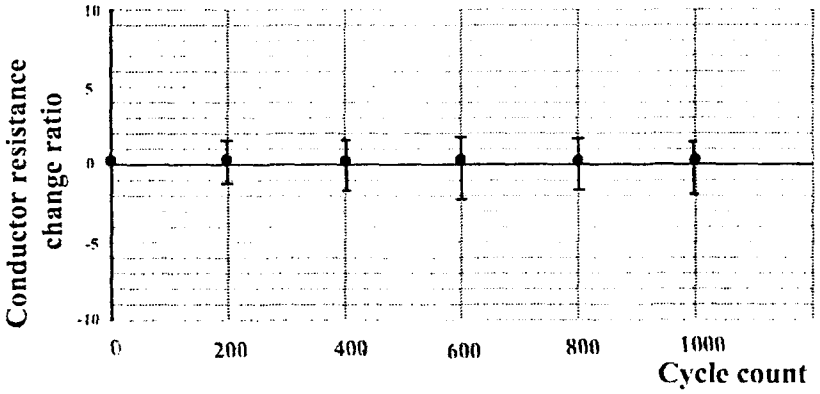
Stacked Vias Reliability

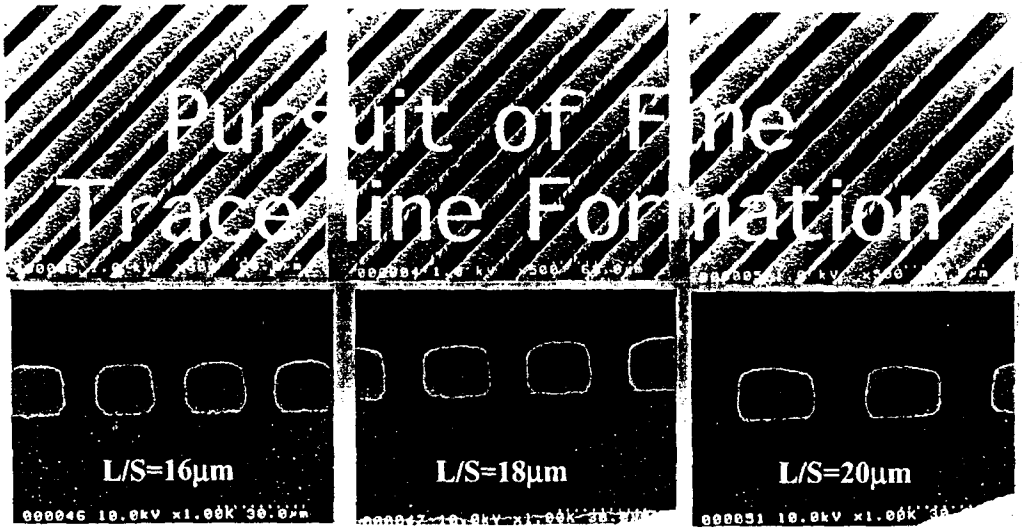


Test pattern: Via chain

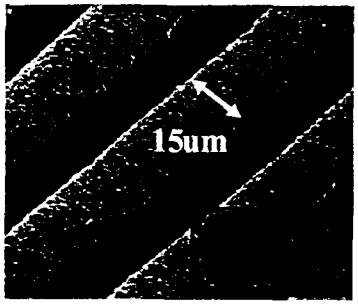
(Via count: 2000 vias)



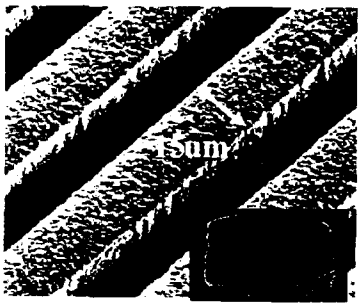
Conductor resistance change ratio in T/C (con. C) test



Fine lines formed
on extension of current using PWB facilities

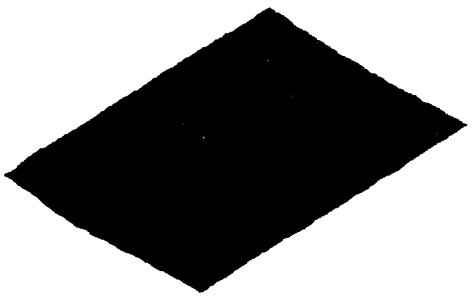


Smooth surface
Ra<0.5 μm

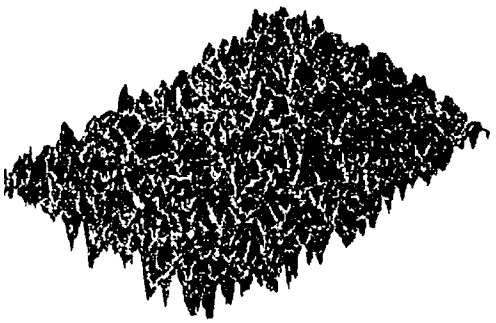


Rough surface
Ra=1~3 μm

Fine line Formation
Smooth Resin Surface Needed



Smooth surface
Modified PPE rsin
Ra<0.5 μm



Rough surface
Current used resin
Ra=1~3 μm

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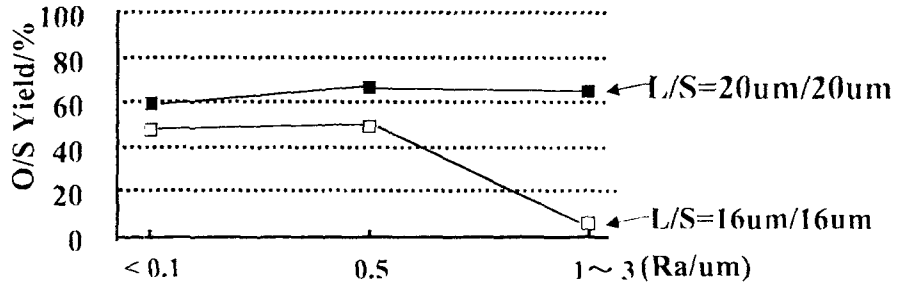
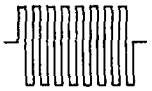
Relationship of Yield with Surface Roughness



Test sample: Comb pattern

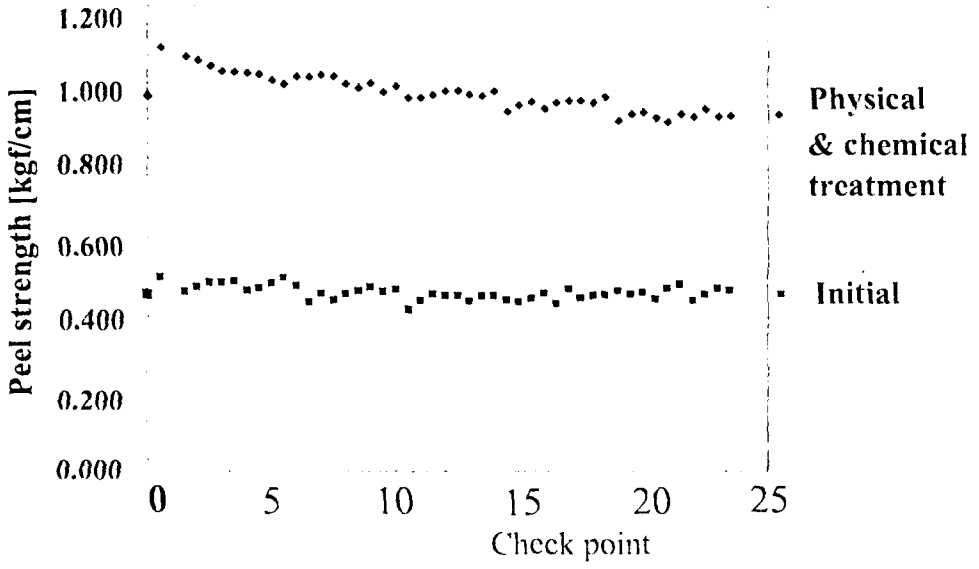


Major failures (Ra= 1～3 um , L/S=16/16um)

Peel Off

Seed Cu Residue

Peel Strength of PPE on Smooth plane



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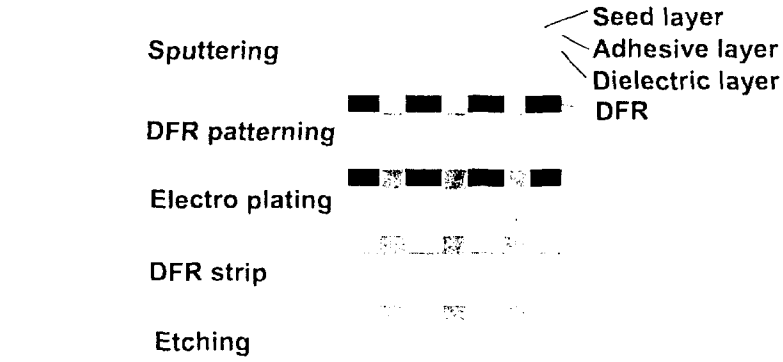
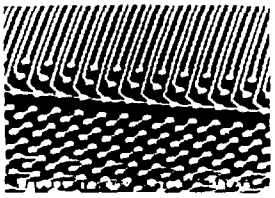
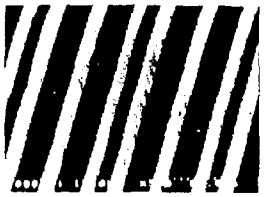
Fine line Patterning by Sputtering

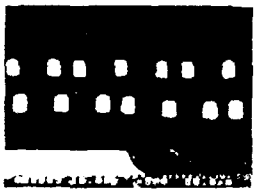




Top view
L/S=12/12um (min)

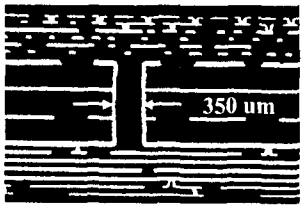


Top view
L/S=12/12um (min)

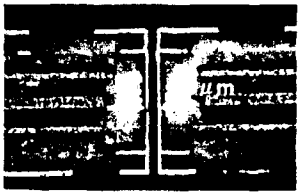


Crosse section
L/S=12/12um (min)

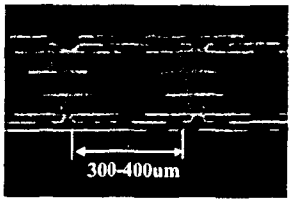
New Core Structure



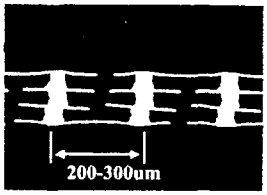
Glass cloth core (standard PKG)



Thin metal
Core



Fine TH Core
Filled with
Conductive paste



Finer TH Core
filled with
Electro plating

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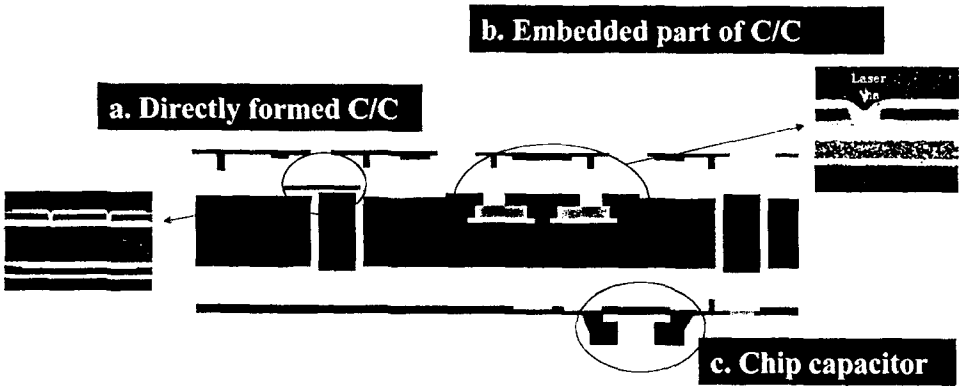
Embedded Capacitor



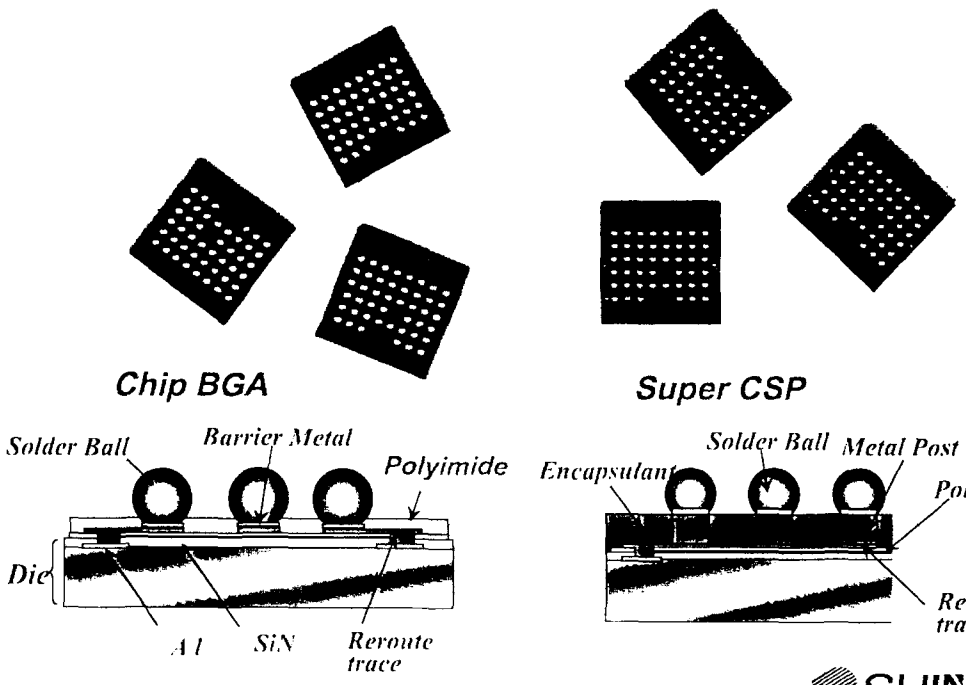
Capacitor types

Formation type	Technology node	Capacitance value	Process
Direct formation type	Coated polymers with high DK materials	Small	Screen printing
	Anodized metals	Middle	Sputtering and anodization
Embedded part type	Embedded part with high DK maerials	Large	Sputtering and embedding
	Embeded chip condensers	Large	Embedding

High DK Material	$Ba(Zr,Ti)O_3$	
	Ta_xO_y	
	SrTiO3	
Capacitor value	Small	several nF
	Middle	several decades nF
	Large	Few hundreds nF over

Super CSP

Structure



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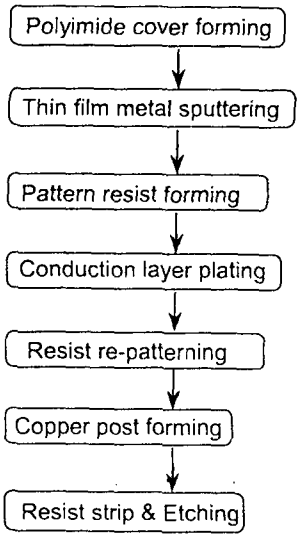
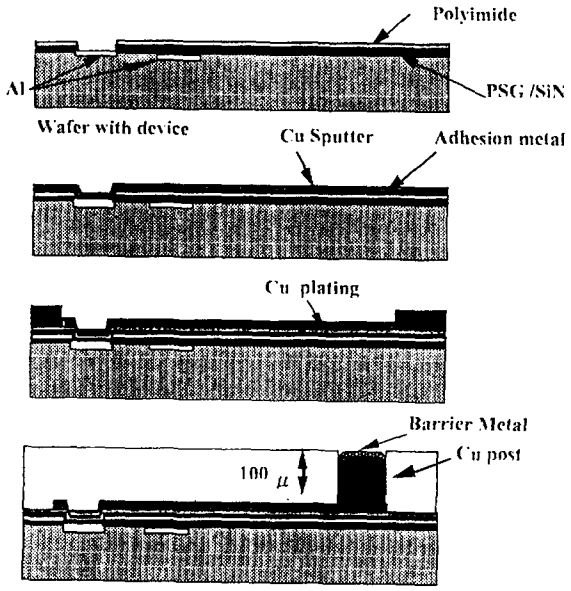
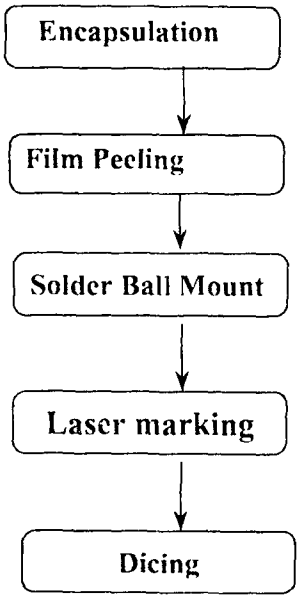
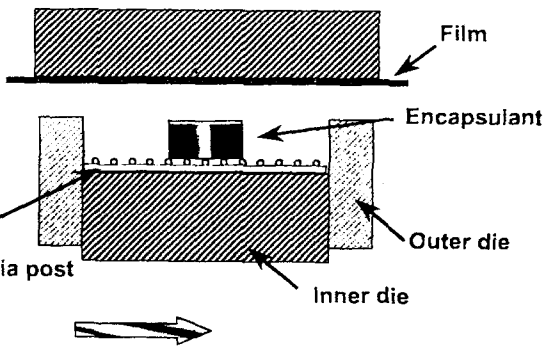
Fabrication Flow (1) Rerouteing & Forming Cu posts

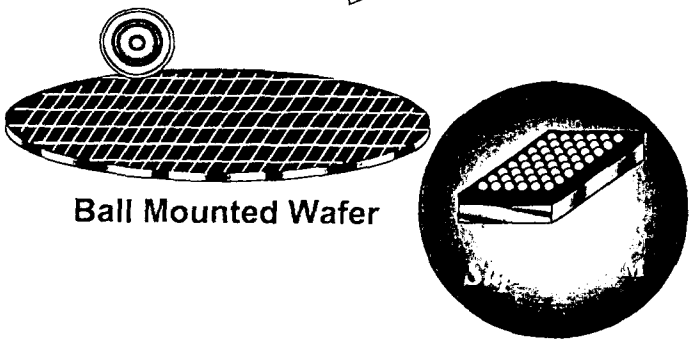




Fabrication Flow (2)







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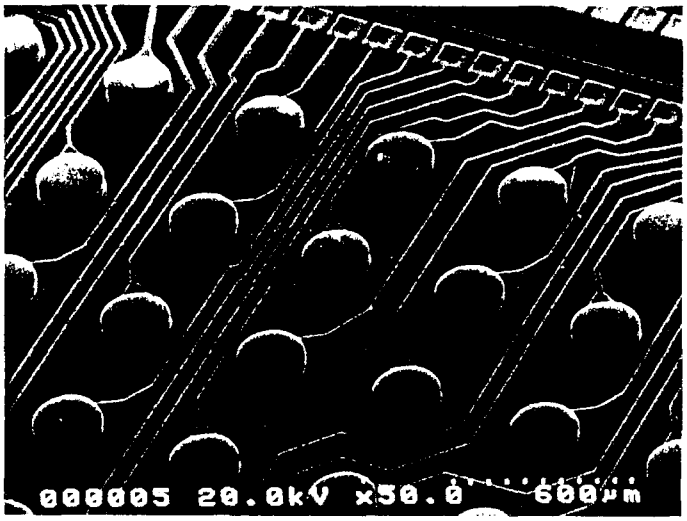
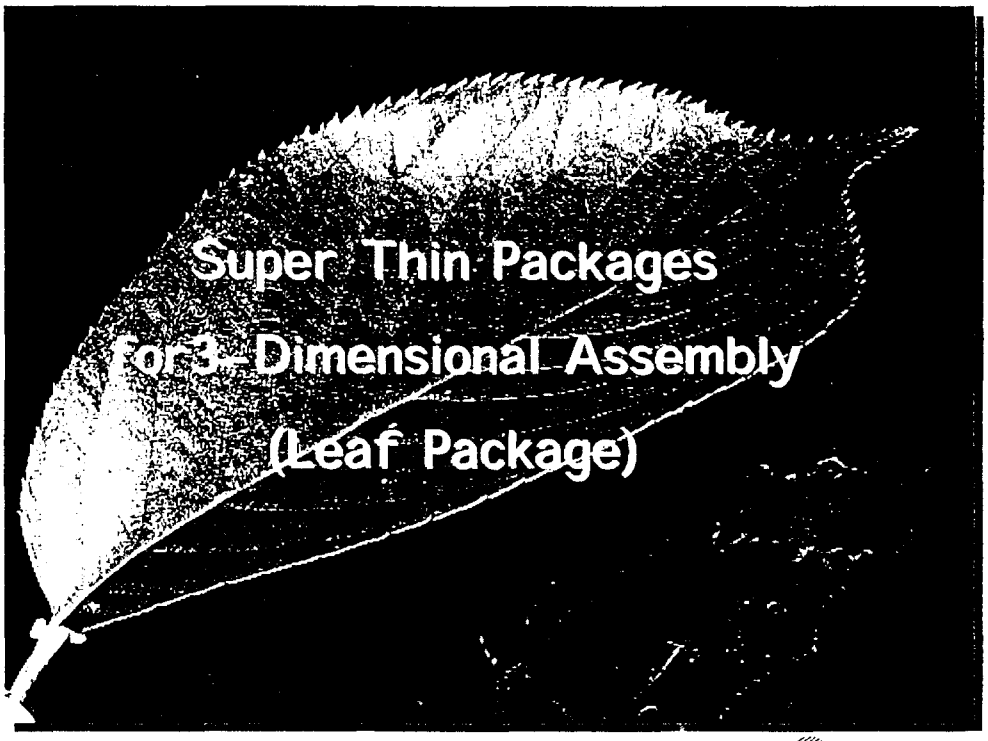
Rerouting Pattern on IC Chip



0.5mm pitch SHINKO TEST VEHICLE

CHIP SIZE 9mm sq Minimum L/S 20/20um



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Comparison of 3-D ass'y

Items / Level	Package level	Chip level	Wafer level
Feasibility	◎	○	△
System Speed	△	○	◎
Key point	Thin package Reduce the trace length	Fine pattern Generality	Fine pattern Generality Yield

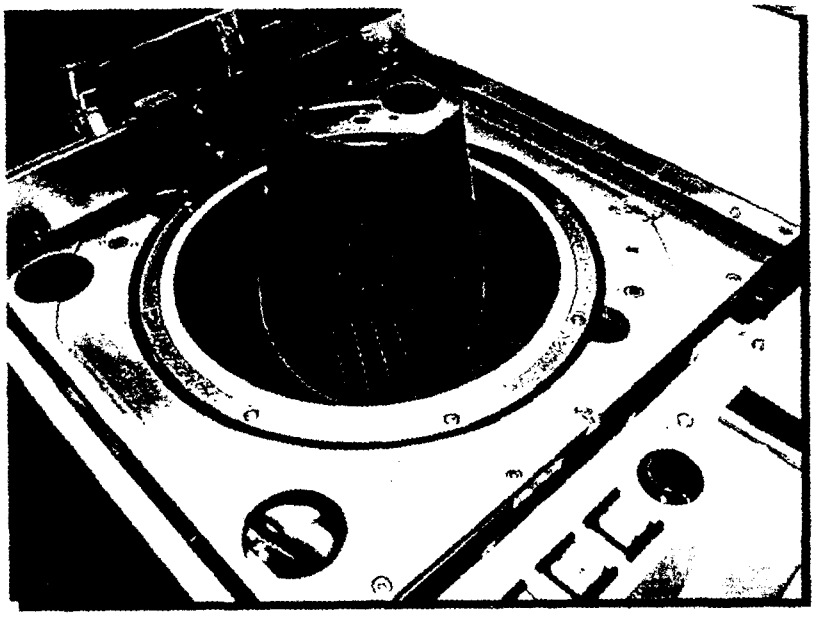
(Nikkei microdevices, Aug. 1999)

Current issue

Wafer thinning process

Handling process of the thinned Wafer

⇨ Warpage / Fragility



An example of the warped wafer (50 m in thick.)

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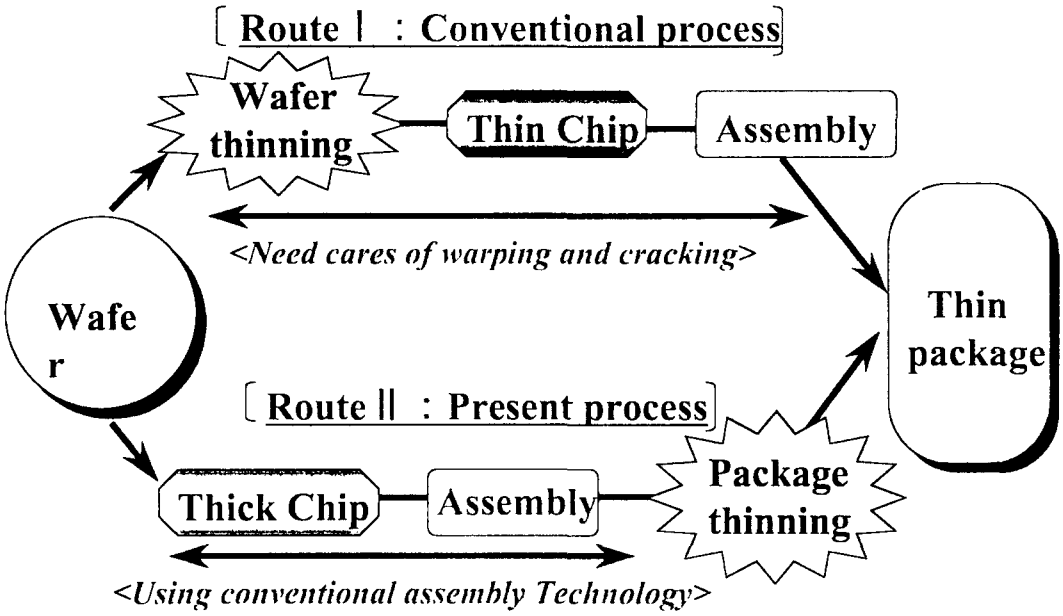
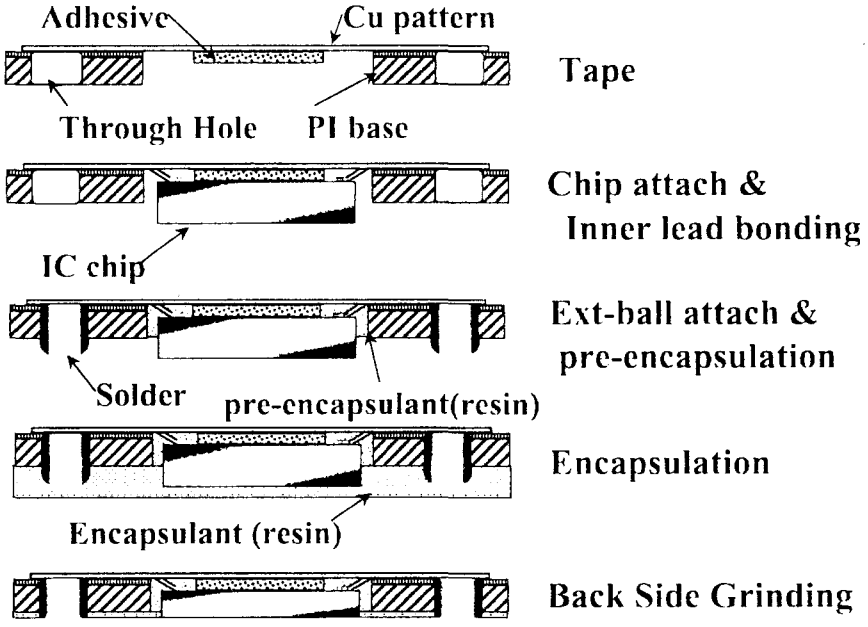
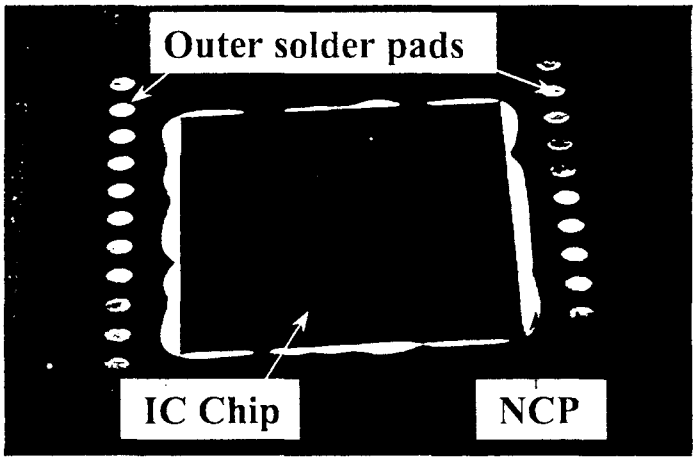
Route from Wafer to Thin package.



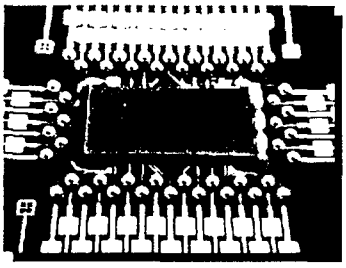
Process flow to assemble ILB type thin package.



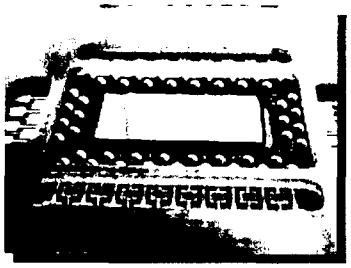


A view of ground and polished package.

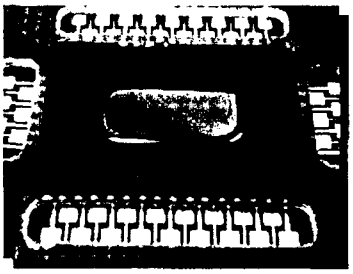
Appearance of product at each process



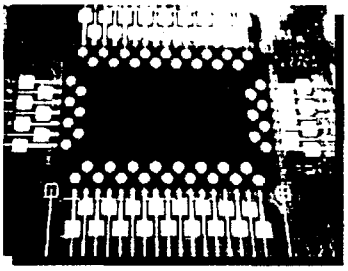
A: Solder balls mounted



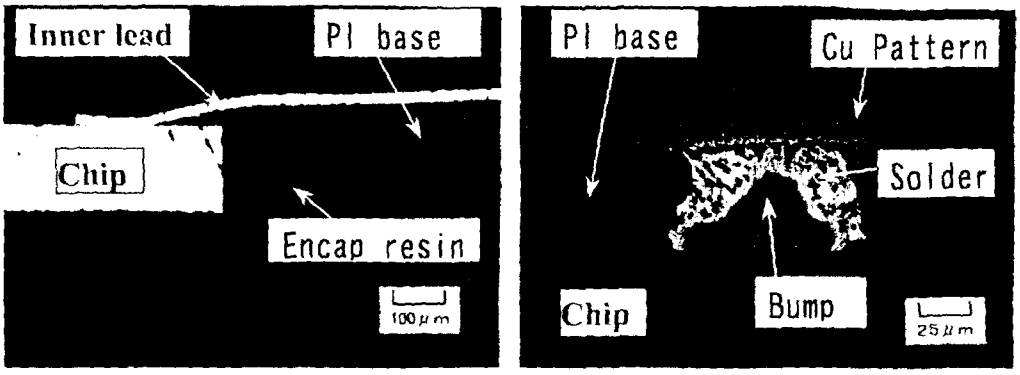
B: Frame for holding the encap. resin mounted.



C: As encapsulated

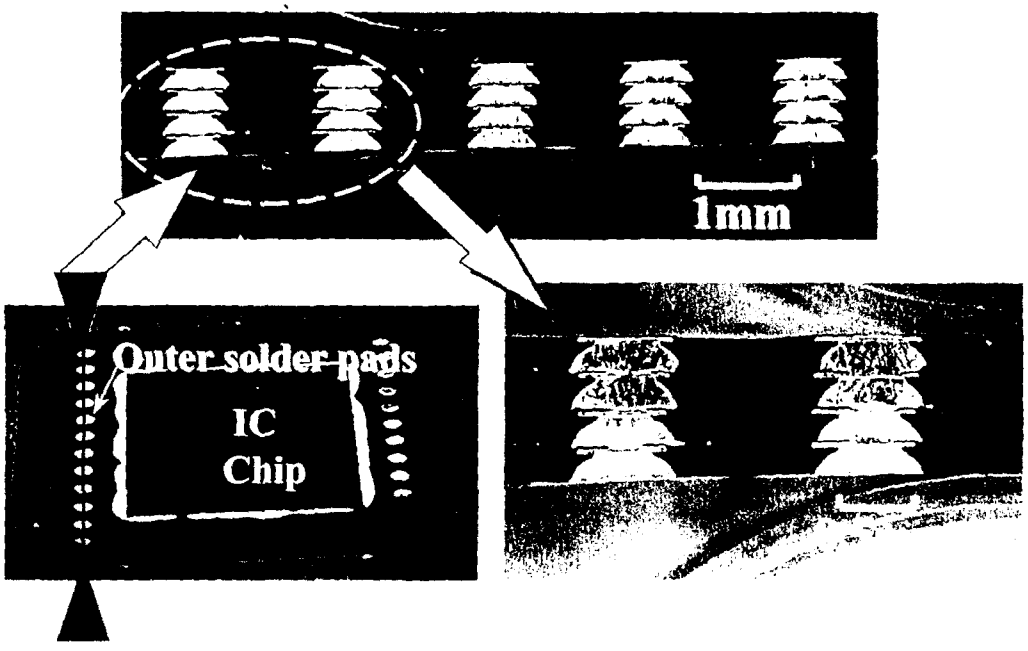


D: As backside ground



(a)ILB type (b)Bump type

The cross sections of the inner connection.



Cross sections of the stacked outer solder joints.

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Reliability of the single thin packages.

Test *	Sample	n	failed
TCT #	Thinned	34pcs	0/34
	Before thinning	12pcs	2/12
PCT $	Thinned	20pcs	0/20
	Before thinning	12pcs	0/12

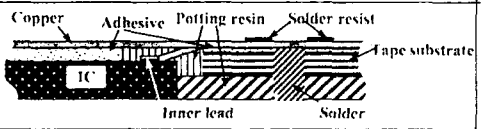
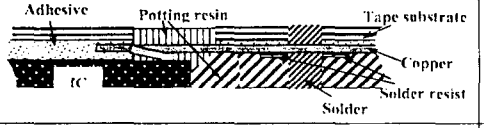
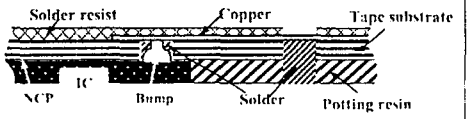
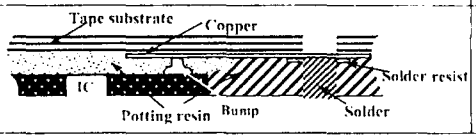
* : Pre-con level_3 (J-STS-020A)

125℃ 24h bake+ 30℃ 60% 192h + IR reflow 235℃ 3 times

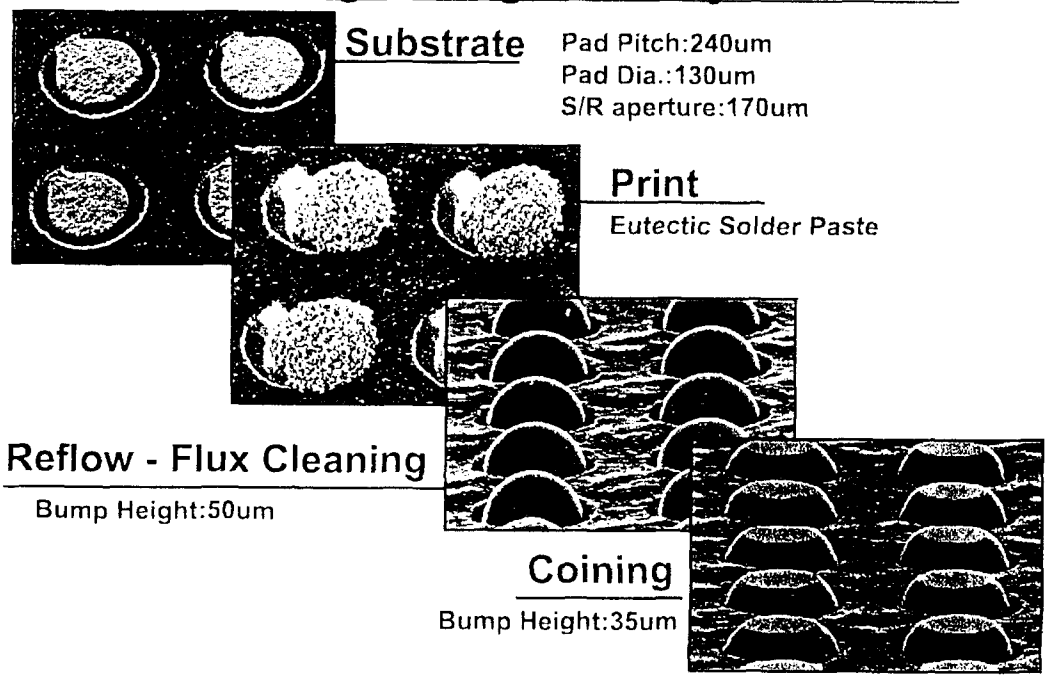
:Thermal cycle test : -55℃~+125℃ 1,000cycles

$:Pressure cuka test :121℃, 2 atms 100% 336h

Structures of the thin package.

No.	Cross sections of the thin packages	Routing	Inter connection
1		Circuit-out Fan-out	ILB
2		Circuit-in Fan-out	ILB
3		Circuit-out Fan-out	Bump
4		Circuit-in Fan-out	Bump

Presoldering for High Density Substrate



Substrate

Pad Pitch:240um
Pad Dia.:130um
S/R aperture:170um

Print

Eutectic Solder Paste

Reflow - Flux Cleaning

Bump Height:50um

Coining

Bump Height:35um

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Variation of Bump High

Eutectic Solder

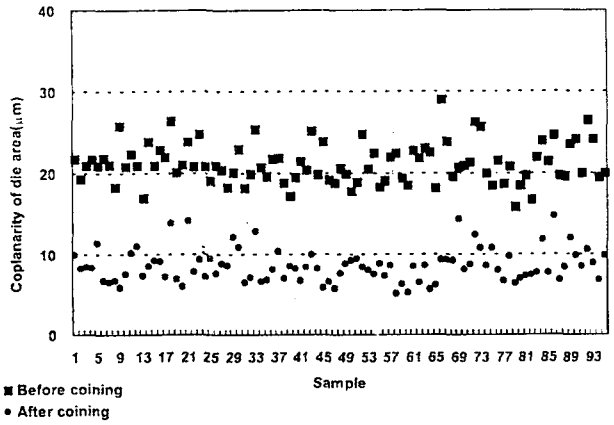

Fig.1 Coplanarity of die area after coining

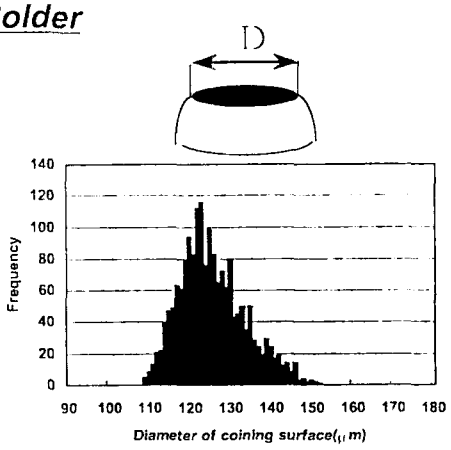

Fig.2 Diameter of coining surface

Presoldering for Lead Free

Solder	Tm[degC]	Reflow conditions [degC]	Feasibility
Sn-Ag(3.5)	221	255peak,220over30sec.	OK
Sn-Ag(3.5)-Cu(0.75)	217-219	255peak,220over30sec.	OK
Sn-Ag(2.5)-Cu(0.5)-Bi(1.0)		250peak,230over30sec.	on Development
Sn-Zn(7.8)-Bi(3.0)	187-197		on Development
Sn(63)-Pb(37)	183	230peak,183over40sec.	OK

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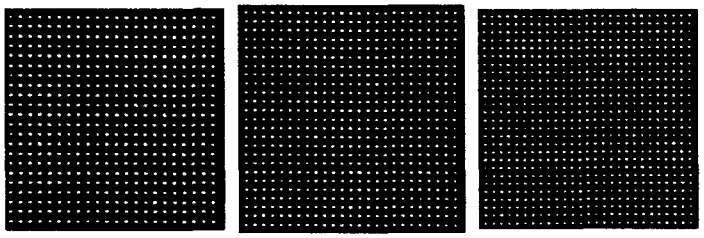
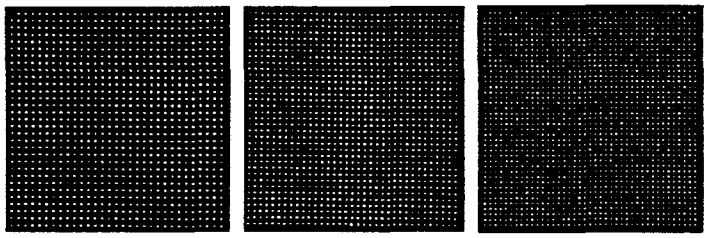
Pre Solder : Pre Solder Printing



For Volume Production

Pad Pitch	220 um	200 um	180 um
Pad Diameter	110 um	100 um	90 um



Just Evaluation Sample

Pad Pitch	160 um	140 um	120 um
Pad Diameter	80 um	70 um	60 um

conclusion

1. New technologies for future build-up packages were demonstrated.
   Fine line formation feasibility, Stacked vias and other key technologies were discussed.

2. Pre-soldering for flip chip attachment was demonstrated to 150 um pitch using screen printing.

3. CSPs with fine line patterns were demonstrated and the microfabrication technologies used for their manufacturing were also presented.

4. 3-D packages and their manufacturing process were investigated, and the availability of future 3-D modules is expectable.

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