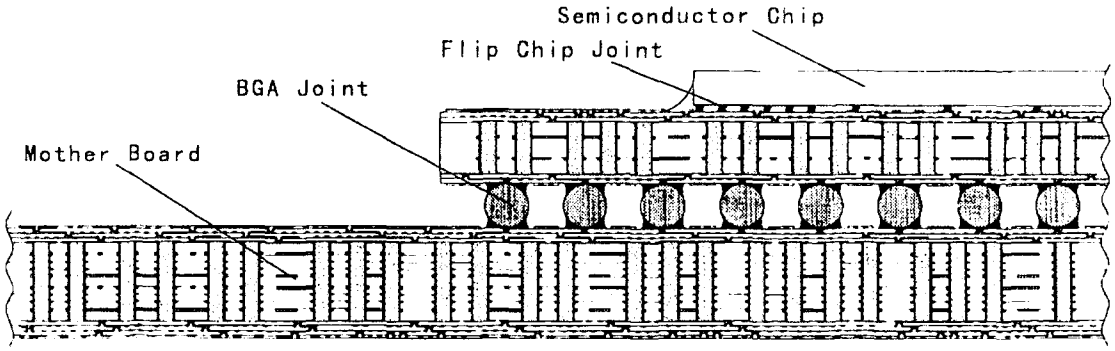
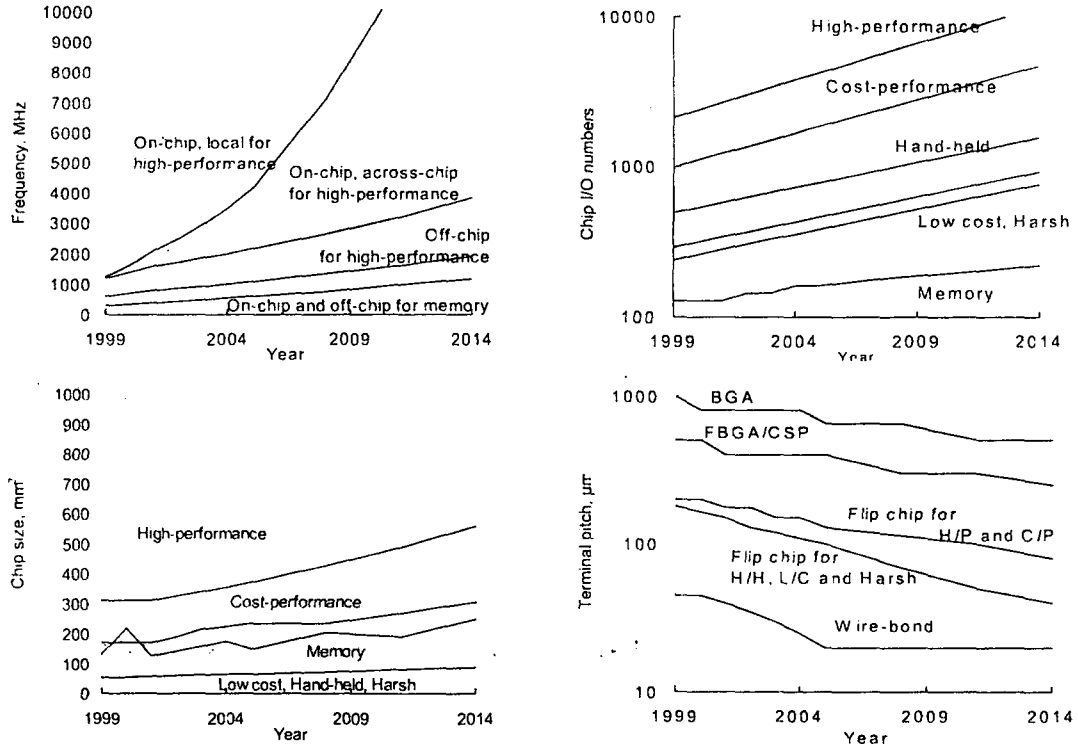
DESIGN AND MANUFACTURING FACTORS OF MICRO-VIA SUBSTRATE TECHNOLOGIES

By Yutaka Tsukada

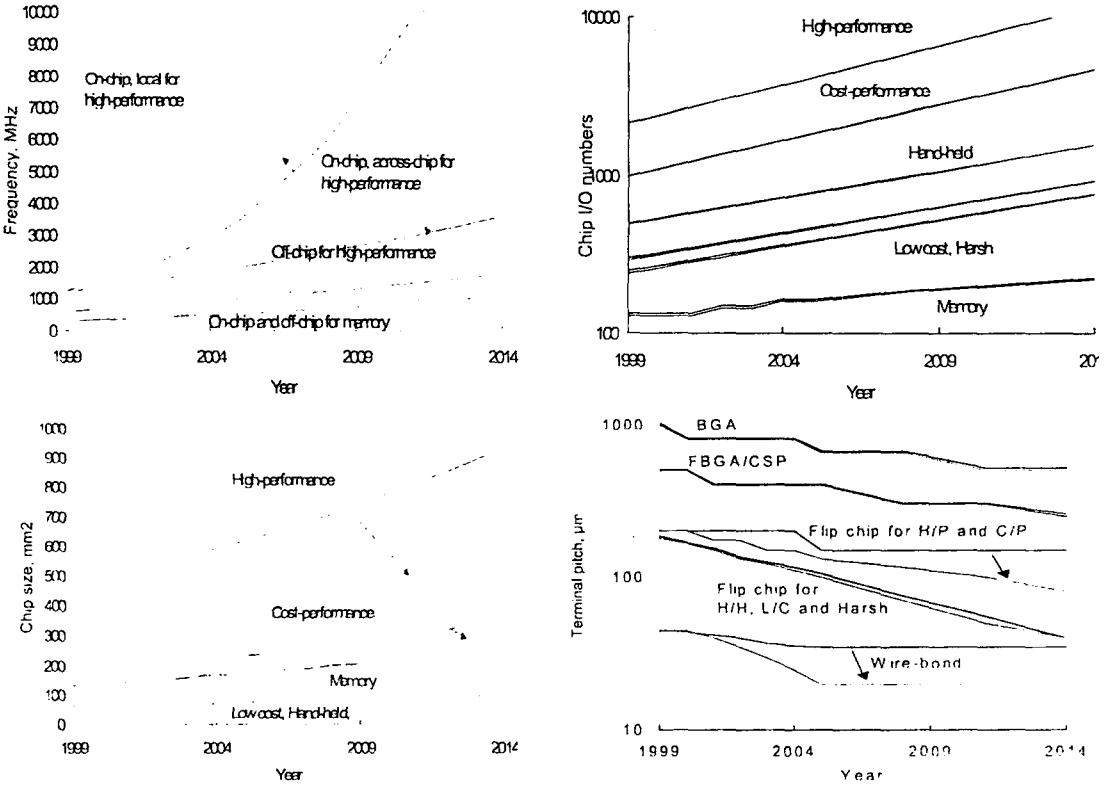
Yasu Technology Application Laboratory, IBM Japan Ltd.
800 Ichimiyake, Yasu-cho, Yasu-gun, Shiga-ken, Japan 520-2392
Phone: 81-77-587-8601, Fax: 81-77-587-8609, E-mail: tsukaday@gold.ocn.ne.jp



Cross section of Flip chip BGA package

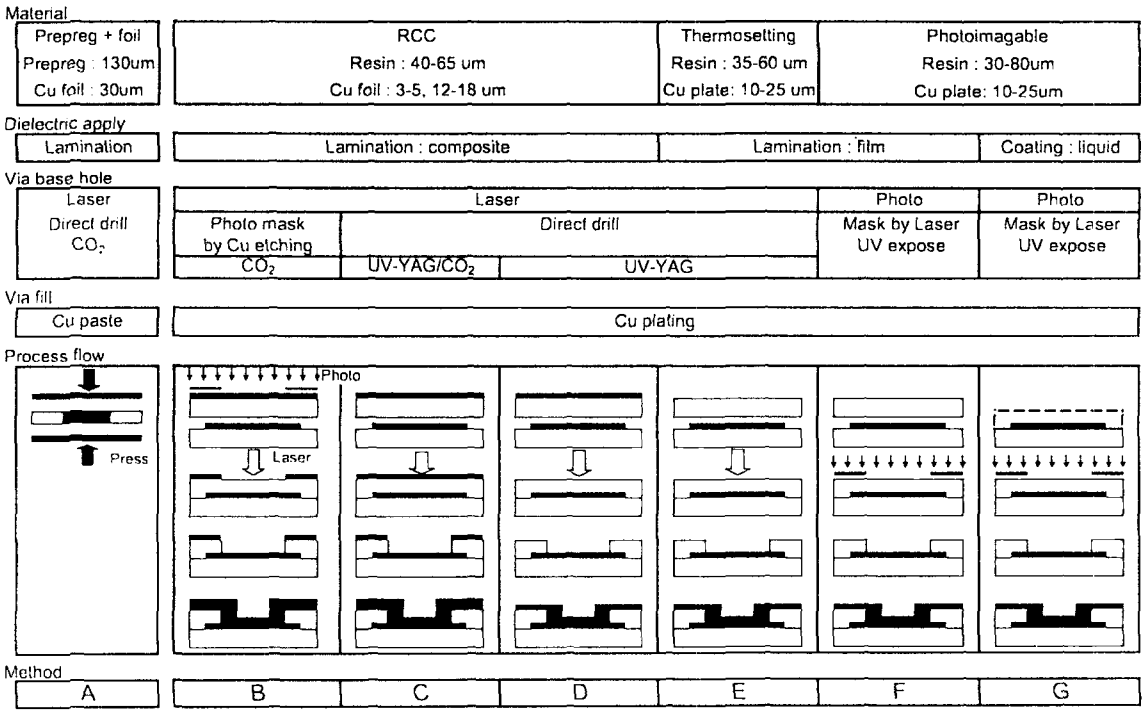


Requirement from semiconductor

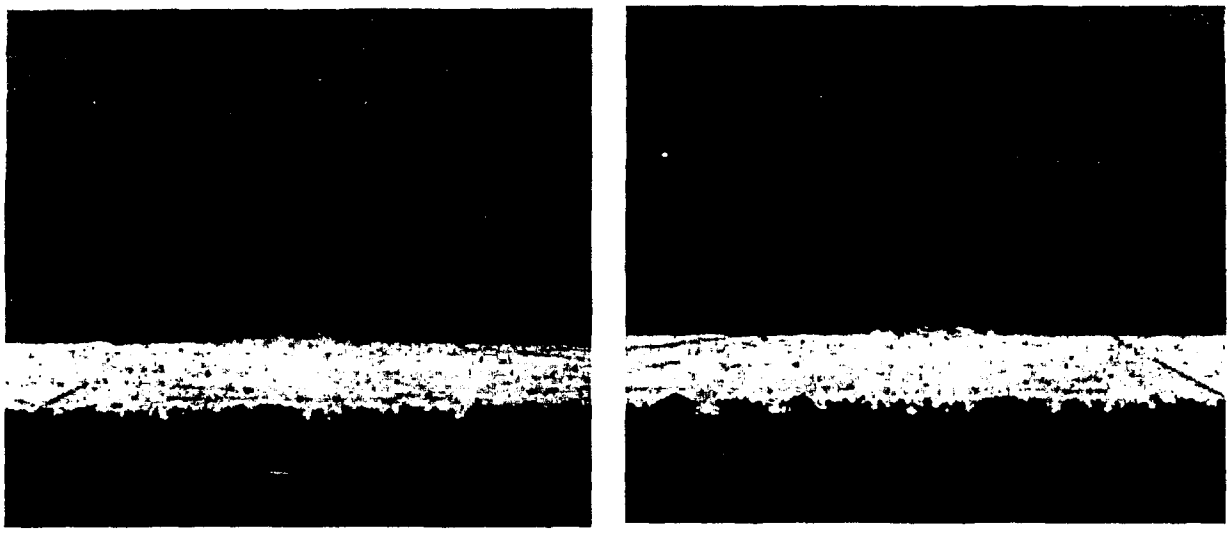


Flip chip fanout requirement

Parameter	2001	2002	2003	2004	2005	2008	2011
Flip chip pad pitch (μm)	175	175	150	150	130	115	100
Pad size (μm)	88	88	75	75	65	58	50
Chip size (mm/side)							
Cost-performance	13	14	15	15	15	15	16
High-performance	18	18	18	19	19	21	22
Array size = #pads along chip edge							
Cost-performance(maximum)	75	79	98	100	118	133	164
Cost-performance(needed)	35	37	39	41	43	50	59
High-performance(maximum)	101	103	123	126	148	180	221
High-performance(needed)	52	55	58	61	65	77	91
Number of outer rows accesses (to determine number of fan-out layers needed)							
Cost-performance	5	5	4	5	5	5	6
High-performance	8	8	8	8	8	9	10
Effective total wiring density for fan-out need (cm/cm2)							
Cost-performance	286	286	267	333	385	435	600
High-performance	457	457	533	533	615	783	1000
Wiring substrate(Three or more lines for one depopulated pad - accessing 2 or more rows per layer)							
Line width (μm)	29.2	29.2	32.1	25.0	21.7	19.2	13.6
Line spacing (μm)	29.2	29.2	32.1	25.0	21.7	19.2	13.6
Wiring substrate(Six or more lines for one depopulated pad - accessing 3 or more rows per layer)							
Line width (μm)	17.5	17.5	15.0	15.0	13.0	10.1	7.9
Line spacing (μm)	17.5	17.5	15.0	15.0	13.0	10.1	7.9



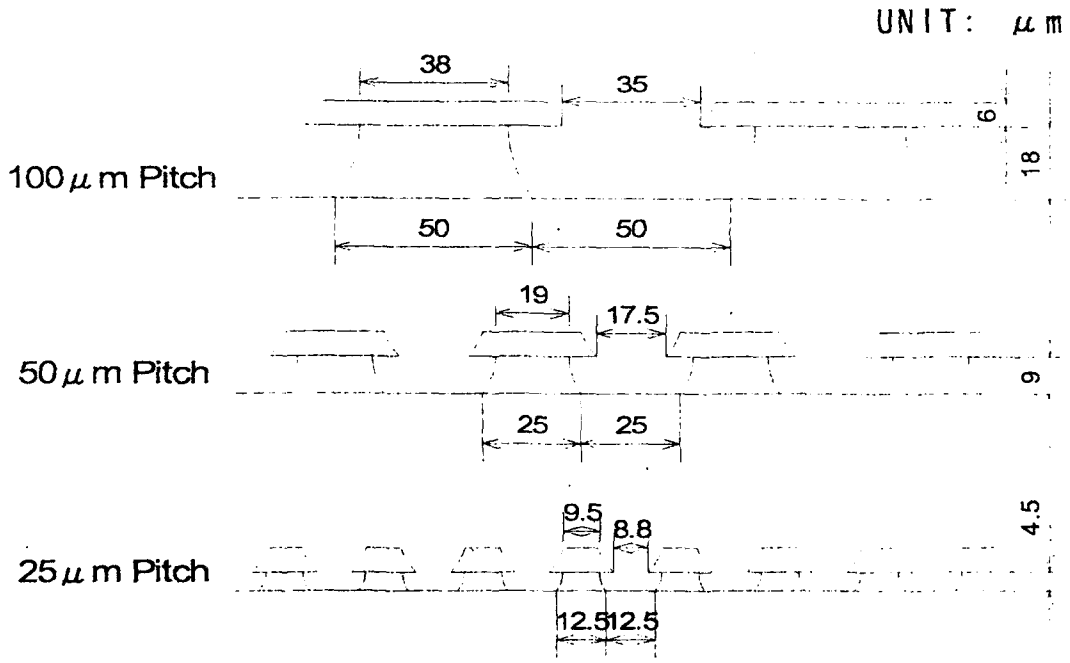
Buildup structure variations



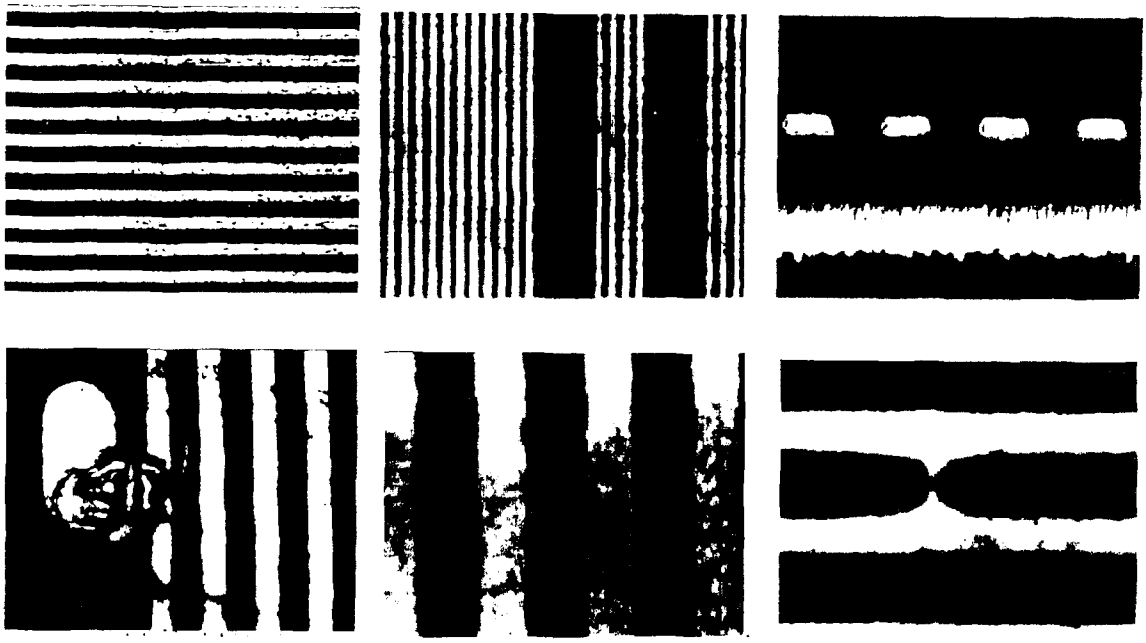
43 μm dia.

48 μm dia.

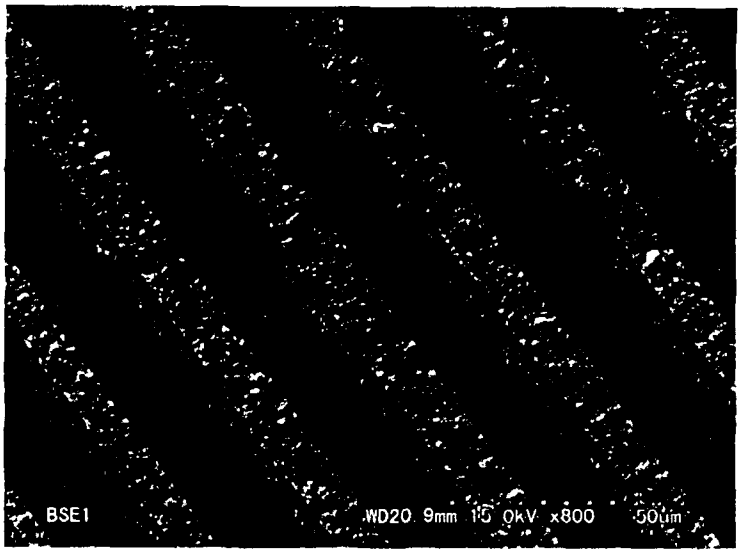
Via hole made by laser drilling



Subtractive etching geometry



Subtractive 50micron pitch lines



30 μm pitch line by pattern plating

$$Z_c = \frac{377}{E_r} \cdot \frac{H}{W_{eff}} \cdot \frac{1}{2+2.8\,(H/W_{eff})^{3/4}}$$

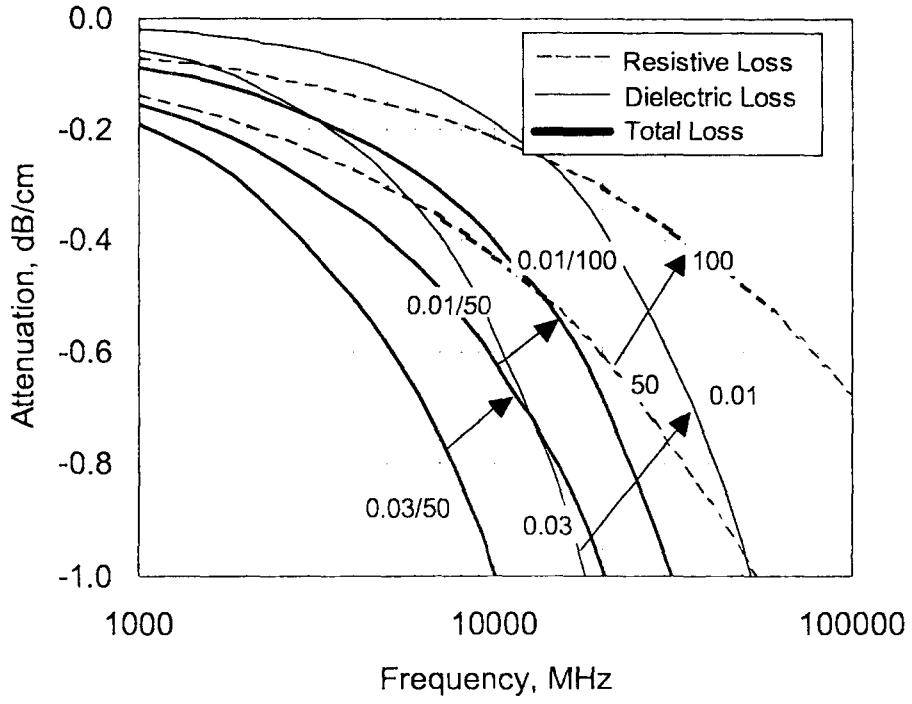
where Z_0: characteristics impedance, Ω

Er: dielectric constant

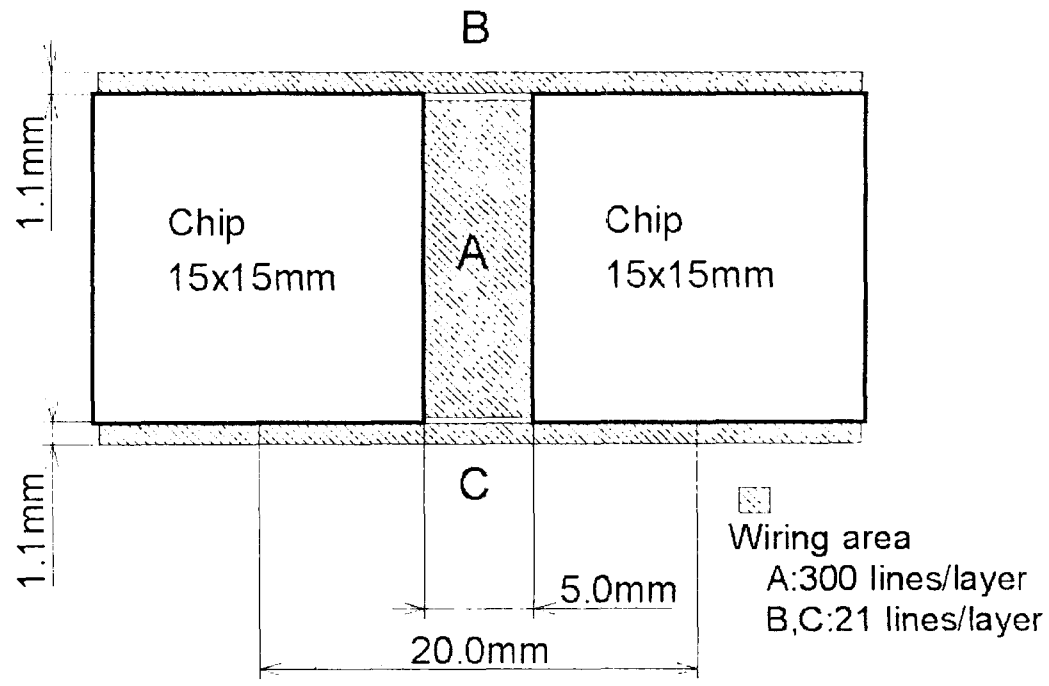
H: height between conductors, μm

W_{eff}: effective width of line, μm

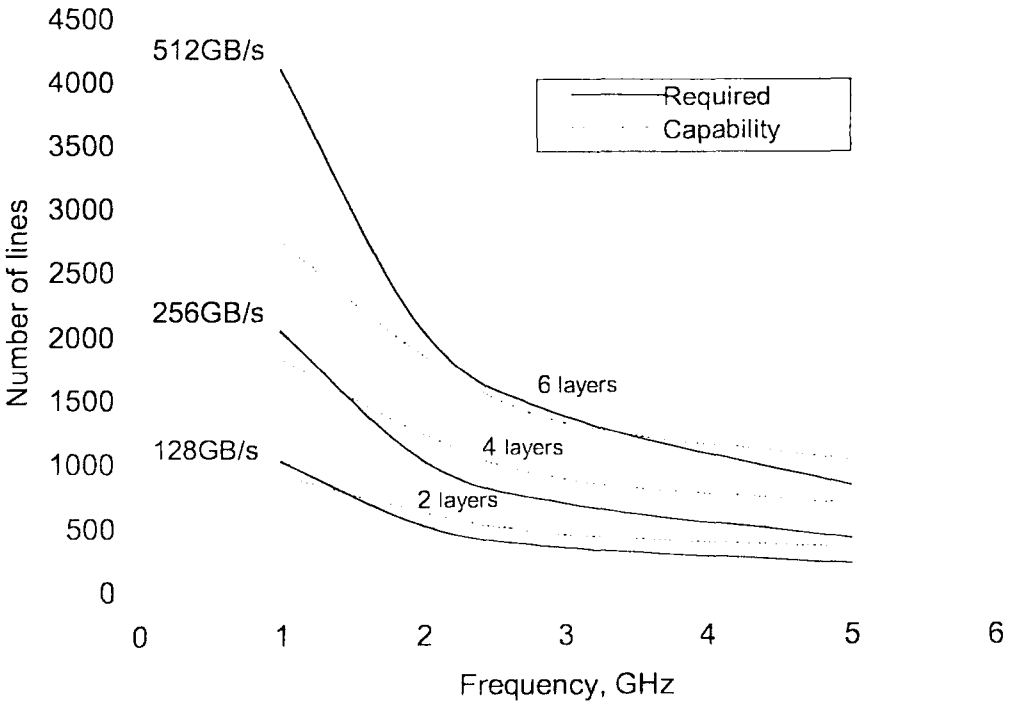
Structure geometry relation



High speed signal capability



High density chip to chip wiring



Required build-up layers for high band signal

SUMMARY

1- Buildup PCB technology is utilized to a bare chip attach substrate technology for packaging of semiconductor chip

2- Requirement for the substrate design rule is described in SIA International Technology Roadmap for Semiconductor.

3- There are seven fabrication methods of build-up technology.

4- Coating and lamination for resin and photo, and laser for micro via hole processes are available. Below 50μm in diameter is possible.

5- Fine pitch lines down to 30 μm can be achieved by pattern plating with better electrical property.

6- Dielectric loss reduction is a key material improvement item for next generation build-up technology.

7- High band width up to 512 GB/s is possible with current wiring groundrule.