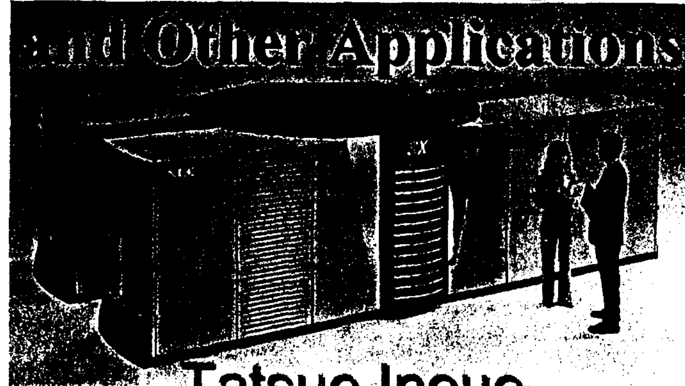
LSI Packaging Technologies for High-End Computers and Other Applications

Tatsuo Inoue

September 13, 2001
3rd Korea-Japan Advanced Semiconductor packaging Technology Seminar

LSI Packaging Technologies for High-End Computers



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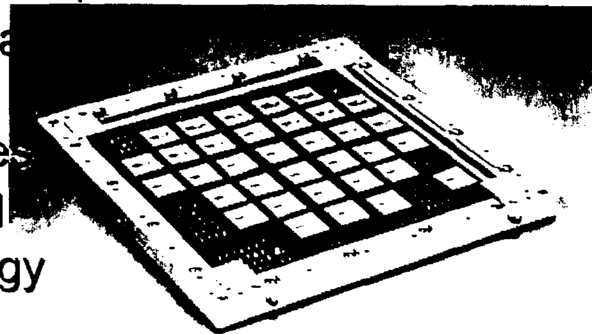
6. Summary



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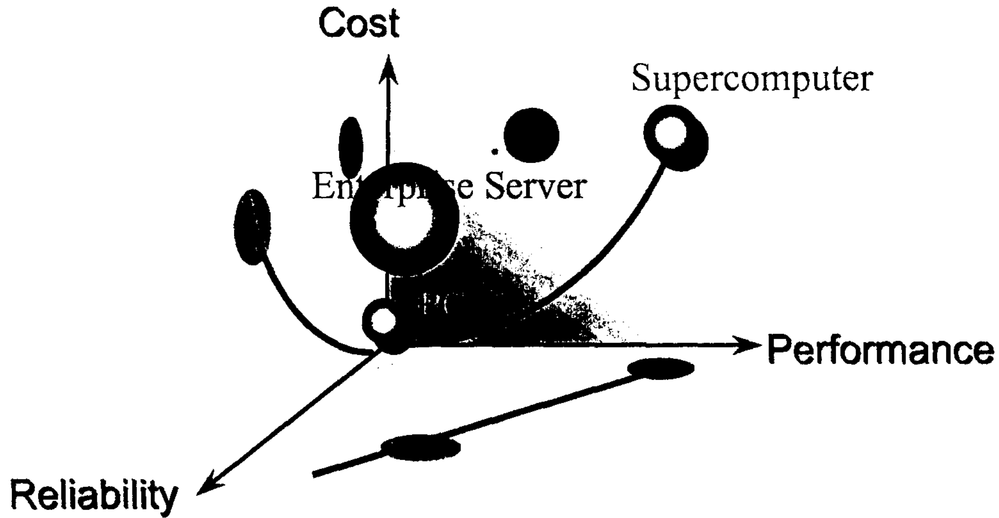
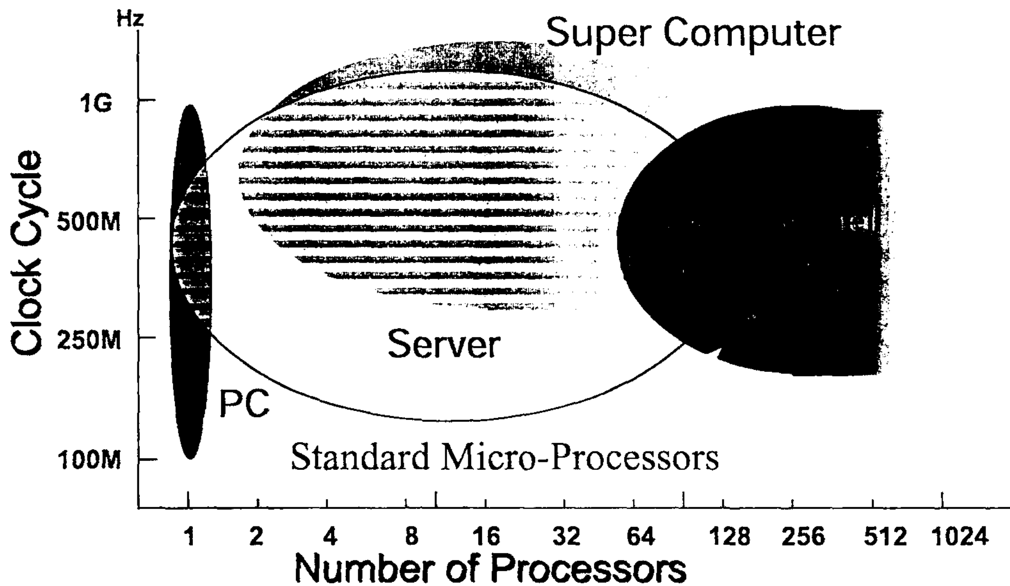
1. Introduction to High-End Computers

■ **Positioning Categorized Computers in Tree Dimensional Space of Cost, Performance and Reliability**



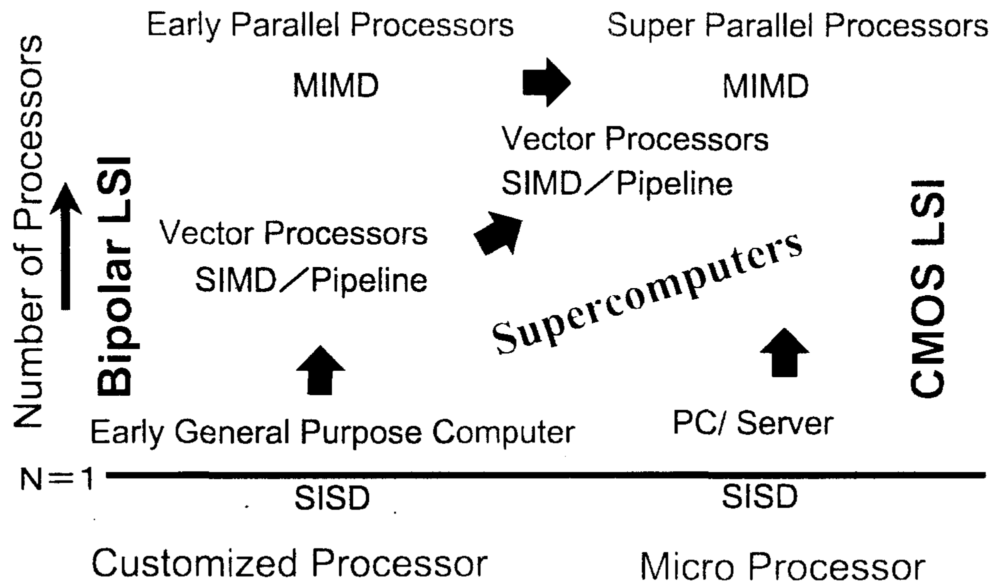
1. Introduction to High-End Computers

■ **Comparison between Categorized Computers in Clock Cycle and Number of Processors**



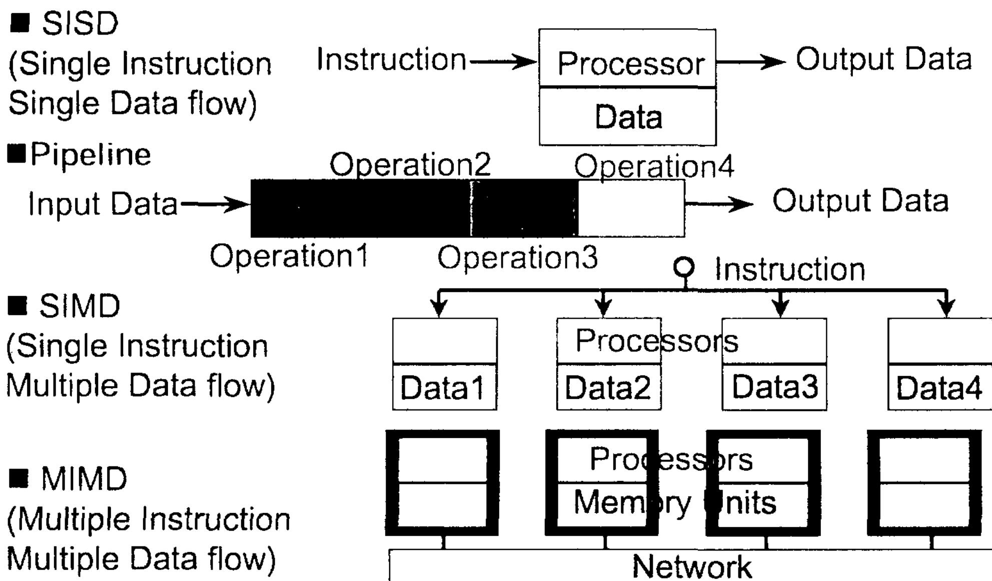
1. Introduction to High-End Computers

■ Comparison between Categorized Computers in Instruction Flow and Data Flow



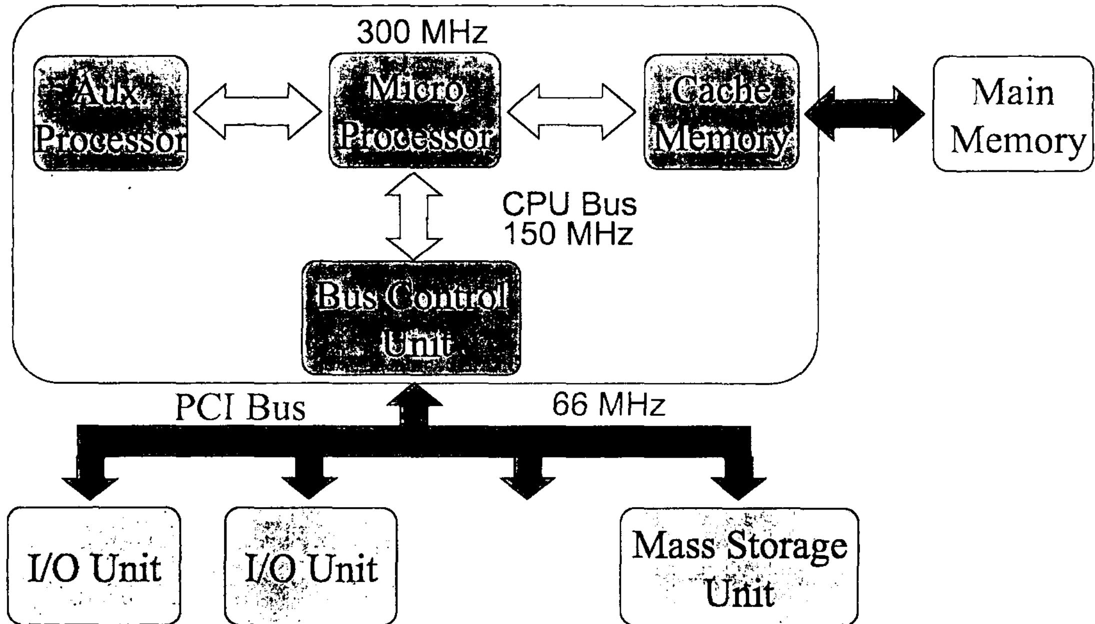
1. Introduction to High-End Computers

■ Categorizing Computers in Instruction Flow and Data Flow



1. Introduction to High-End Computers

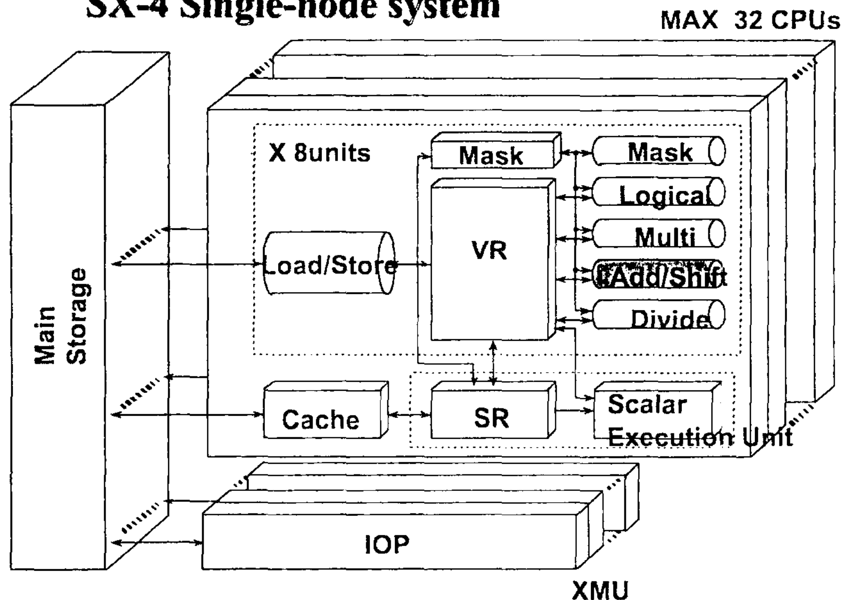
■ Architecture of Personal Computer



1. Introduction to High-End Computers

■ Architecture of Vector Supercomputer

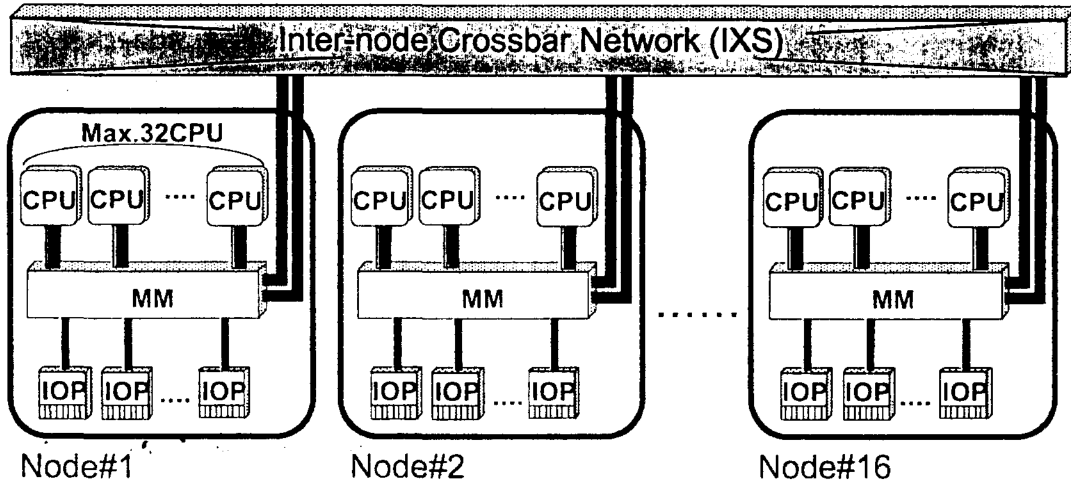
SX-4 Single-node system



1. Introduction to High-End Computers

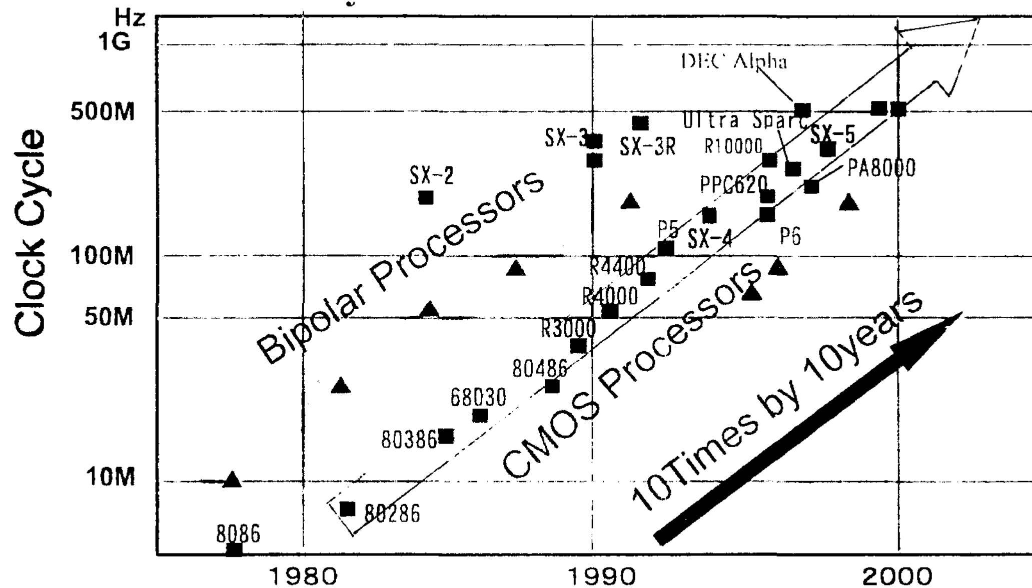
■ **Architecture of Vector Supercomputer**

SX-4 Multiple-node system



2. Trend of LSI Packaging Technology for High-End Computers

■ **Trend of Clock Cycle in Interconnection of Processors**



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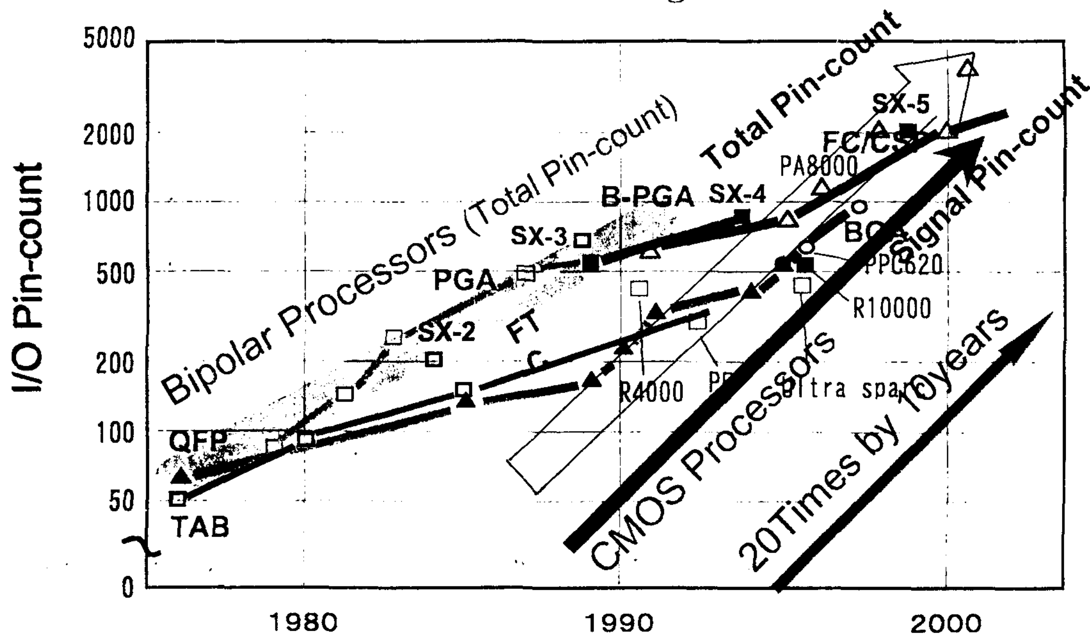
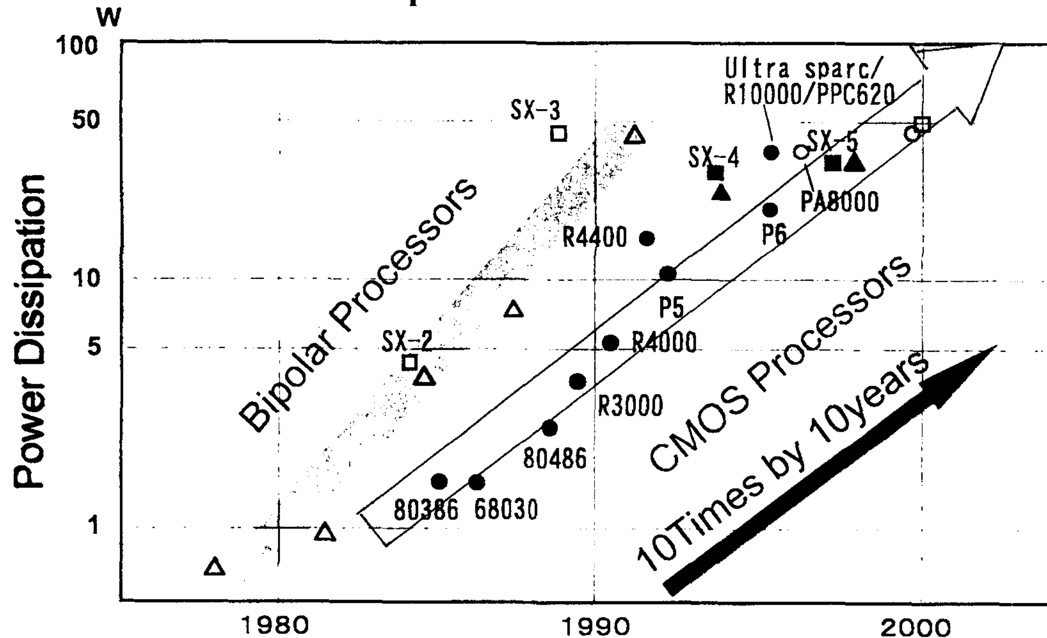
2. Trend of LSI Packaging Technology for High-End Computers

■ Trend of I/O Pin-count in LSI Package for Processors



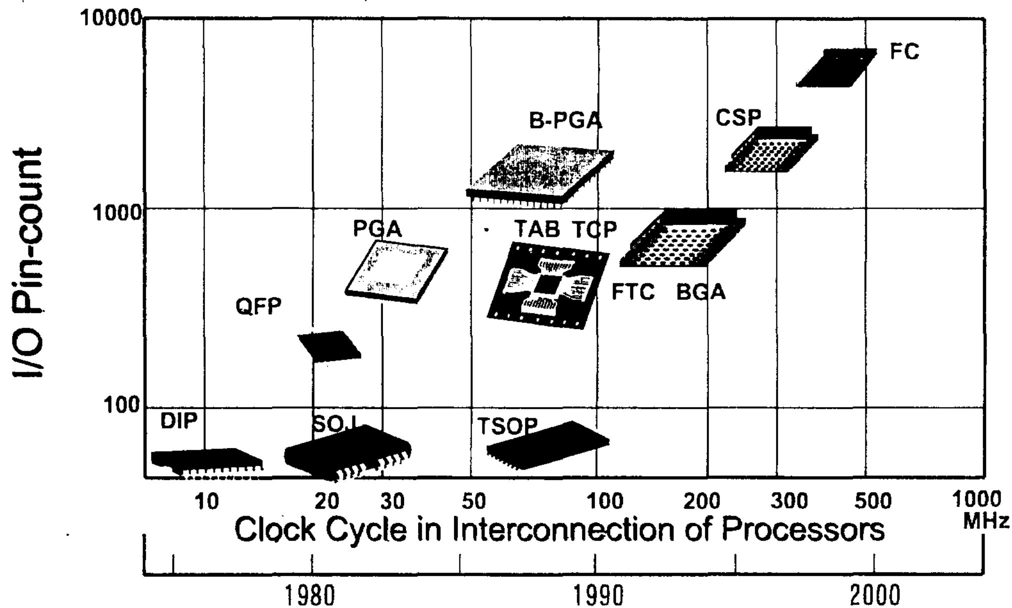
2. Trend of LSI Packaging Technology for High-End Computers

■ Trend of Power Dissipation in LSI Processors



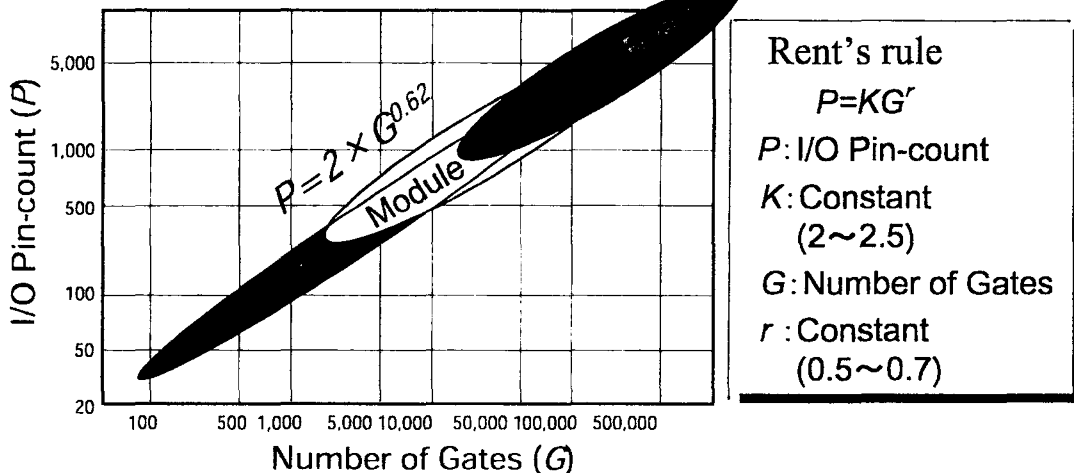
2. Trend of LSI Packaging Technology for High-End Computers

■ **Trend of LSI Package for Processors**



2. Trend of LSI Packaging Technology for High-End Computers

■ **"Rent's Rule, A Study in Relation between Scale of Integration and I/O Pin-count**



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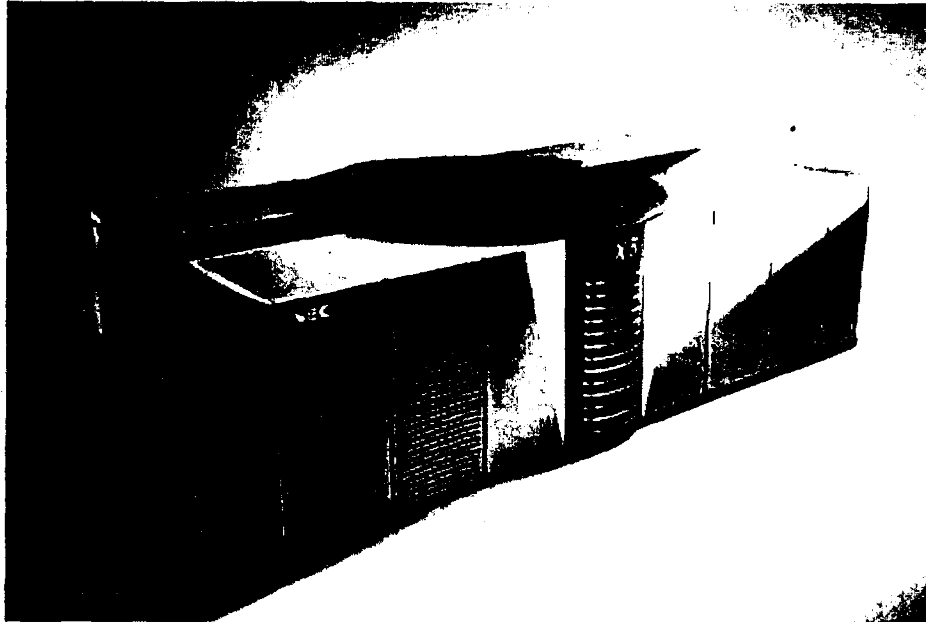
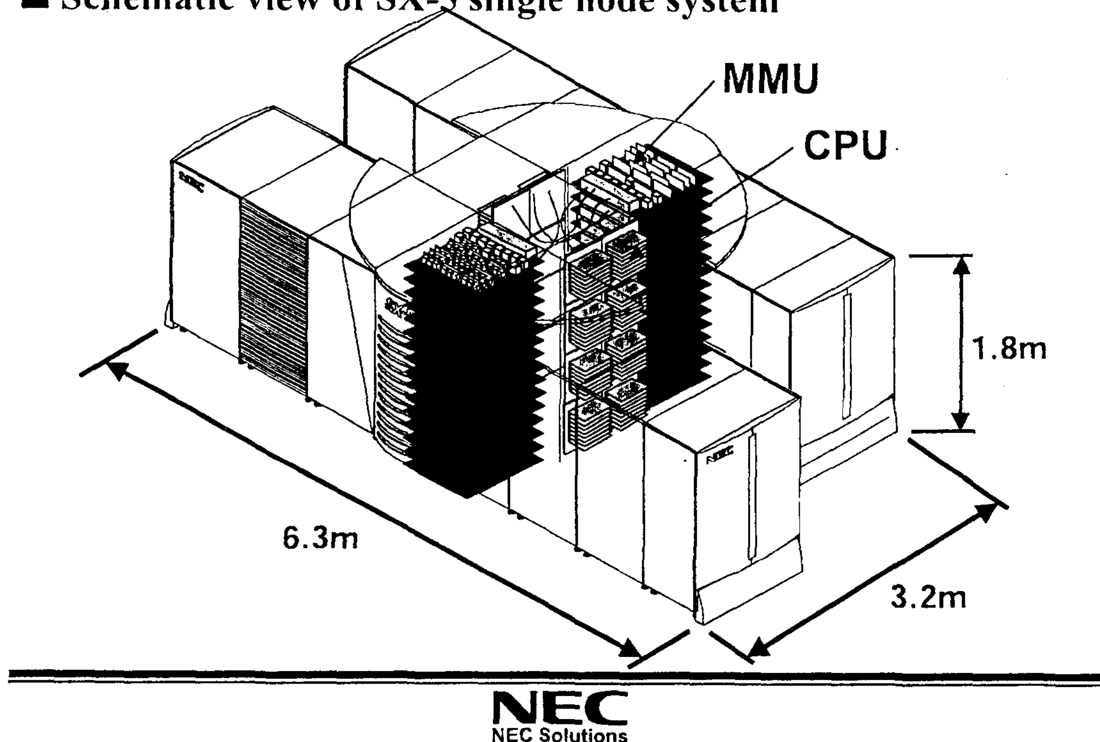
3. LSI Packaging Technologies in NEC's High-End Computers



3. LSI Packaging Technologies in NEC's High-End Computers

■ Schematic view of SX-5 single node system



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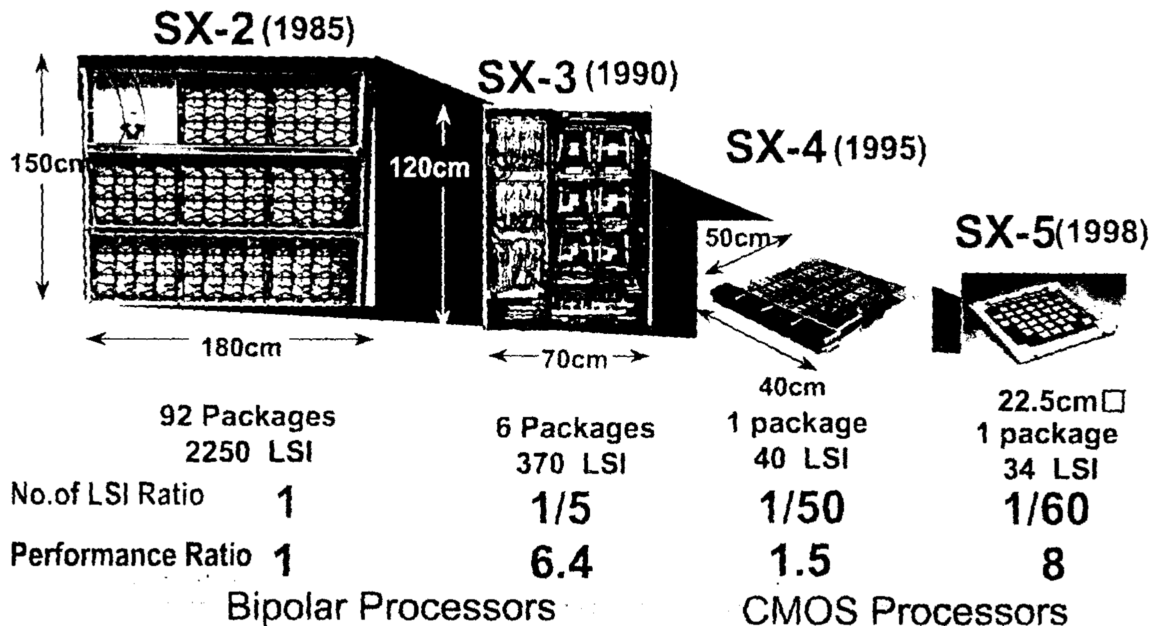
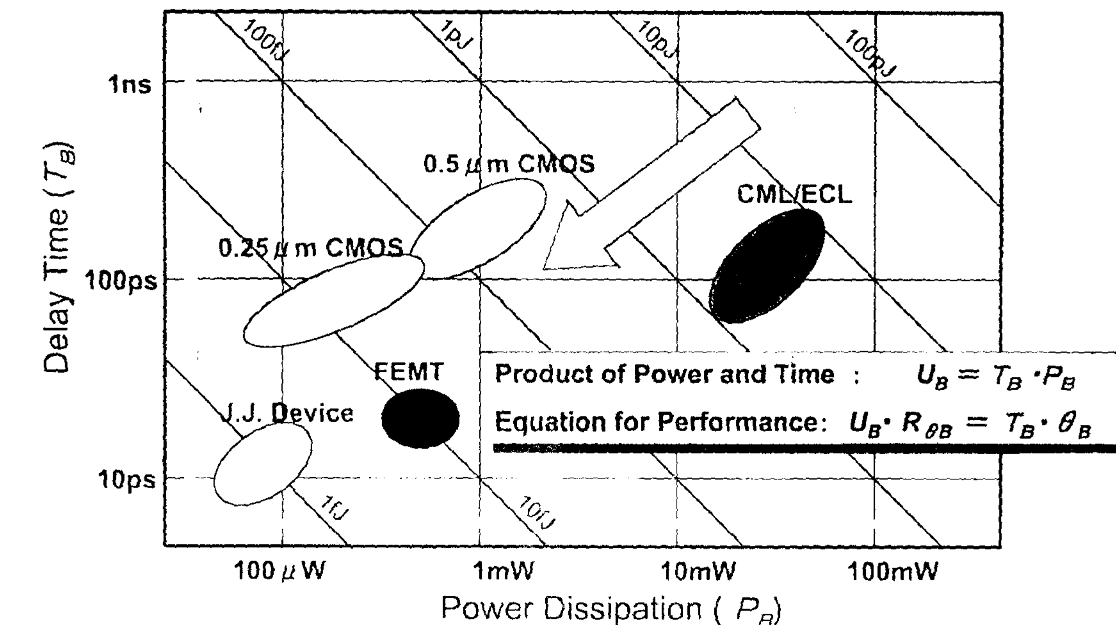
3. LSI Packaging Technologies in NEC's High-End Computers

■ Transition in Technology for NEC's Supercomputers



3. LSI Packaging Technologies in NEC's High-End Computers

■ Comparison in Power and Delay of Switching Devices



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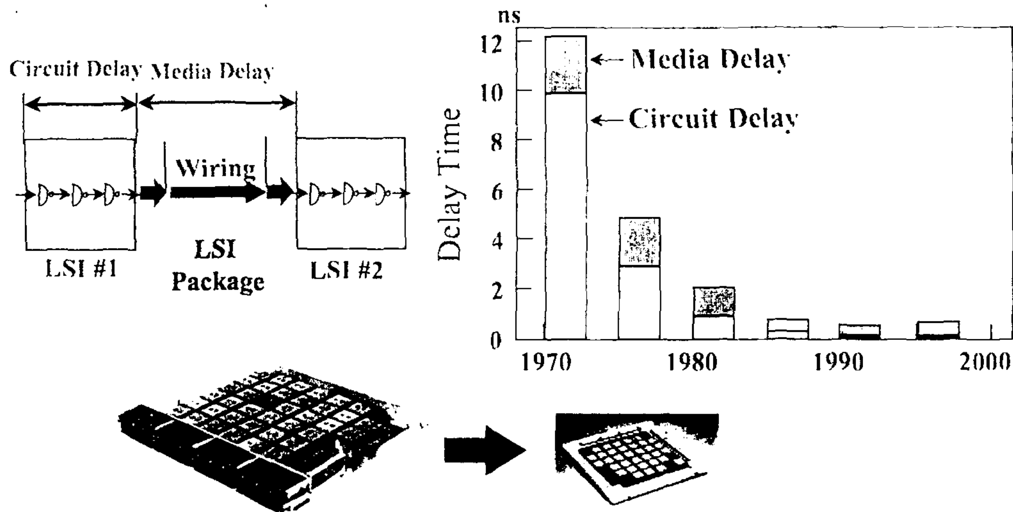
3. LSI Packaging Technologies in NEC's High-End Computers

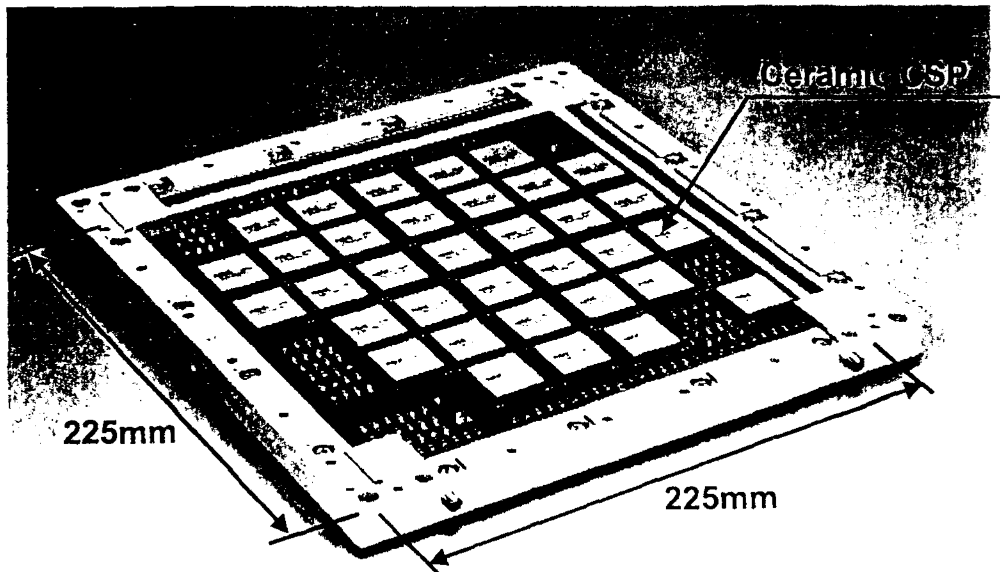
■ Circuit Delay and Media Delay



Higher density of LSI package reduces Media Delay, it also brings higher heat density. It causes higher error rate in operating electronic devices.

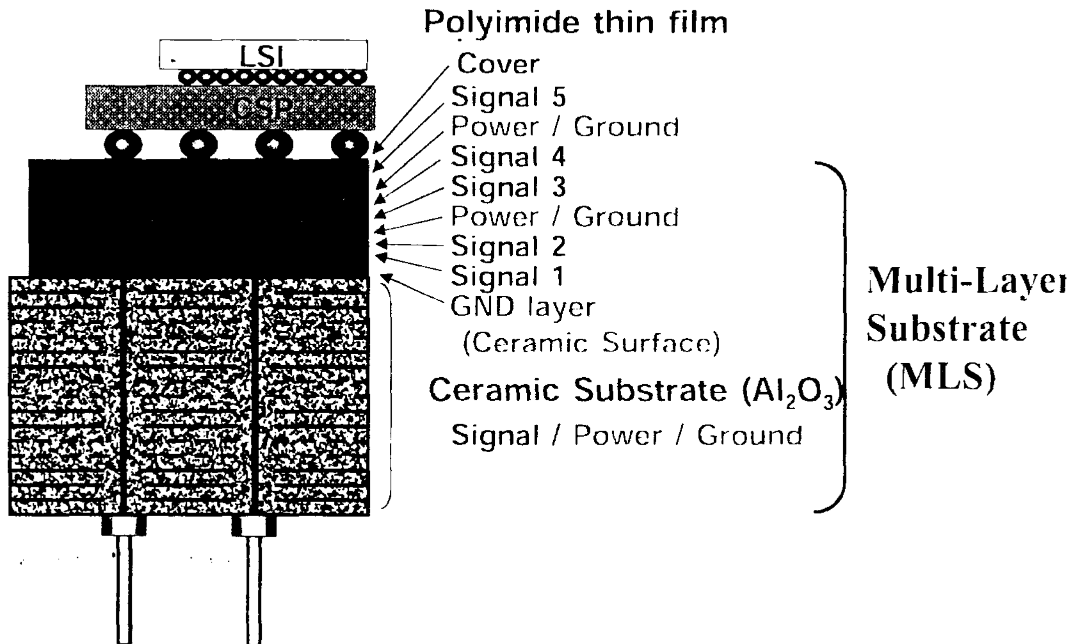
3. LSI Packaging Technologies in NEC's High-End Computers

■ CPU Package (MCP) of NEC SupercomputerSX-5



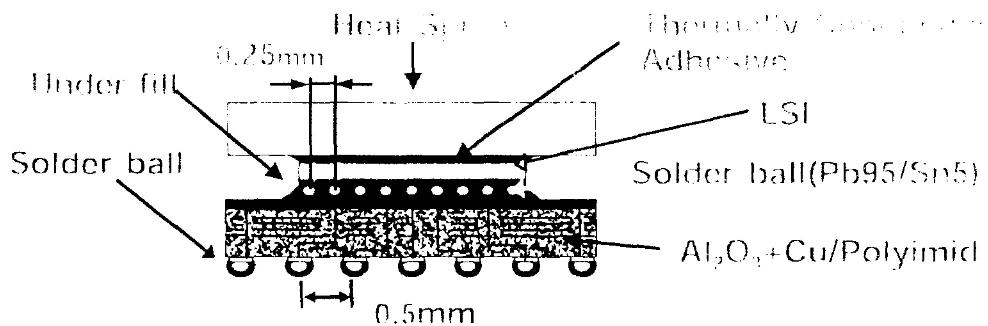
3. LSI Packaging Technologies in NEC's High-End Computers

■ Cross Section of Multi-Chip Package (MCP)



3. LSI Packaging Technologies in NEC's High-End Computers

■ Cross Section of Ceramic CSP

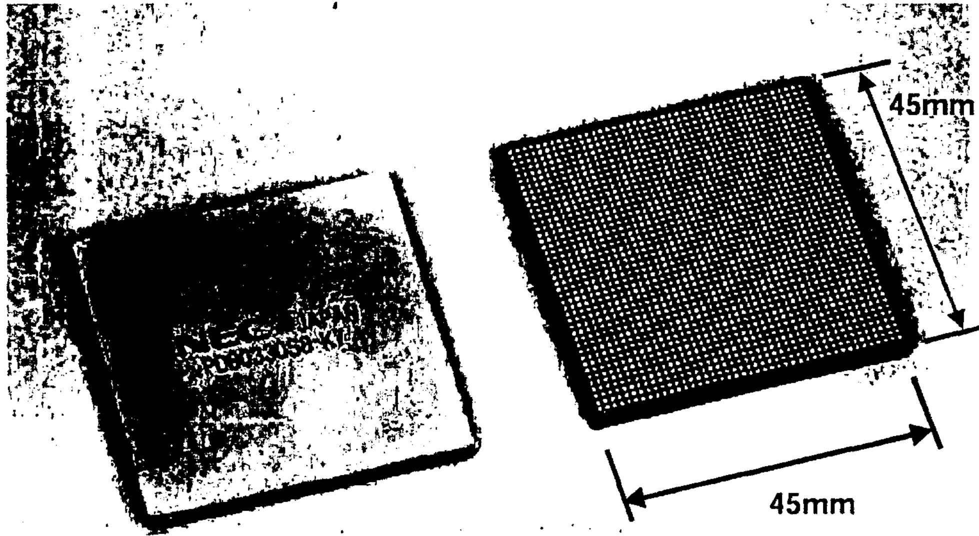


Specifications of ceramic CSP

Size [mm]	23 x 23
No. of I/O pins	2009
IO pitch [mm]	0.5
Substrate	Al_2O_3 + Cu/Polyimide
LSI I/O pitch [mm]	0.25

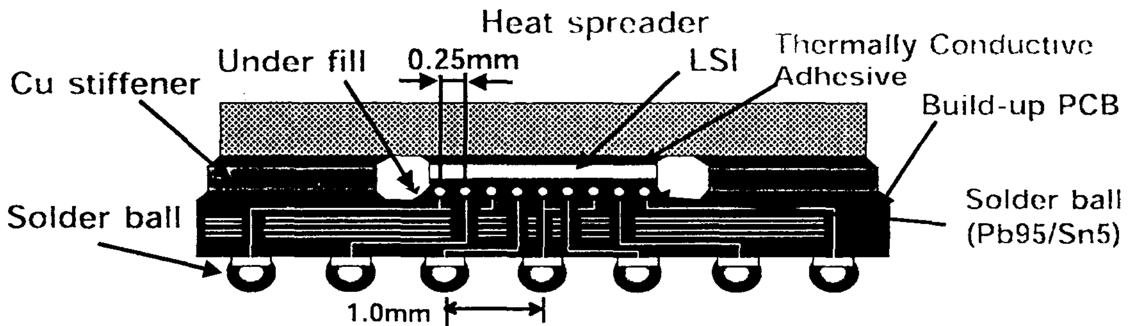
3. LSI Packaging Technologies in NEC's High-End Computers

■ BGA for Memory PCB



3. LSI Packaging Technologies in NEC's High-End Computers

■ Cross Section of BGA



Specifications of BGA	
Size [mm]	45 x 45
No. of I/O pins	1849
I/O pitch [mm]	1.0
Substrate	Build up PCB
LSI I/O pitch [mm]	0.25

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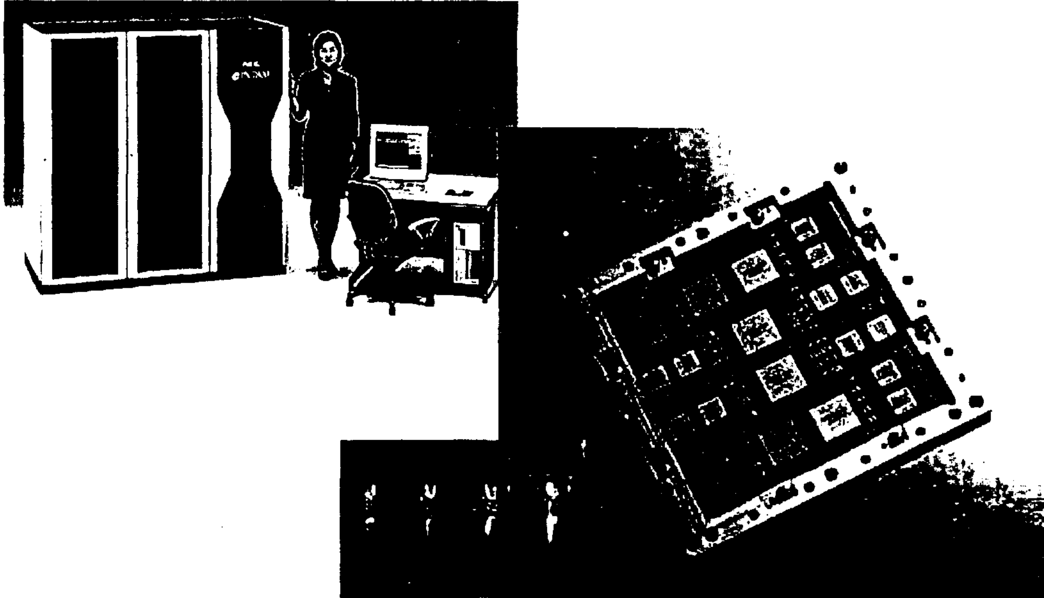
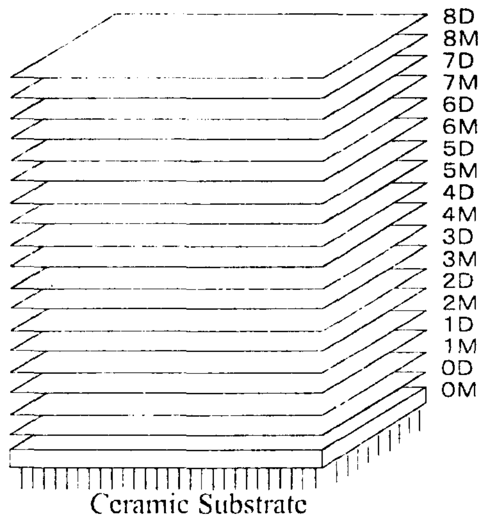
3. LSI Packaging Technologies in NEC's High-End Computers

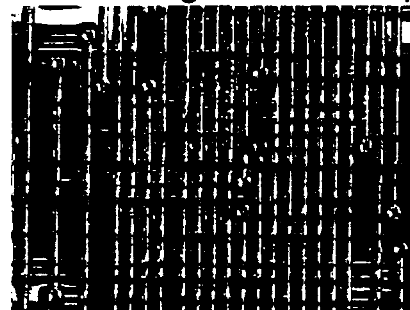
■ CPU Package(MCP) for NEC Server iPX7800SV



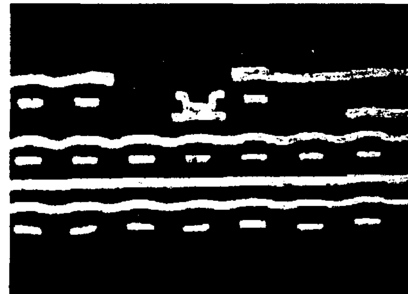
3. LSI Packaging Technologies in NEC's High-End Computers

■ Structure of Multi-Layer Substrate





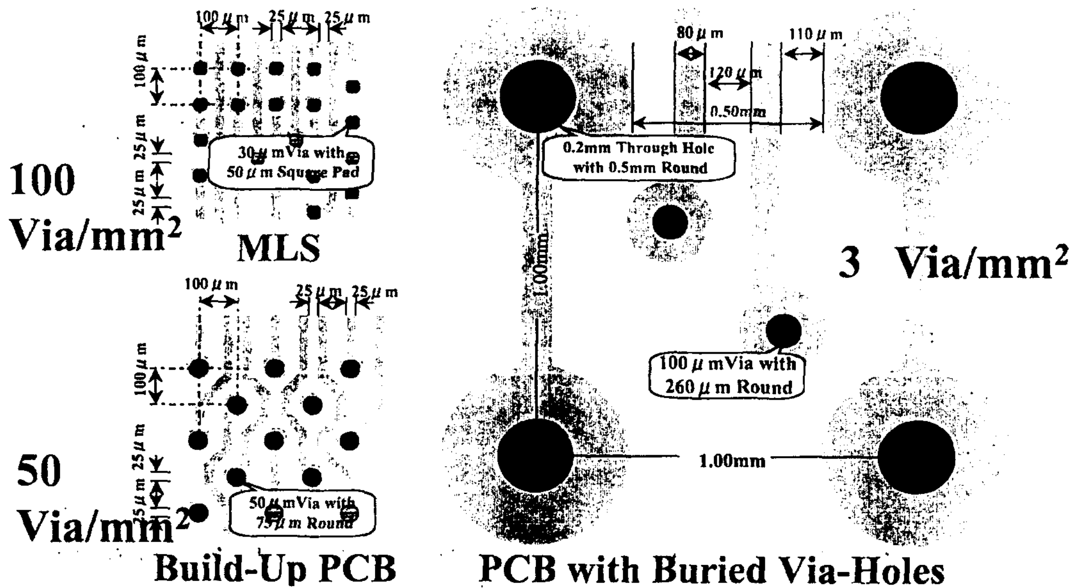
(a) Photograph of Signal Layer (L/S=25/ 25 μ m)



(b) Cross Section of Polyimide Thin-film Layers

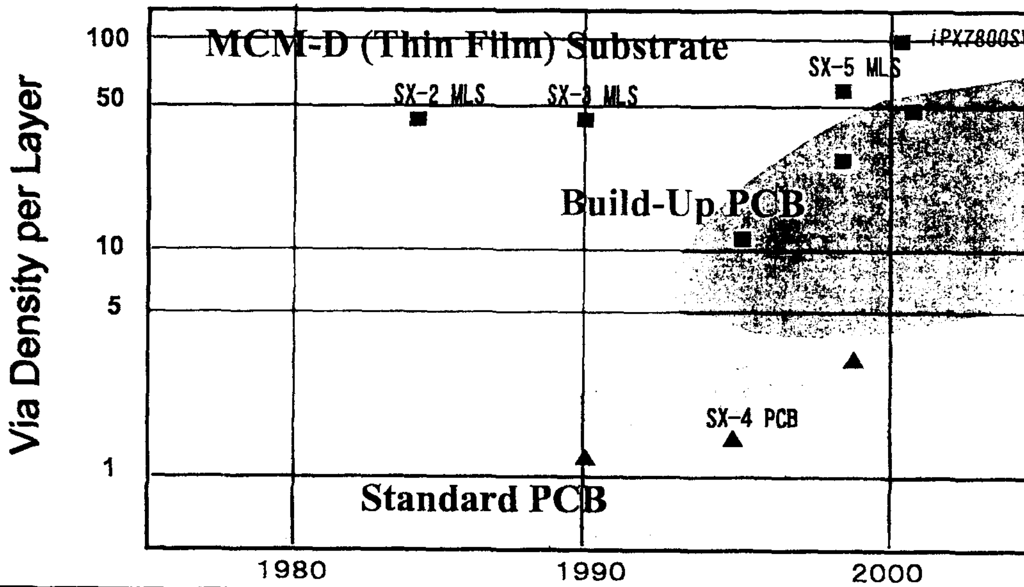
4. "Inter-Layer Transferability" of Wiring Substrates as Packaging Devices

■ Comparison of Design Rules for Wiring Substrates



4. "Inter-Layer Transferability" of Wiring Substrates as Packaging Devices

■ Transition of Inter-Layer Transferability



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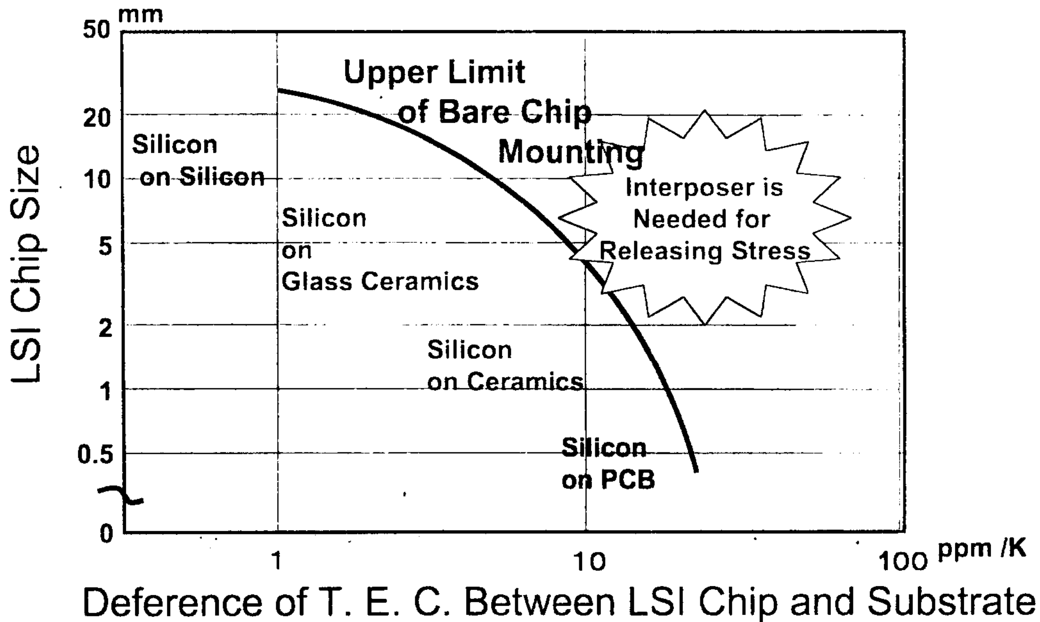
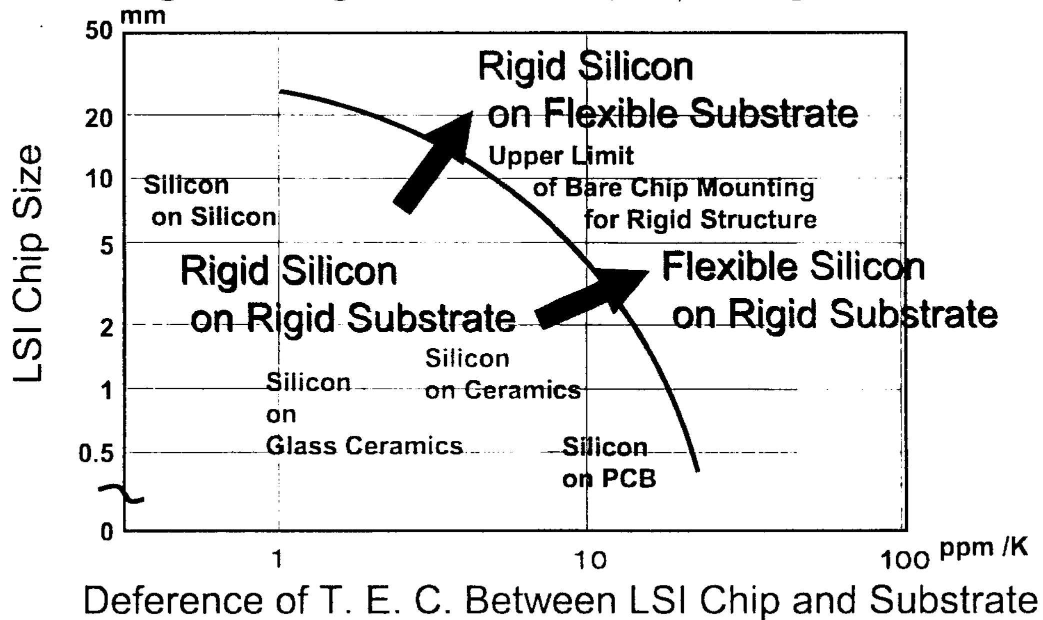
5. Future Aspect of LSI Packaging Technology

■ **Limit of Rigid Structure for Bare Chip Mounting**



5. Future Aspect of LSI Packaging Technology

■ **Challenge for Large Size Bare Chip Mounting**



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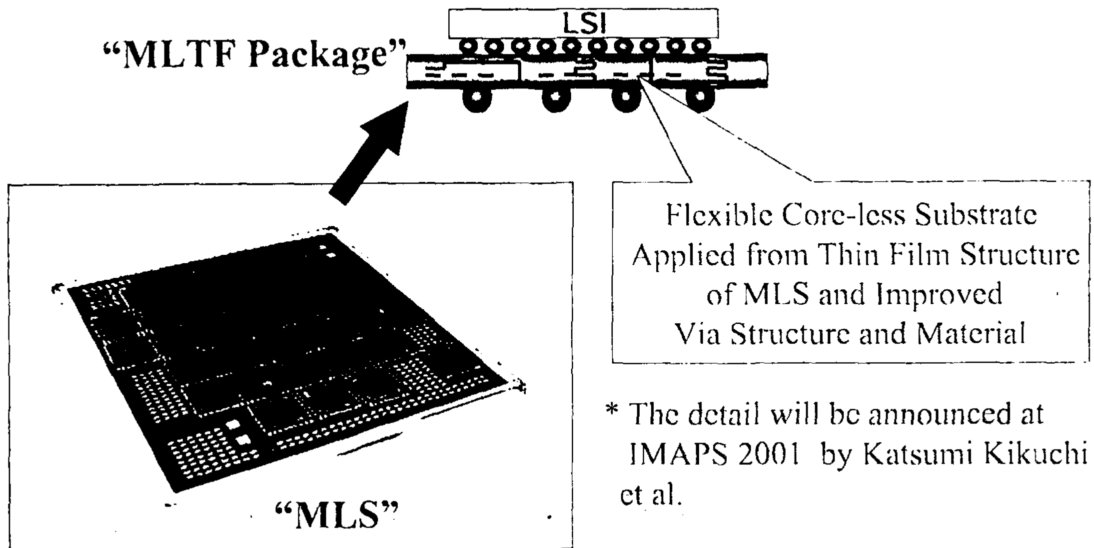
5. Future Aspect of LSI Packaging Technology

■ **"MLTF" Package, an Application of Flexible Substrate**



* The detail will be announced at IMAPS 2001 by Katsumi Kikuchi et al.

6. Summary

1. "MLS", state of the art MCM-D wiring substrate.
2. High pin-count LSI assembly.
3. Higher speed needs higher packaging density.
4. Wiring substrate, the key of LSI packaging device.
5. "Inter-Layer Transferability", a new index for the performance of wiring substrates.
6. "MLTF package", a core-less flexible package for high pin-count LSI.