Printed Circuit Board Technology Roadmap 2001 in Japan

Henry H. Utsunomiya

JEITA

Technology Trends on Printed Wiring Boards

September, 2001

Henry H. Utsunomiya

Interconnection Technologies, Inc.

JEITA

Contents

- Introduction on Working Group Members
- Trends on Motherboard Technologies
- Trends on Substrate Technologies
- Difficult Challenges
- Summary

JEITA

Introduction on WG Members

- Chair : Henry Utsunomiya ICT
- Motherboard WG :
  Hidetaka Hayashi, Fujikura
  Toshiki Sasabe, Shipley Fareast
  Toshiyuki Kobayashi, CMK
  Kazumasa Saito, Hitachi Kokusai

JEITA

Introduction on WG Members

- Substrate WG
  Ryusuke Yajima, Hitachi Chemical
  Kiyotaka Tsukada, Ibiden
  Kuniyuki Tanaka, Shinko Electric
  Seiichi Abe, Kyocera
  Jun Sasaki, Toppan

JEITA

Introduction on WG Members

- Observer

Toyohiko Kumakura, Hitachi Cable
Rikio Komagine, Hitachi Cable
Yoshinori Nakamura, Ibiden
Tadanori Ohminato, Fujikura
Fuminori Yamaguchi, NET
Susumu Honda, Shoei Laboratory

JEITA

WG Activity Report

- Questionnaire Investigation

◆Letter of Request Sending to : 100 Companies

◆Acceptance of Questionnaire Investigation : 60 Companies

◆Data Collected from : 106 Works

JEITA

Collected Questionnaire Data

- Buildup PWBs: 18 Works
- All Layer IVH PWBs: 6 Works
- Single Sided PWBs: 3 Works
- Double Sided PWBs : 11 Works
- Multilayer PWBs : 22 Works
- Flexible PWBs: 6 Works
- Rigid-Flex PWBs: 3 Works
- Substrate: 16 Works
- Common Issues: 21 Works


2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

Classified Production Technology Difficulties

Class	Required Production Technologies	Production Ratio	Cost
Class A Conventional	General Technology	80 %	Reasonable
Class B Leading Edge	Advanced Technology	15 %	Cost up
Class C State of the art	Most Advanced Technology	5 %	High Cost


2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

Characteristic of PWBs

- Motherboard PWBs:
- Basically supply to domestic market
- World most advanced technology for High Density Jisso Application (Especially Buildup Technology
- Delayed of development for Embedded Passive Devices & Embedded Active Devices from Europe, USA & Singapore
- Also delayed in R&D for Opto/electronics Jisso from Europe & USA

JEITA

Characteristic of PWBs

- Substrate:
- Holding 80% of Worldwide Market
- World most leading technology for Advanced substrate in volume production

3. Already started production of EPD substrate
4. Getting more severe competition against Taiwan & Korea

JEITA

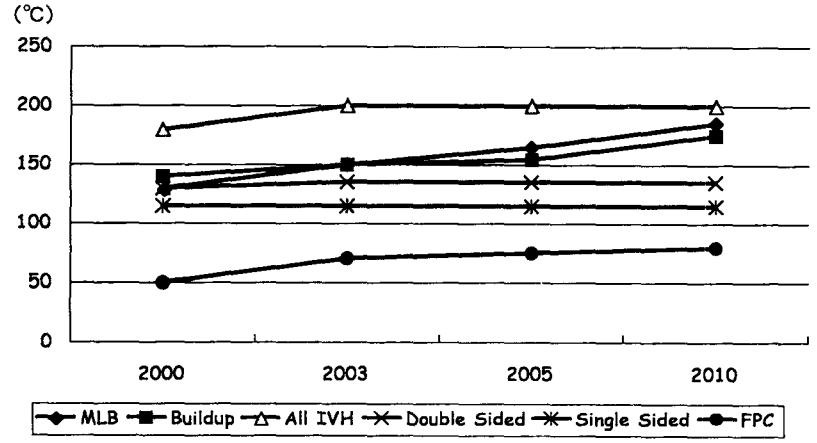
Technology Trends for Motherboard PWBs

- Characteristic Trends for Base Materials
- Mechanical Specifications Trends
- Conductor Specifications Trends
- Hole Specifications Trends
- Trends for Time to Market
- Trends for Cost

2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

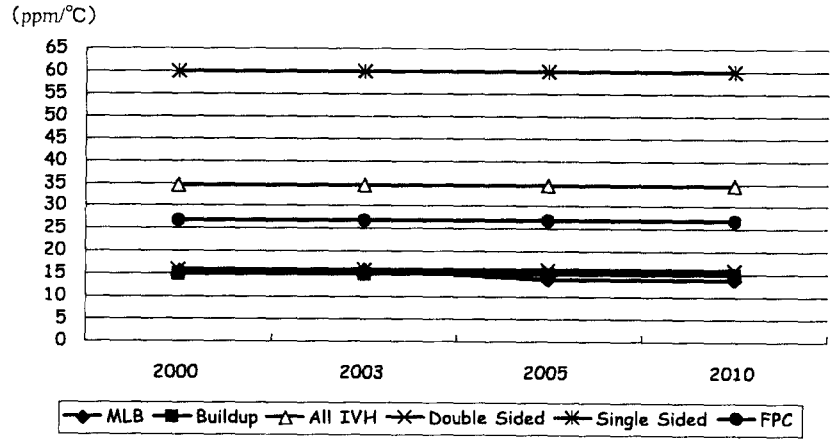
Trends on Glass Transition Temperature for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

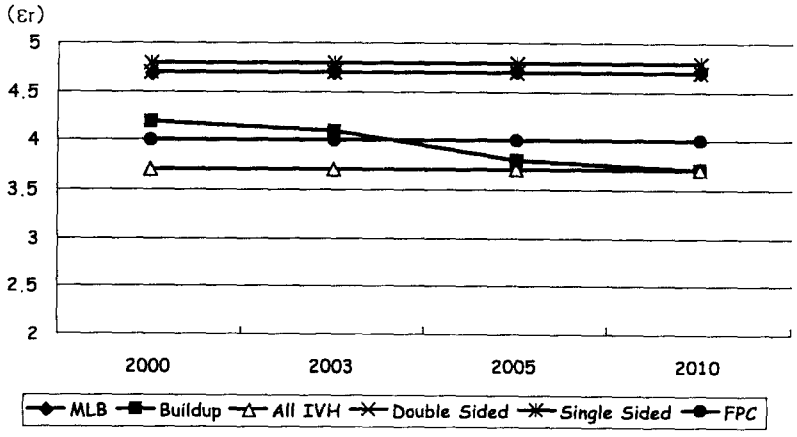
Trends on CTE for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

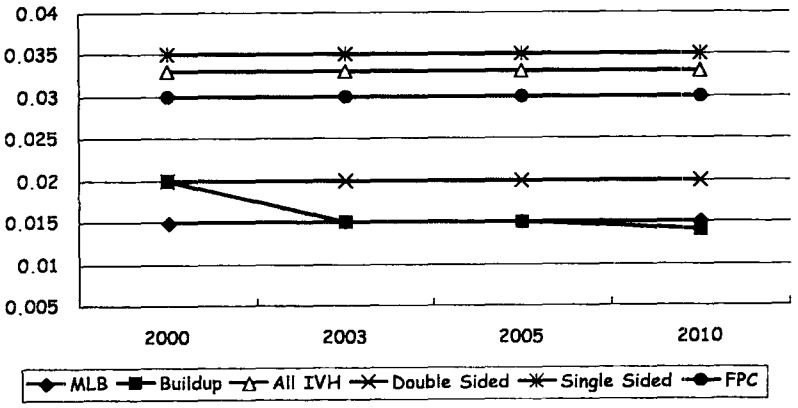
Trends on Dielectric Constant for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

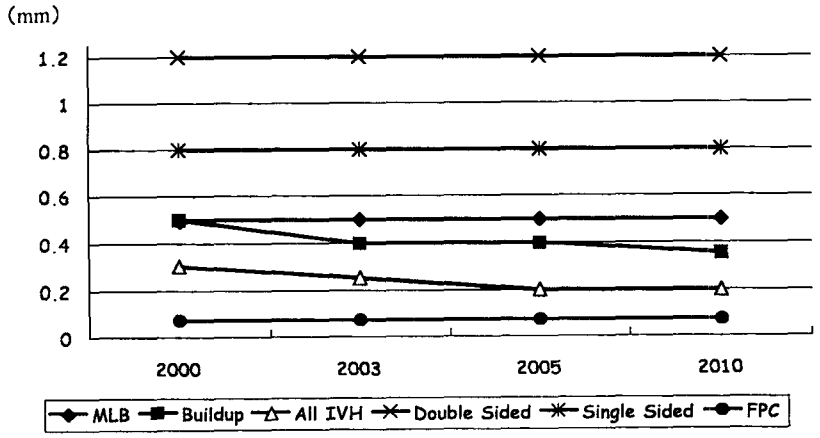
Trends on Dielectric Loss for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

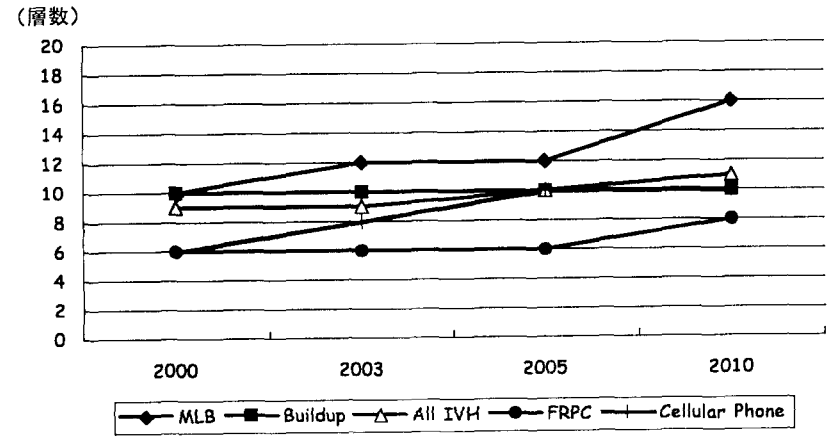
Trends on Min. PWB Thickness for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

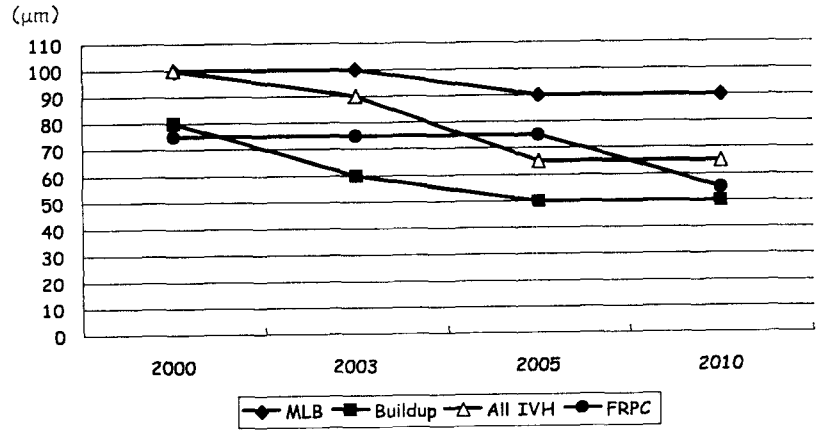
Trends on Max. Number of Layers for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

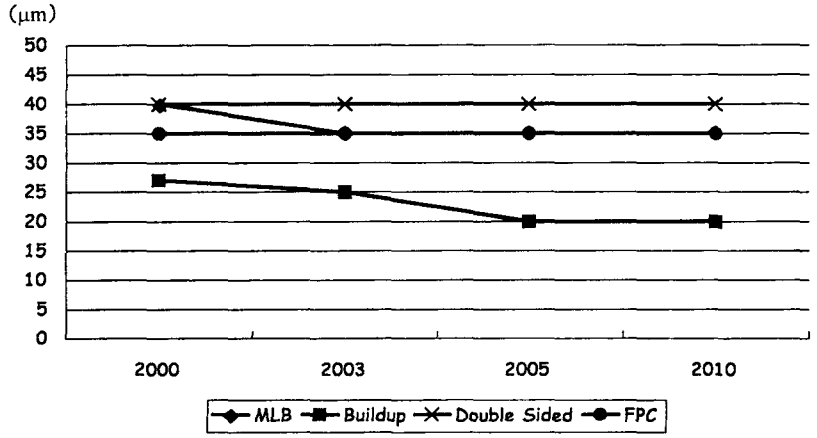
Trends on Min. Dielectric Material Thickness for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

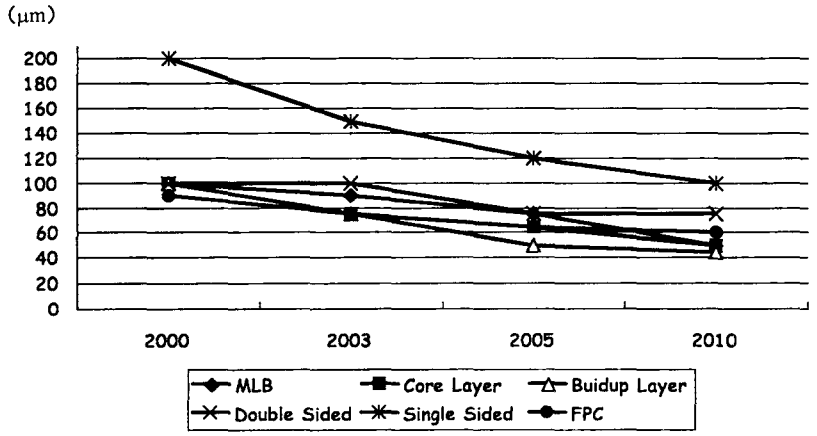
Trends on Min. Conductor Thickness for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

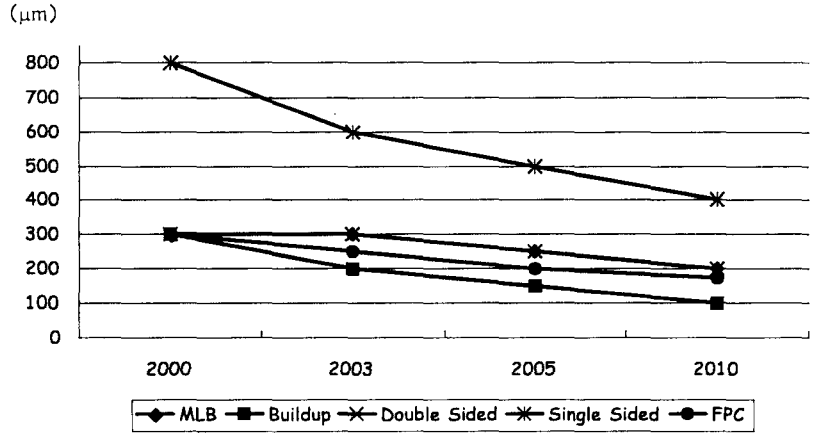
Trends on Min. Conductor Width for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

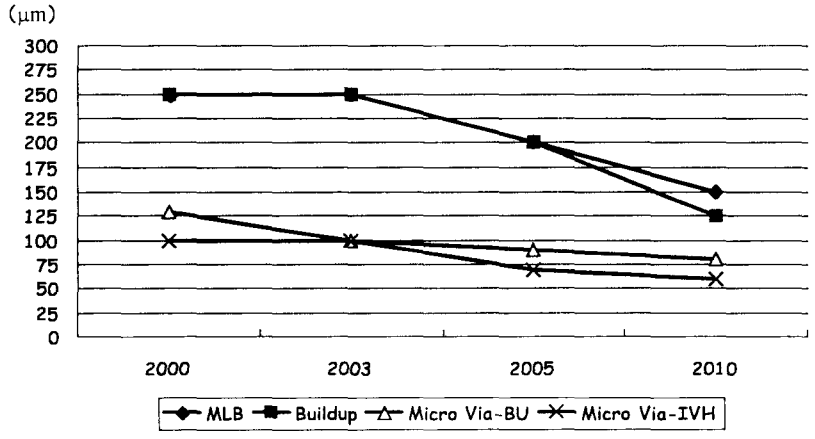
Trends on Min. Plated Through Hole Diameter for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

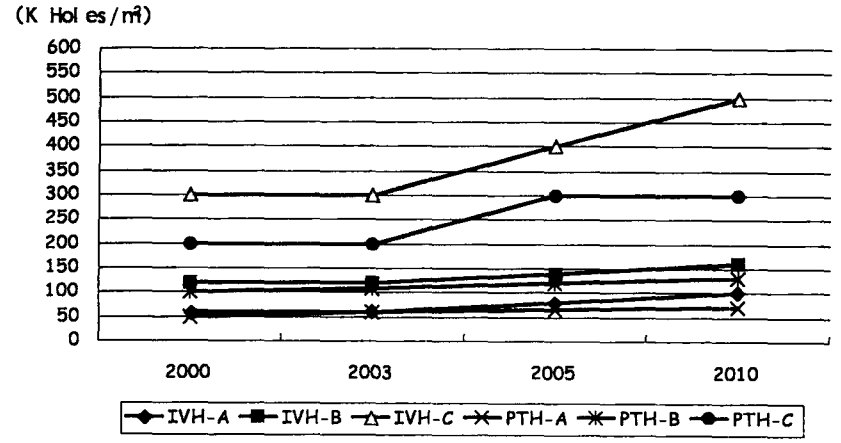
Trends on Min. IVH Diameter for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

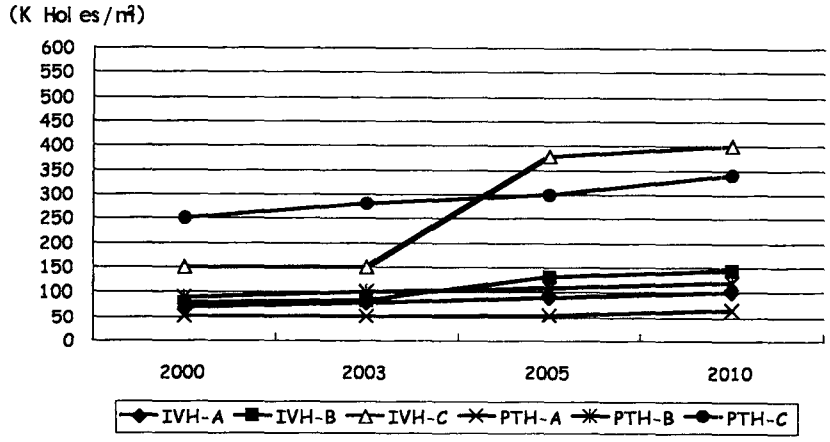
Trends on Max. Number of Holes for MLB Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

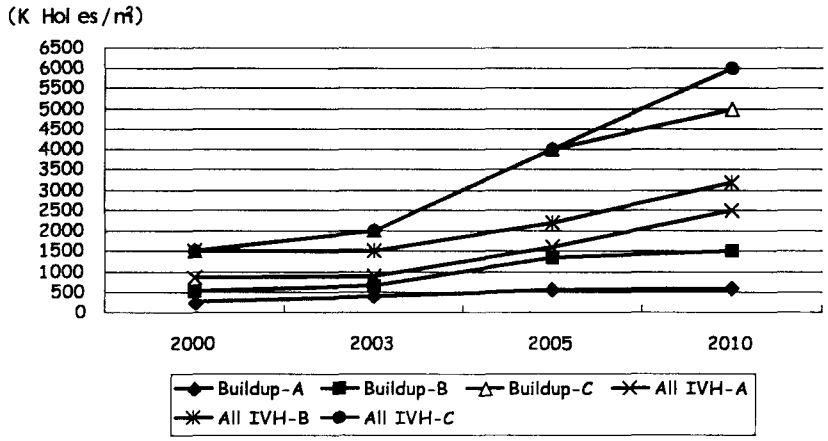
Trends on Max. Number of Holes for Buildup Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

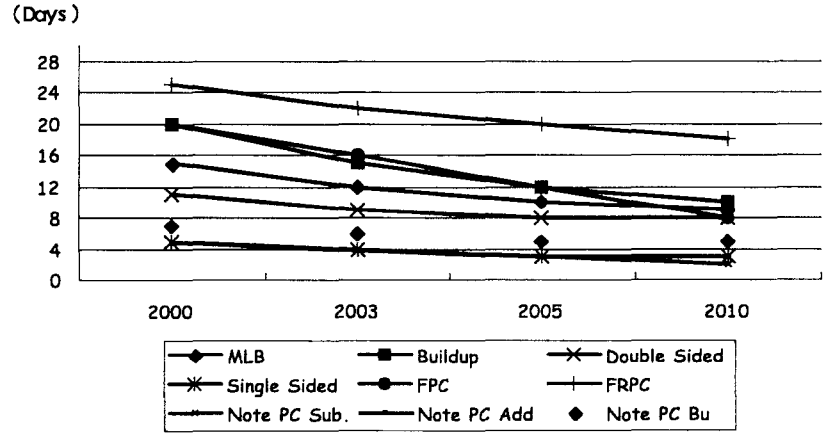
Trends of Max. Number of Micro Via Holes for Buildup



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

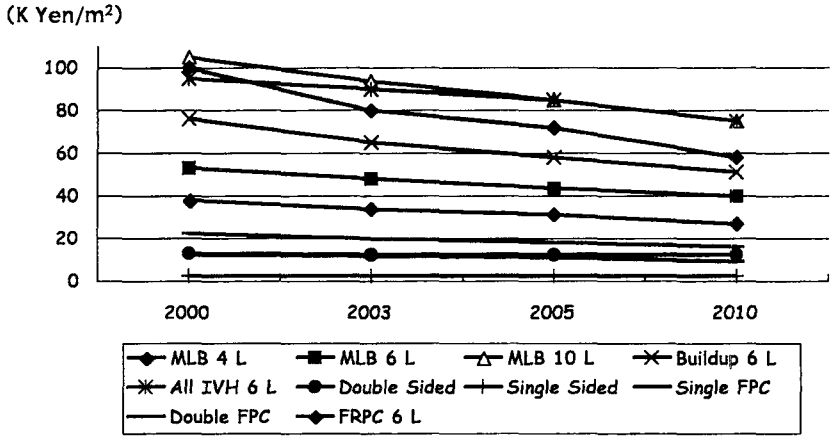
Trends on Average Lead Time for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

Trends on Average Price for Mother Board



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

Cost Reduction Requirements from Electronics Products

	2000	2005	2010
Notebook PC	100%	29%	19%
Digital TV	100%	69%	38%
Digital Camcorder	100%	58%	36%
Cellular phone	100%	69%	38%
Wearable PDA	100%	70%	50%

Source: 2001 JJTR-WG1 Activity Result, EIAJ

2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

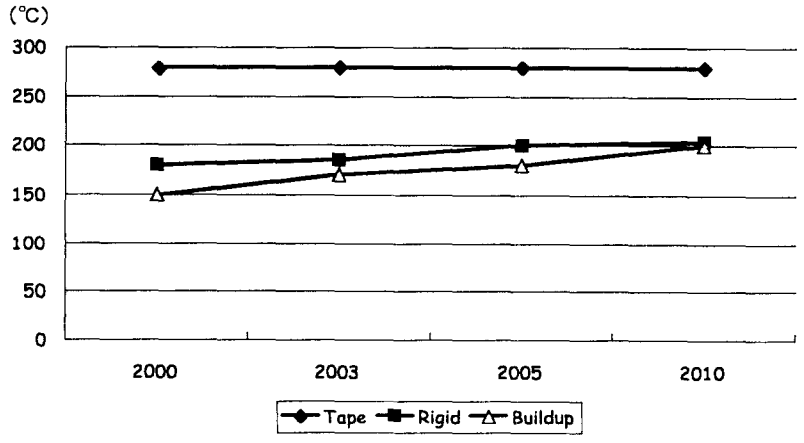
Technical Trends for Substrate

- Trends on Base Material Characteristic
- Trends on Mechanical Specifications
- Trends on Conductor Specifications
- Trends on Hole Specifications
- Trends on Average Lead Time
- Trends on Average Cost

2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

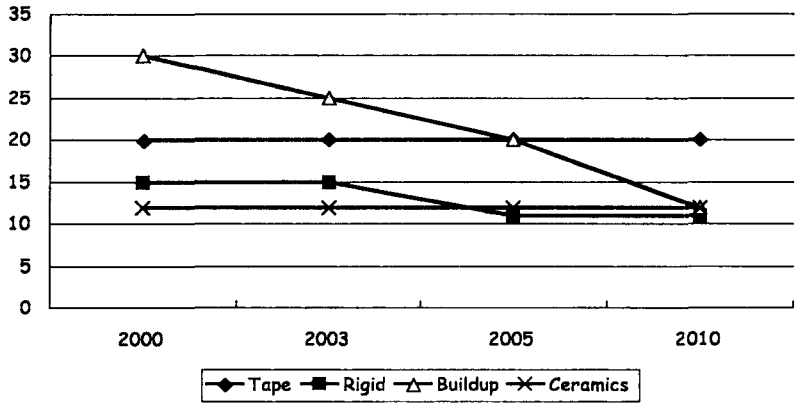
Trends on Glass Transition Temperature for Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

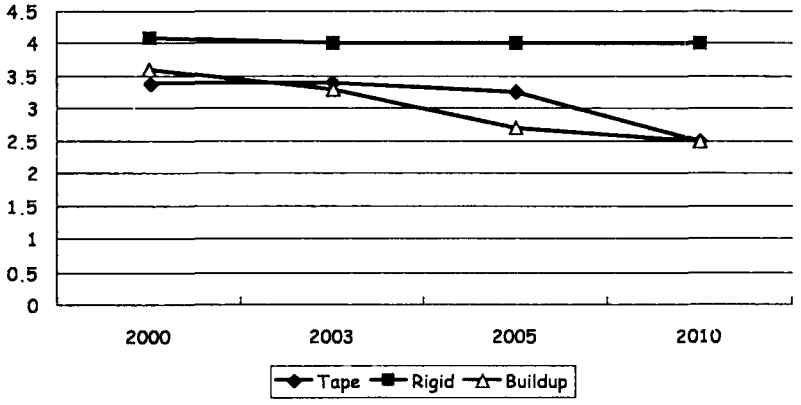
Trends on X-Y Dimension CTE for Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

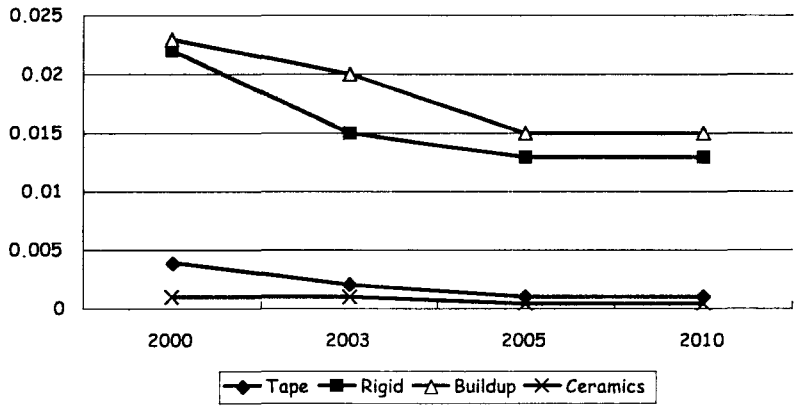
Trends on Dielectric Constant for Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

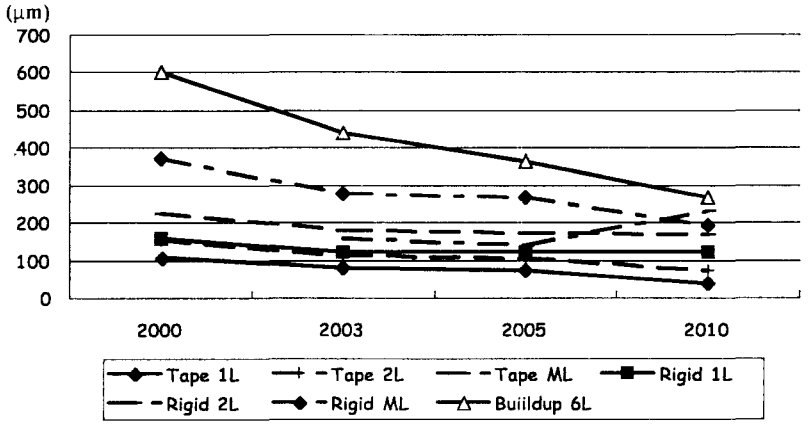
Trends on Dielectric Loss for Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

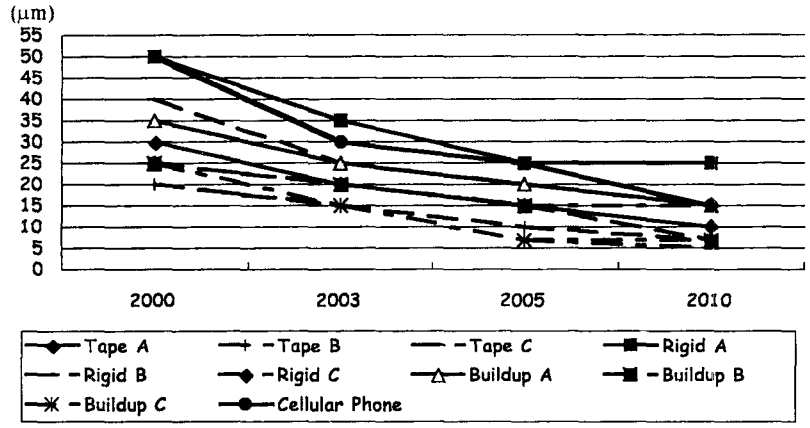
Trends on Min. Finished Substrate Thickness



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

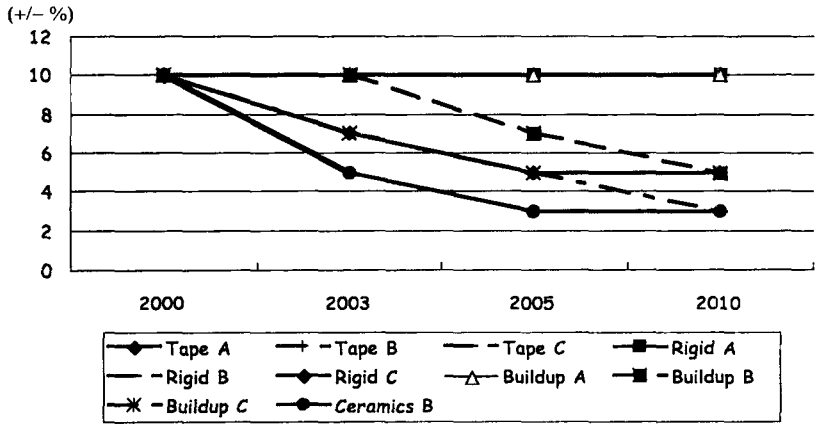
Trends on Min. Conductor Width for Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

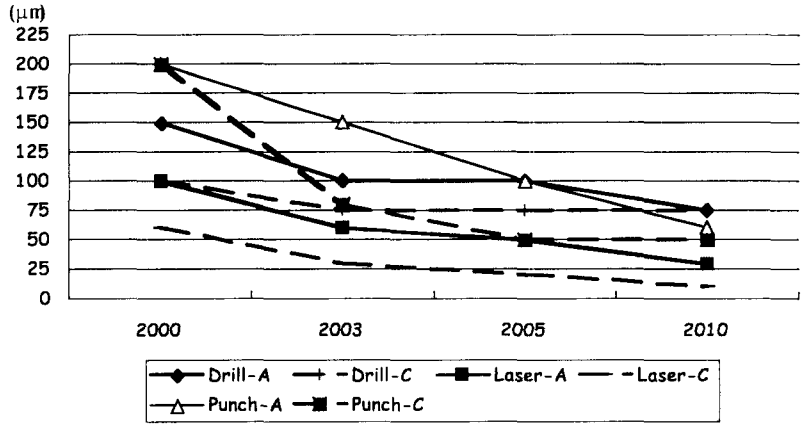
Trends on Characteristic Impedance Control for Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

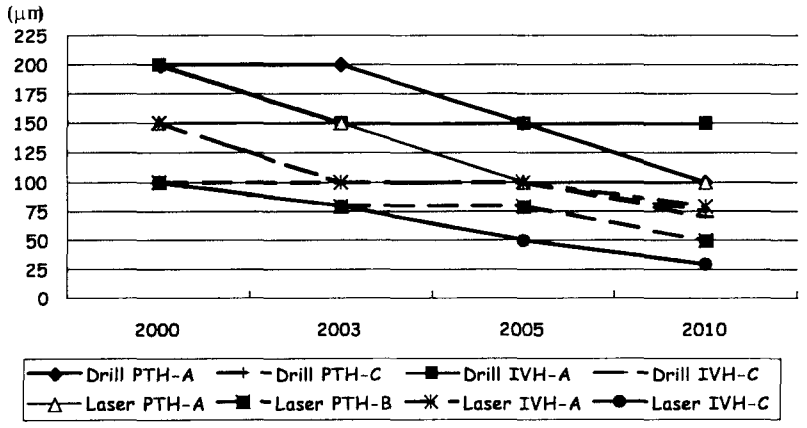
Trends on Min. Hole Diameter for Tape Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

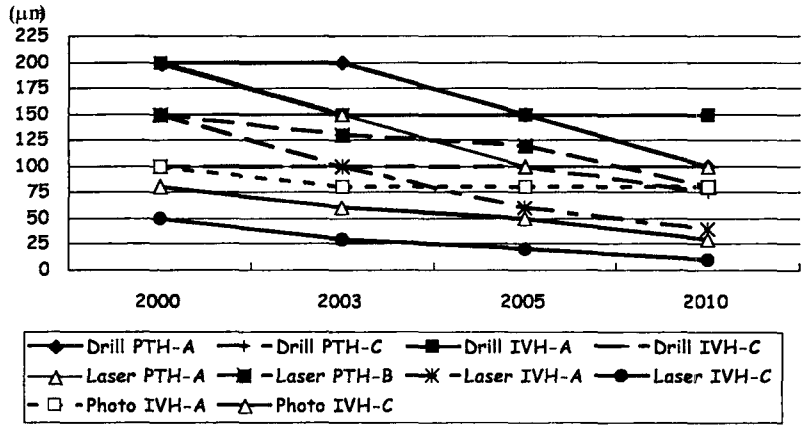
Trends on Min. Hole Diameter for Rigid Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

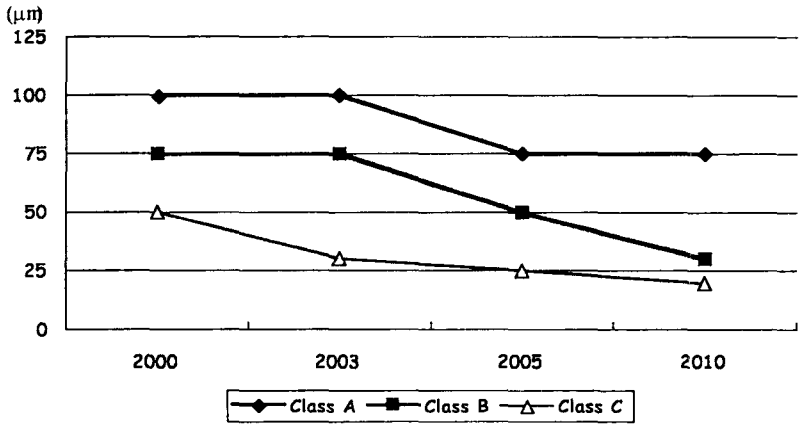
Trends on Min. Hole Diameter for Buildup Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

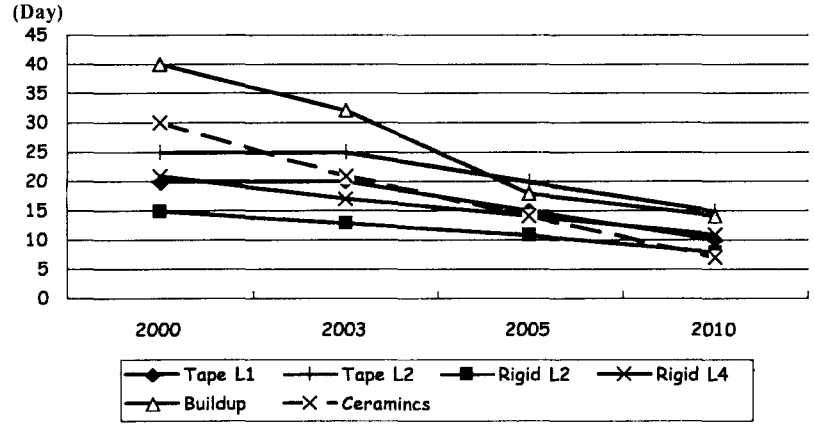
Trends on Min. Hole Diameter for Ceramics Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

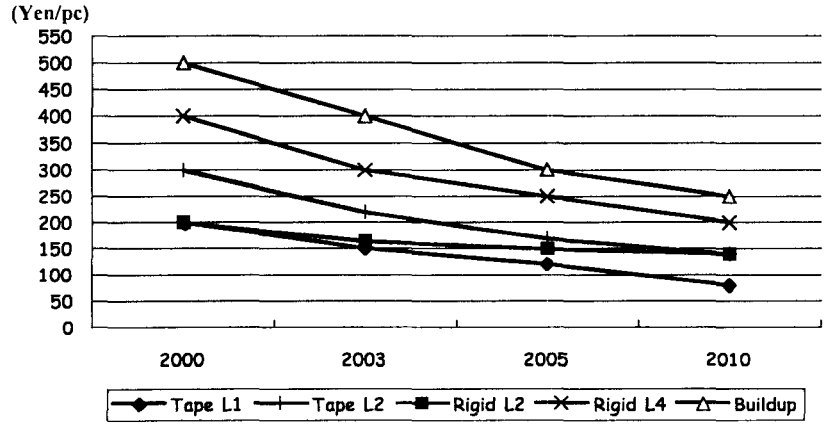
Trends on Average Lead Time for Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

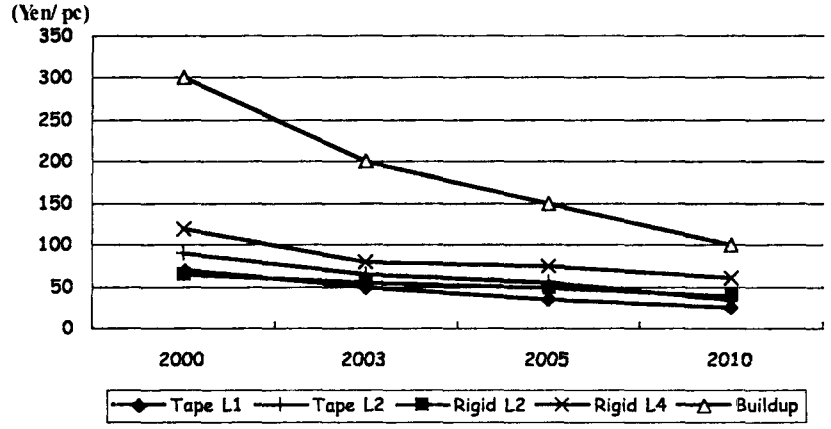
Trends on Average Cost for 45mm^2 Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

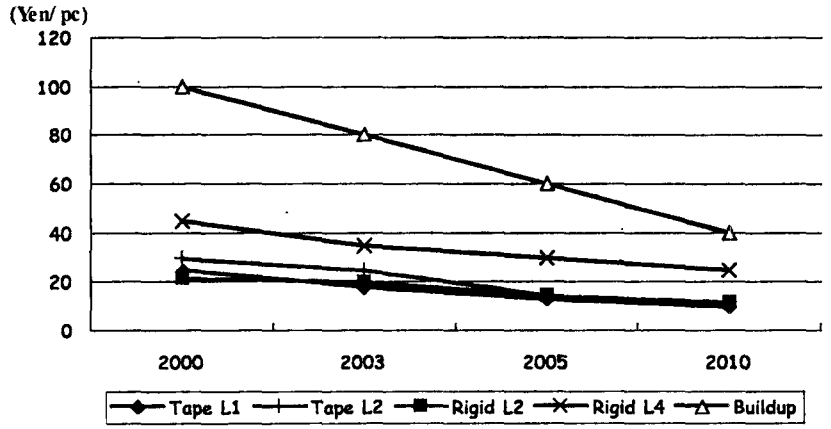
Trends on Average Cost for 25mm² Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

Trends on Average Cost for 12mm² Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

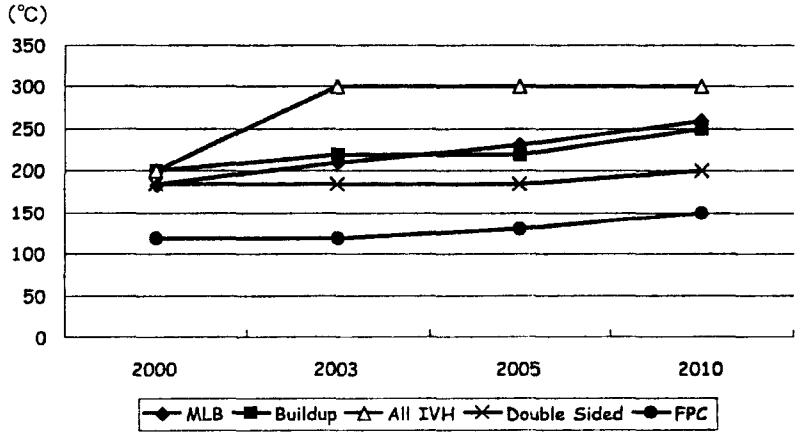
Difficult Challenges

- Mother Board Base Material
- Substrate Base Material
- Mother Board Mechanical Specifications
- Substrate Mechanical Specifications
- Mother Board Conductor Specifications
- Substrate Conductor Specifications

2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

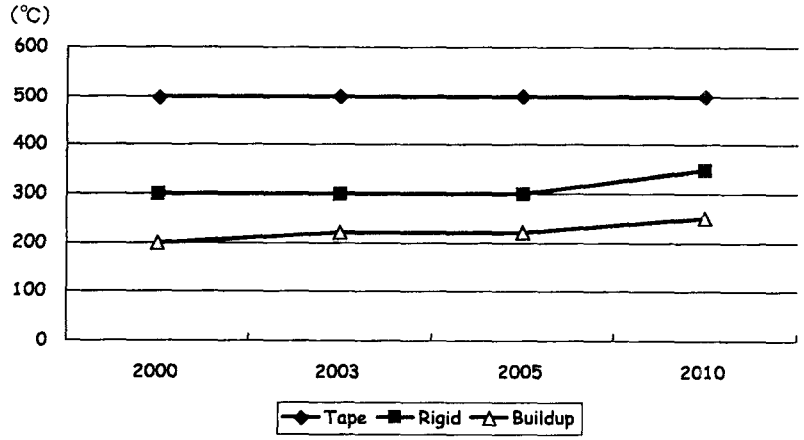
Trends on Class C Mother Board Glass Transition Temperature



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

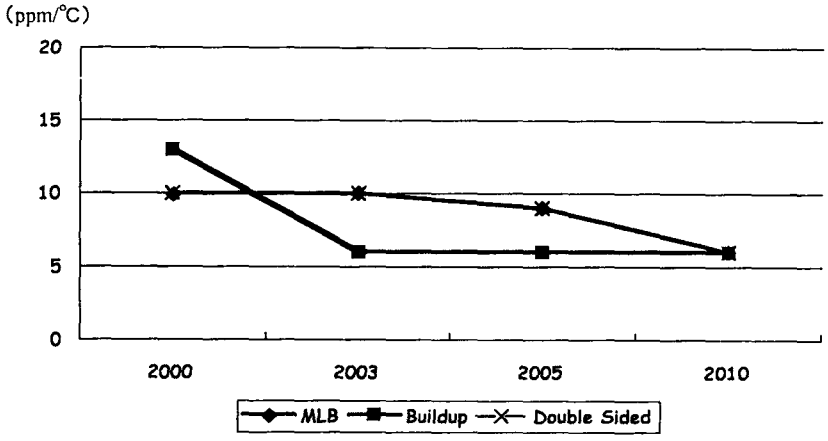
Trends on Class C Substrate Glass Transition Temperature



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

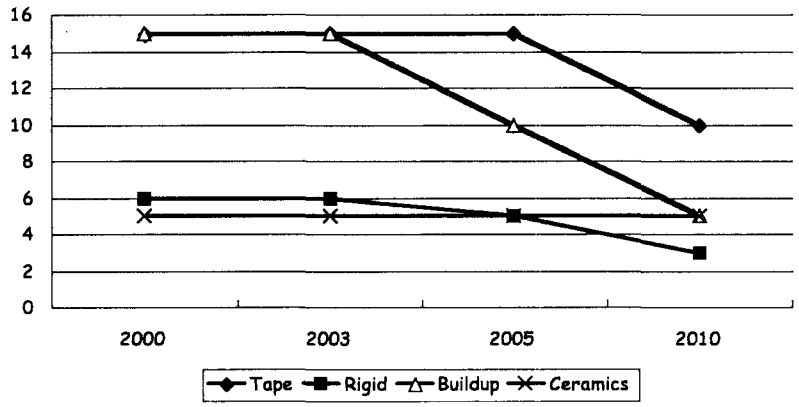
Trends on Class C Mother Board CTE



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

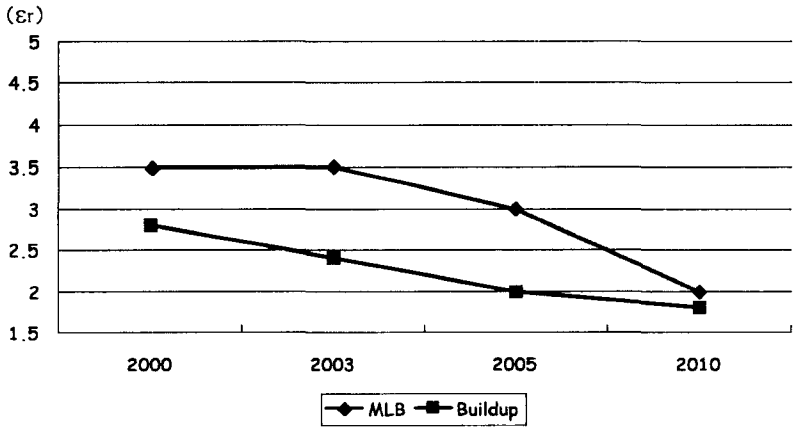
Trends on Class C Substrate X-Y Dimension CTE



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

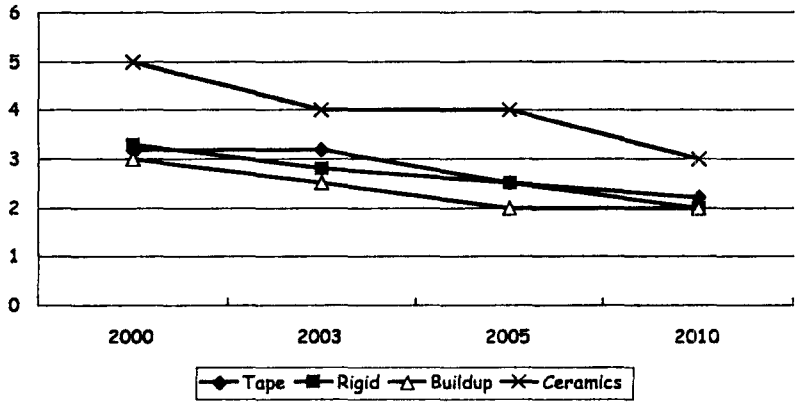
Trends on Class C Mother Board Dielectric Constant



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

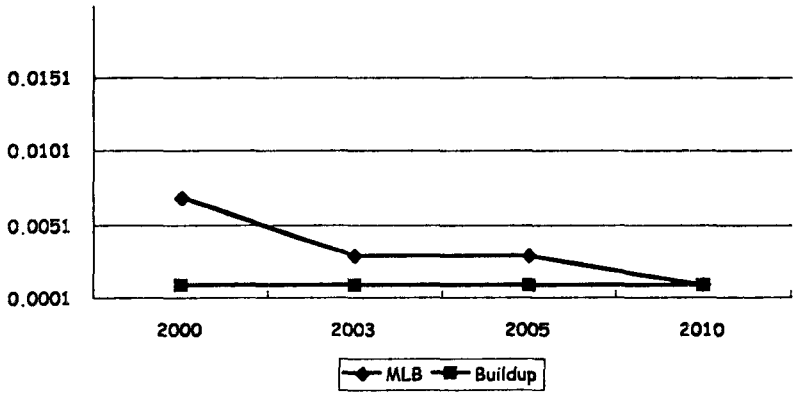
Trends on Class C Substrate Dielectric Constant



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

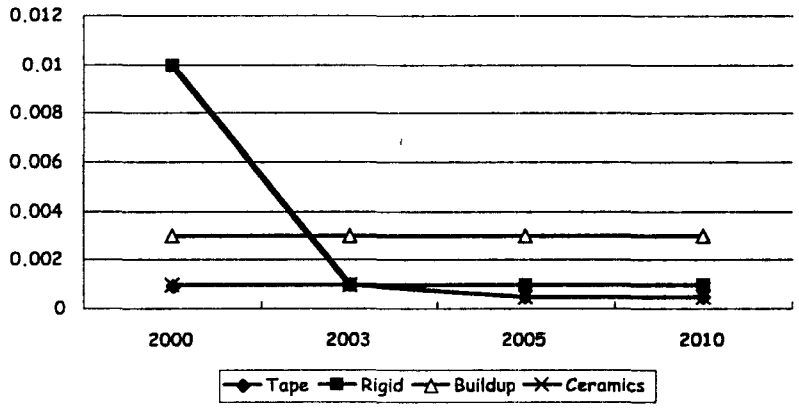
Trends on Class C Mother Board Dielectric Loss



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

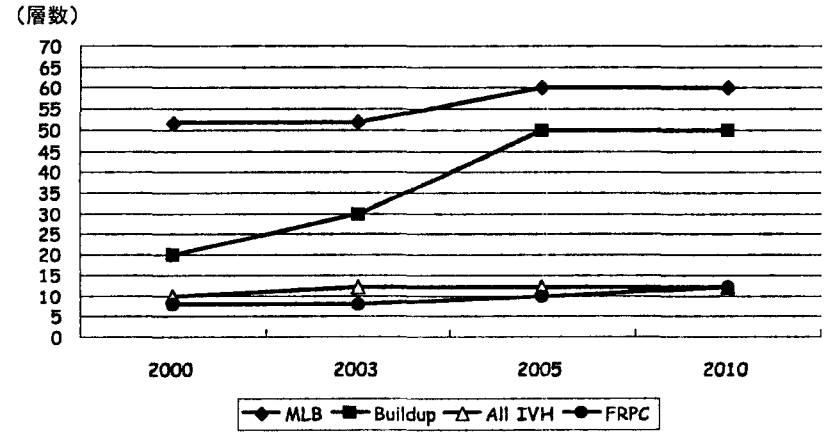
Trends on Class C Substrate Dielectric Loss



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

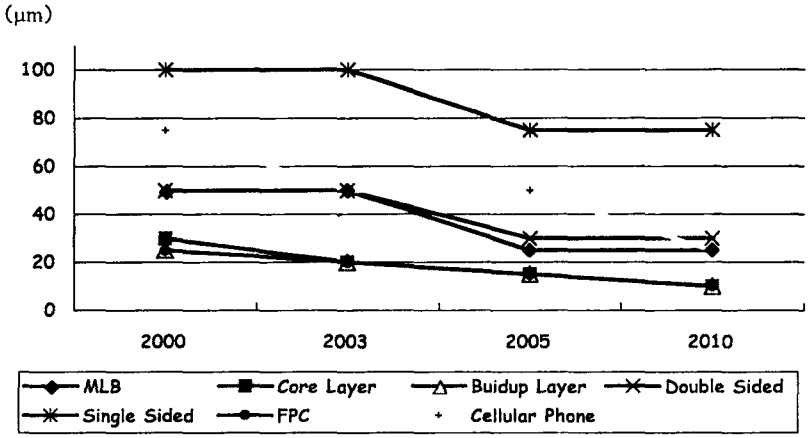
Trends on Class C Mother Board Max. Number of Layers



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

Trends on Class C Mother Board Min. Conductor Width



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

Min. Line/Space Requirements from Electronics Products

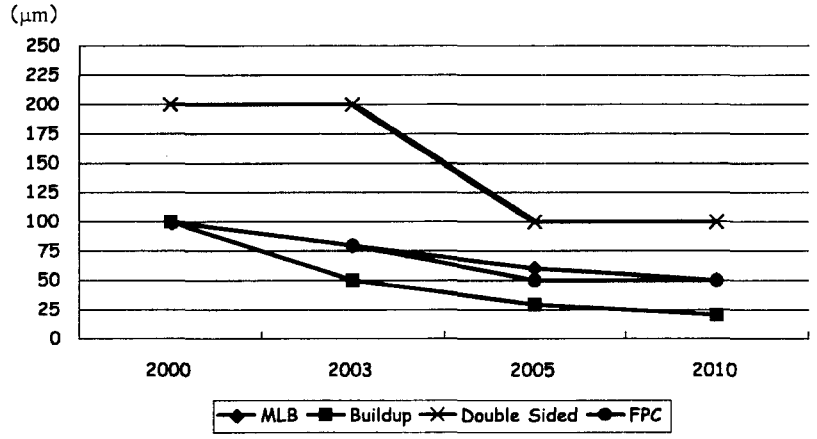
	2000	2005	2010
Not [illegible] oPC (μm)	100/100 50/70	50/50 40/60	20/20 20/20
Digital TV (μm)	150/150 100/100	100/100 80/80	80/80 50/50
Digital Cam corder (μm)	70/350 100/100	50/50 50/50	50/50 20/20
Cellular-phone (μm)	100/100 50/50	50/50 20/25	20/25 10/15
Wearable PDA (μm)	150/150	50/50	30/30

Source: 2001 JJTR-WG1 Activity Result, EIAJ

2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

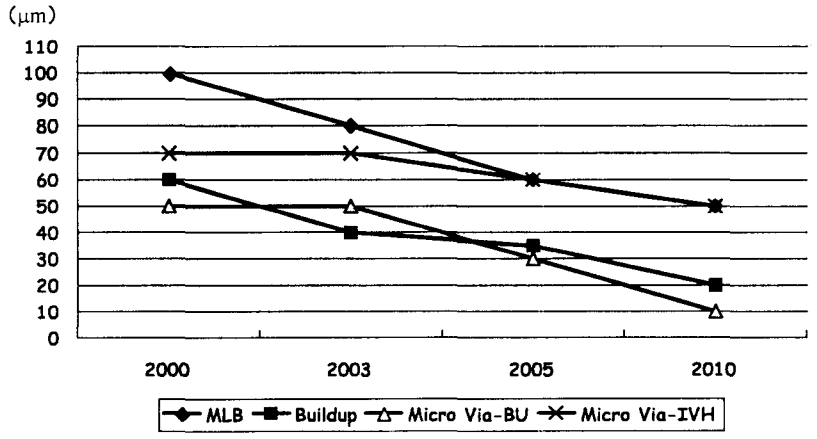
Trends on Class C Mother Board Min. PTH Diameter



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

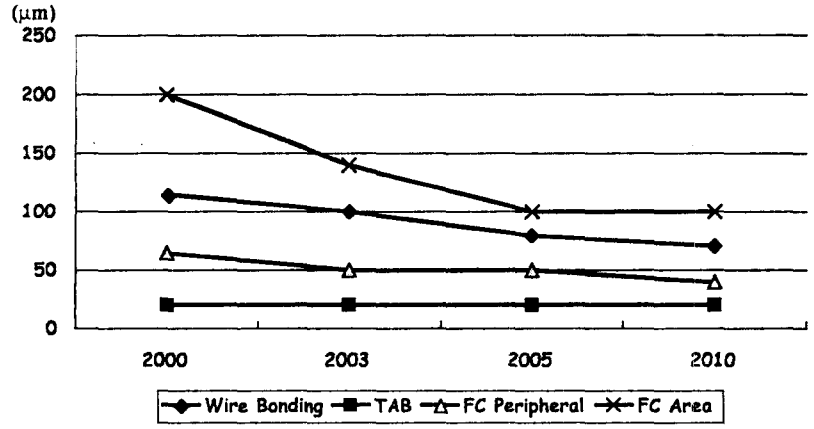
Trends on Class C Mother Board Min. IVH Diameter



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

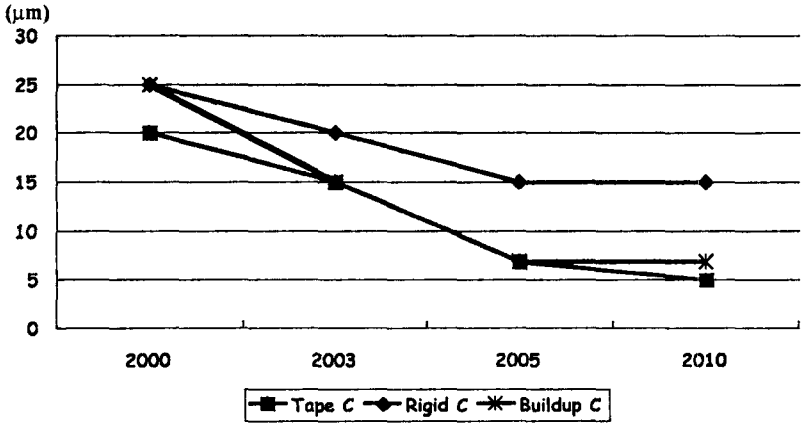
Trends on Outer Pad Diameter for Class C Substrate



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

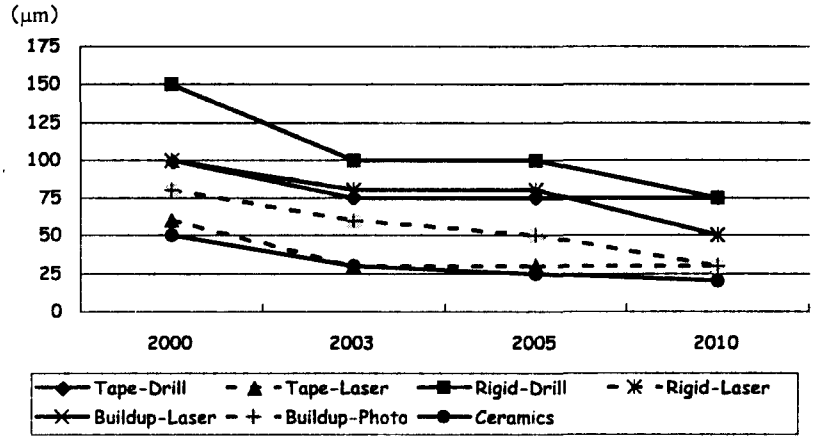
Trends on Class C Substrate Min. Conductor Width



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

Trends on Class C Substrate Min. PTH Diameter



2001 Japan Jisso Technology Roadmap in Seoul,

JEITA

Summary

- Fine Pitch Technology will be accelerated among next decade
- Buildup Technology is Key Technology for High Density Interconnection
- Novel Base Material is critical for High Speed, Area Array Flip Chip Application
- Japanese PWB Technology Roadmap will be Published soon.

2001 Japan Jisso Technology Roadmap in Seoul,