September 13, 2001

Jisso Technology Roadmap 2001 in Japan

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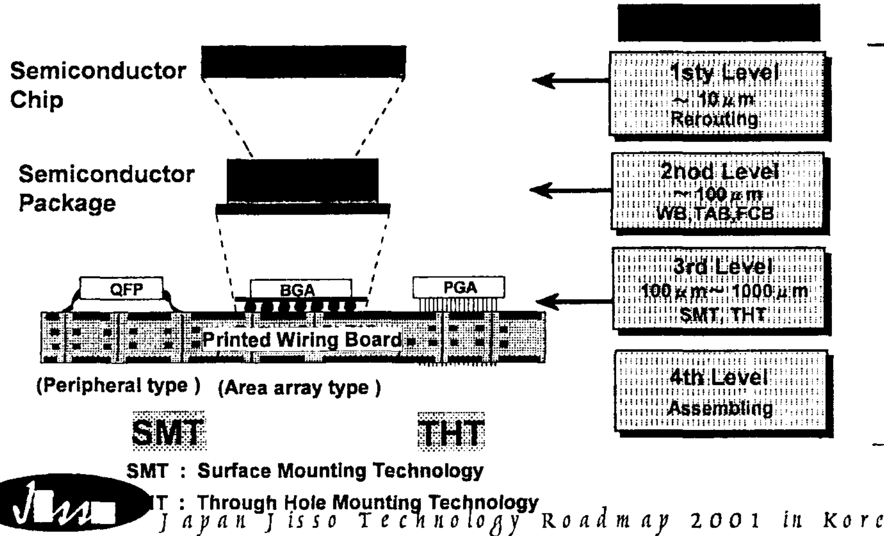
Japan Jisso Technology Roadmap Council,
Japan Electronics & Information Technology Industries Association (JEITA)

Contents

- Introduction
- Electronic Products Trends
- LSI Package Trends
- Electronic Components Trends
- Jisso Equipment trends
- Summary


The Concept of Jisso (実装) ?
Total solution for Interconnecting, Assembling, Packaging, Mounting and Integrating system design.
Semiconductor Chip
Semiconductor Package
QFP
BGA
PGA
Printed Wiring Board
(Peripheral type)
(Area array type)
SMT
THT
1sty Level
~10μm
Rerouting
2nod Level
~100μm
WB,TAB,FCB
3rd Level
100μm~1000μm
SMT, THT
4th Level
Assembling
SMT : Surface Mounting Technology
T : Through Hole Mounting Technology
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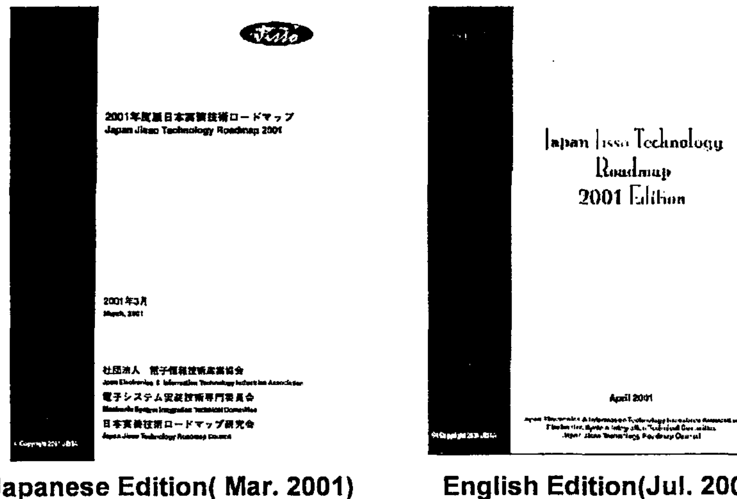
Japan Jisso Technology Roadmap 2001
2001年度版日本実装技術ロードマップ
Japan Jisso Technology Roadmap 2001
Japan Jisso Technology Roadmap 2001 Edition
April 2001
Japanese Edition(Mar. 2001)
English Edition(Jul. 2001)
Japan Jisso Technology Roadmap 2001 in Korea

Contents of JJTR 2001

1. General Overview
2. Trends of Electronic Products
3. Trends in Components & Packaging Equipment
   - 3.1 Semiconductor Devices
   - 3.2 Electronic Components
   - 3.3 Printed Wiring Boards
   - 3.4 Jisso Equipment

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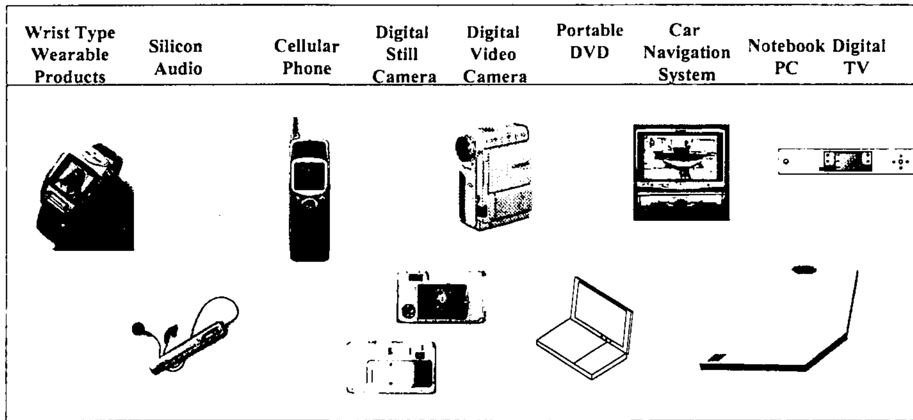
Electronic Products Classification

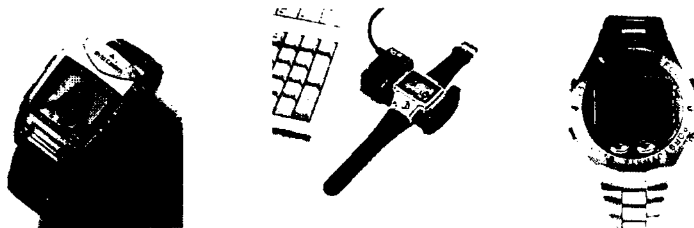
- Classified by Japanese competitiveness & strength
- Product's outer dimension & size

Size Small ⟵ ⟶ Size Large

Wrist Type Wearable Products	Silicon Audio	Cellular Phone	Digital Still Camera	Digital Video Camera	Portable DVD	Car Navigation System	Notebook PC	Digital TV



Jisso Technology Requirements from Wearable Products



- ■ Low Power Consumption
  - ⇨ 1/5～1/7 of the current level
- ■ Use of bare chip for smaller and thinner devices
- ■ Integration of middleware ASIC & Bluetooth into chip
- ■ SiP Module Design
- ■ 3D LSI Packages
- ■ CCD embedded LSI

Good Prospect on SoC

Jisso Technology Requirements from Cellular Phone

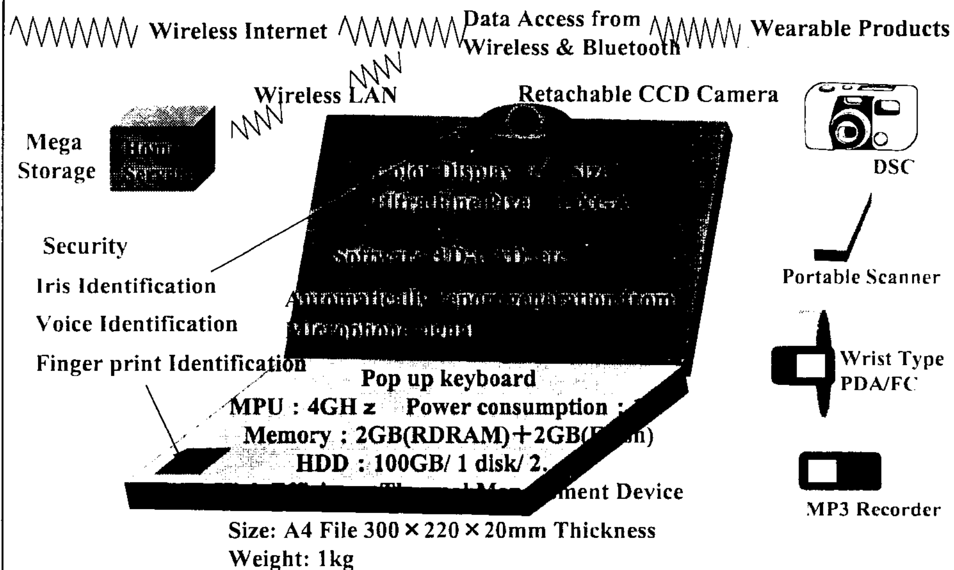
■ **More Diversified Functions**

Color Display	GPS
PDA	Game
MP3	Blue tooth
CCD	E-Commerce

■ **Request for LSIs & Packages**

- ■ Lower power consumption
- ■ Lower voltage drive
- ■ Small, thin, large-capacity memory
- ■ Low profile Semiconductor package
- ■ CCD embedded LSI
- ■ Speedy implementation of new functions
- ■ Cost reduction

Notebook PC Forecast by 2005

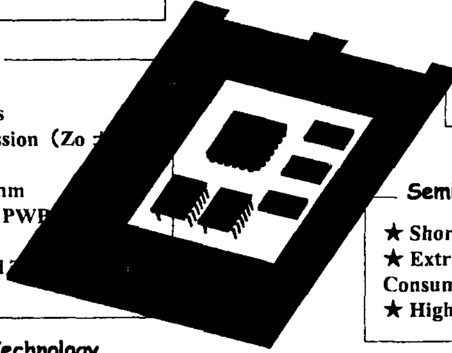


Jisso Technology Required for Notebook PC in 2005

Design Systems
- ★ High accuracy, advanced function design CAD Systems
- ★ New concept based manufacturing process CAD/CAE

PWB
- ★ Mother Board PWB
  Light weight 4 Layers
  High Speed Transmission (Zo
  L/S : 75 μm /75 μm
  Size : 150mm × 100 mm
- ★ Module & Substrate PW
  L/S: 25μm/25 μm
  6 Layers, High Speed
  Size: 75mm × 50 mm

Jisso Process Technology
- ★ Low Temperature Reflow Soldering



Passive Components
- ★ Mini. Chip Size: 0603

Other Components
- ★ Peltier Device

Semiconductor Package
- ★ Short TAT LSI Development
- ★ Extremely Low Power Consumption
- ★ High Speed Graphic Chip

Quick Delivery, Good Quality at Low Cost

Requirements for Packaging

CSP ball pitch (advanced Technology)

(mm)

	2000	2005	2010
Note type PC	0.8	0.5	0.15
Wearable Products	0.5	0.3	0.3
Mobile Audio Sets	0.5	0.3	0.15
DVC.DSC	0.5	0.3	0.15
Palm top DVD	0.8	0.5	0.3
Digital TV sets	0.5	0.3	0.15
Cellular Phone	0.5		0.3

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Low Profile Requirements (mm)

	2000	2005	2010
Wearable Products	1.5	1.0	0.8
Mobile Audio Sets	2.0	1.0	0.7
Cellular Phone	1.0~1.5	0.8~1.0	0.5~0.8
Digital Still Camera	1.2	0.8	0.4
Digital Video Camcorder	1.2	0.8	0.5
Palm top DVD	3.9	1.0	0.7
Car-Navigation	1.5	1.0	1.0
Note type PC	1.0~1.2	0.5~1.0	0.5
Digital TV sets	4.0	4.0	3.0

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PWB Structure Requirement

	2000	2005	2010
Wearable Products	Buildup 4 Layers	Buildup 4-6 Layers	Silicon PWB 3D PWB
Mobile Audio Sets	Buildup 6 Layers	Buildup 8 Layers	3D PWB
Cellular Phone	Buildup 4~6 Layers	Buildup 4~10 Layers	Buildup 4~10 Layers
DSC	IVH 8 Layers Buildup 6~8 Layers Rigid Flex 6 Layers	Buildup 6~8 Layers Rigid Flex 6~8 Layers	Buildup 6~8 Layers Rigid Flex 6~8 Layers
DVC	Buildup 8 Layers	Buildup 8 Layers + Rigid Flex	Buildup 8 Layers + Rigid Flex
Palm top DVD	IVH 6 Layers	Buildup 8 Layers	Buildup 8~12 Layers
Car-Navigation	IVH 4~6 Layers	Buildup 6~8 Layers	Buildup 6 Layers
Note type PC	Buildup 6-10 Layers	Buildup 4-8 Layers	Buildup 4 Layers
Digital TV sets	Ag PTH 6 Layers	Ag/Cu PTH + Buildup 6 Layers	Ag/Cu PTH + Buildup 6 Layers

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Components Embedded Requirement

	2000	2005	2010
Wearable Products	0%	C, R, L	Filter, LSI:2007
Mobile Audio Sets	0%	C, R, L	Filter, LSI:2007
Cellular Phone	0%	C:2002, R:2003 L, Filter:2005	LSI:2005~2008
DSC	0%	C, R, L	Filter, LSI
DVC	0%	C, R, L	Filter, LSI
Palm top DVD	0%	C, R, L, Filter & LSI	←
Car-Navigation	0%	—	—
Note type PC	0%	C, R, L & Filter	LSI
Digital TV sets	0%	C, R	L, Filter

Common Requirements for Jisso Technology

- Low Temperature Reflow Soldering
- Next Generation Conductive Adhesive

- Moisture absorption free packages
- Standardization of new semiconductor packages

- Reduction of PWB warpage

- Module components

- Low temperature soldering
- Repairable underfill

- Reduction of manufacturing-attributable faults to 0%
- Automatic quality information feedback

- Delivery of more advanced products at low cost

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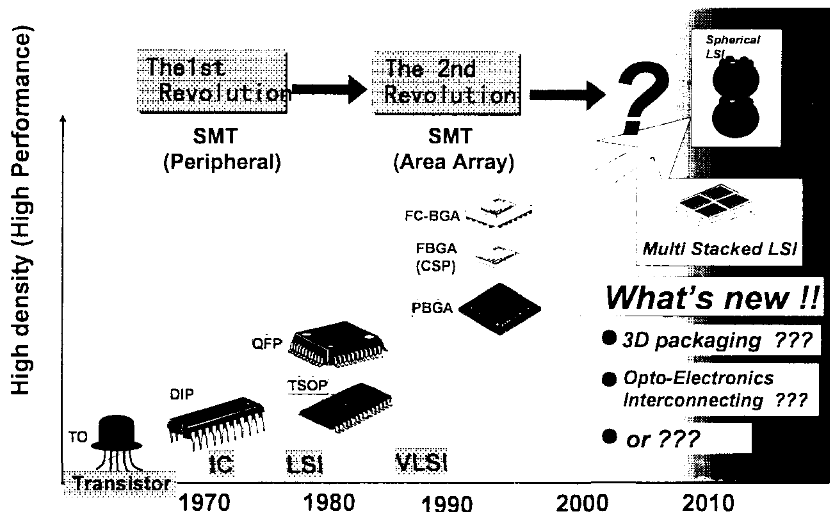
Trends of Semiconductor Package



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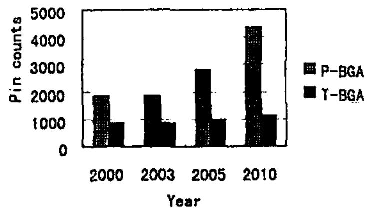
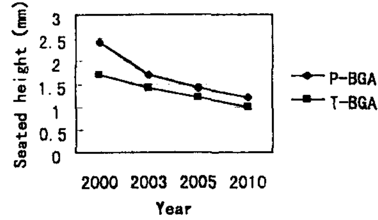
BGA Package

Package Type	Item	2000	2003	2005	2010
P-BGA	Max. Body Size (mm)	45	45	45	45
	Min. Pin Pitch (mm)	1.0	1.0	0.8	0.65
T-BGA	Max. Body Size (mm)	45	45	45	45
	Min. Pin Pitch (mm)	0.8	0.8	0.65	0.5

■ Maximum Pin Counts



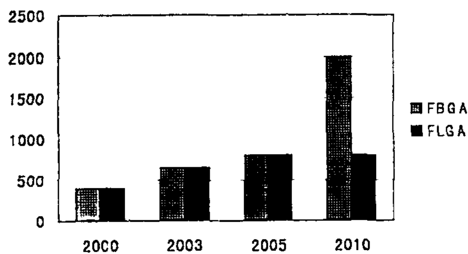
■ Minimum Seated Height



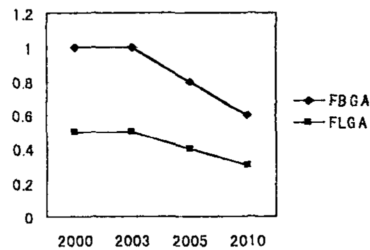
FBGA/FLGA Package

Package Type	Item	2000	2003	2005	2010
FBGA	Max. Body Size (mm)	21	21	21	21
	Min. Pin Pitch (mm)	0.5	0.4	0.3	0.15
FLGA	Max. Body Size (mm)	21	21	21	21
	Min. Pin Pitch (mm)	0.5	0.4	0.3	0.3

■ Maximum Pin Counts



■ Minimum Seated Height



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Issues for Developing Finer Pitch FBGA

(0.15 to 0.3 mm pitch)

- **Packaging Technology**
- **Solder Ball Formation Technology**
- **Socket Technology**
- **Printed Circuit Board**
- **Mounter and Mounting Technology**
- **Low Cost Material & Process**

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Wire Bonding Technology

Item	2000	2003	2005	2010
Bonding Method	Ball	←	←	←
	Wedge	←	←	←
Min. Pad Pitch (μ m)	50	40	35	20
Typ. Wire Diameter (μ m)	23	20	15	10
Wire Material	Au	Au, Alloy	Au, Alloy, Cu	←
Pad Material	Al	←	Al, Cu	←
Position Precision(μ m)	±3.5	±3.0	±2.0	±1.0
L/F Min. Inner Pitch (μ m)	160	140	120	100
Interposer Min. Pitch (μ m)	100	←	80	50

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Issues for Developing Finer WB Technology

(20 to 40 μm pitch)

- **Finer Pitch Bonding Technology**
- **Wire Bonder for Finer pitch**
- **Wire & Capillary for Finer Pitch**
- **Cu Wire Bonding Technology**
- **Encapsulation Technology for Finer Pitch**
- **Finer Pitch Probe Technology**
- **Low Cost Material & Process**

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Flip Chip Technology

Item	Pad Location	2000	2003	2005	2010
Min. Pad Pitch (μm)	Peripheral	80	60	40	20
	Area Array	200	150	100	70
Min. Bump Diameter (μm)	Peripheral	40	30	20	10
	Area Array	100	75	50	35
Bump Material	Peripheral	Au	←	←	←
		Sn-Pb	Sn-Ag	←	←
	Area Array	Pb-Sn	Sn-Ag	←	←
Pad Material	Peripheral	Al	←	Al,Cu	Cu
	Area Array	Al	←	Al,Cu	Cu

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Issues for Developing Finer FC Technology

(20 to 40 μm pitch)

- **Finer Pitch Bump Formation Technology**
- **Highly Reliable Bump Connection Technology**
- **Under-fill Technology for Narrower Space**
- **Repairable Under-fill Technology**
- **Finer Pitch Probe Technology for Grid Array**
- **Finer Pitch Interposer Technology**
- **Low Cost Material & Process**

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Elimination of Lead (Pb-free)

Subject			2000	2003	2005	2010
Solder Plating (Lead Frame)	Cu Alloy Frame	Material	Ni/Pd Sn-Bi Sn-Ag	Ni/Pd Sn-Bi Sn-Ag Sn-Cu	←	←
		Usage ratio	Partially	50%	100%	100%
	Fe-Ni Frame	Material	Sn-Bi Sn-Ag	Sn-Bi Sn-Ag Sn-Cu	←	←
		Usage ratio	Partially	50%	100%	100%
Solder Ball (External Terminal)		Material	Sn-Ag-Cu	←	Sn-Ag-Cu Su-Cu	←
		Usage ratio	Partially	50%	100%	100%
Package Heat Resistance (°C)		Reflow	250~260	←	←	←
		Flow	250~265	←	←	←

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Pb-free Issues to be developed

■ Die bonding material at high temperature (300℃ or higher) instead of Pb-Sn solder for high power devices
■ High melting solder ball (300℃ or higher) instead of Pb-rich solder for Flip Chip Bonding
■ Package heat resistance improvement for reflow temperature at 260℃ or higher

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Minimum Size of Electronic Components

Component	Item	2000	2005	2010
C/R/L	Mainstream Size (mm)	1.0 x 0.5 (1005)	0.6 x 0.3 (0603)	0.6 x 0.3 (0603)
	Advanced Size (mm)	0.6 x 0.3 (0603)	0.4 x 0.2 (0402)	0.4 x 0.2 (0402)
Ta Capacitor	Minimum Size (mm)	1.6 x 0.8 (1608)	1.6 x 0.8 (1608)	1.0 x 0.5 (1005)

C/R/L : Laminated chip capacitors, Chip square resistors, Chip inductors
Ta Capacitor : Chip Tantalum Electrolytic capacitors

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Δ

Pb-free of C/R/L Components

Item		2000	2005	2010
Pb-free Terminal plating		Sn	Sn	Sn
Pb-free Compliance (%)		70	80	100
Reflow solder heat tolerance	Mainstream	260 / 2	260 / 2	260 / 2
	Harsh	270 / 2	270 / 2	270 / 2

Note : Reflow solder heat tolerance shows
Maximum temperature (℃) / Number of reflow cycles.

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Pb-free of Electrolytic Components

Item			2000	2005	2010
Pb-free Terminal plating			Sn, Sn-Ag	←	←
Pb-free Compliance (%)			95	100	←
Reflow solder heat tolerance	Ta	Mainstream	260 / 2	260 / 2	260 / 2
		Harsh	260 / 2	260 / 2	260 / 2
	Al	Mainstream	240 / 1	240 / 1	240 / 1
		Harsh	240 / 2	240 / 2	240 / 2

Note : Reflow solder heat tolerance shows
Maximum temperature (℃) / Number of reflow cycles.

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Summary

■ Japan Jisso Technoly Roadmap 2001 (JJTR2001) was published by JEITA in April 2001.
■ Future electronic products request further higher assembly technology (ex. Finer pitch packages & components, 3D assembly, *etc.*) to reduce size and improve performance of the electric products.
■ For LSI Packages, finer ball pitch technology and finer chip connection technology will be developed.
■ For electric components, further size reduction will be developed.
■ For Jisso (assembly) machine, finer pitch assembly and short tact time technology will be developed.

■ Mr. Utsunomiya will present PCB roadmap next.

Appendix

■ JJTR 2001

Please contact below address, if you are interested in JJTR 2001.

Web. :
http://www.jeita.or.jp/english/public/data/book09.htm
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