# 플립칩용 UBM (Under Bump Metallurgy)연구의 최근동향
## Recent UBM (Under Bump Metallurgy) Studies for Flip Chip Application

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## Abstract

This paper presents several UBM (Under Bump Metallurgy) systems which are currently used for wafer level solder bumping technology. The advantages and disadvantages of each UBM are summarized from the point of view of process compatability and interface morphological stability.

## 1. Introduction

Flip chip solder bump interconnection provides a very attractive solution for high-density packaging with excellent advantages such as small-size, high I/O capability, quick and easy assembly, and good electrical performance. For the preparation of solder bumps on a wafer, the application of multi-layer thin films is necessary to provide adhesion to the chip metallization, a solder diffusion barrier and a solder wettable layer. Fig.1 shows the schematic diagram of these multi-layer thin films called collectively the UBM (Under Bump Metallurgy). Common choices for each functional layer are summarized in Table I. To select a proper UBM system, the following issues should be addressed: (1) The stress of UBM should be optimized to avoid film delamination, chip/UBM failure, or Si cratering. (2) The processability depending on solder deposition method must be considered. (e.g. selective etching for plating method and oxide prevention layer for stencil printing method.) (3) The understanding of UBM/solder IMC growth behavior during process and usage is needed especially for Pb-free and fine-pitch interconnection. (4) The UBM structure should serve as an effective diffusion barrier between chip pad and solder bump. (5) The electrical contact resistance of UBM/solder should be minimized. (6) The metallurgy and the deposition method should be as simple as possible for the process cost down.
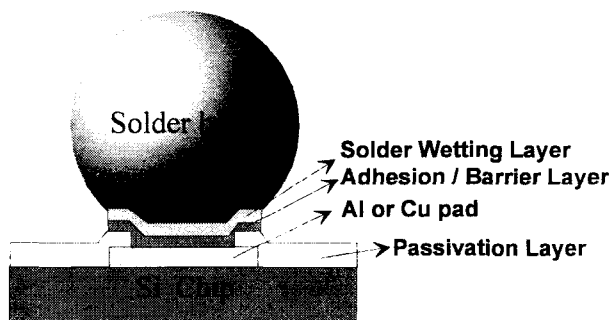


Fig.1 UBM(Under Bump Metallurgy) Structure

Table I. UBM Deposition Systems

| Function | Common Choices |
|---|---|
| adhesion/diffusion barrier layer | Cr, Ti, TiW |
| intermediate/buffer layer | Ni(V), Cr-Cu, Ni-Cu |
| solder wettable layer | Cu, Ni(V), Au |

# 2. UBM Systems

## 2-1. Ti(W)/Cu/electroplated Cu

The TiW/Cu/electroplated Cu UBM is one of the most commonly used metallurgy structure for electroplated bumping process. TiW (10Ti-90wt%W) layer is known to have better diffusion barrier property than Ti or Cr. Normally, more than 5 $\mu$m thick Cu is needed to avoid total Cu consumption which may cause the solder bump detachment by IMC growth during the process or usage. The reported disadvantages of this UBM are: First, the thick Cu-Sn IMC layer can cause stress induced crack site between soft solder and hard IMC. Secondly, the Si cratering was detected in some reports. However, this UBM is still one of the most commonly used UBM especially for electroplating bumping process because its process is well established and is suitable to other plated bumping material. Numerous studies have been reported on Cu and Sn containing solder interface. Double layered $Cu_6Sn_5$ and $Cu_3Sn$ IMC phases can be seen at the interface in normal liquid state solder reflow or solid state aging condition. Generally, the $Cu_6Sn_5$ IMC is the first forming phase between Cu and solder because it has the highest driving force [1] and lower activation energy than $Cu_3Sn$ in normal reflow temperature range [2-4]. The shape of $Cu_6Sn_5$ IMC appears so-called scallop-like grains in the liquid solder reflow condition. The $Cu_3Sn$ IMC is formedetween Cu and $Cu_6Sn_5$ if the Cu supply is not limited [5]. The scallop-like major $Cu_6Sn_5$ IMC are shown in Fig.2 (a) and (b) which are with eutectic Pb/63Sn and Sn/3.5Ag respectively.



TiW / Cu / electroplated Cu UBM

Cr / Cr-Cu / Cu UBM

NiV / Cu UBM
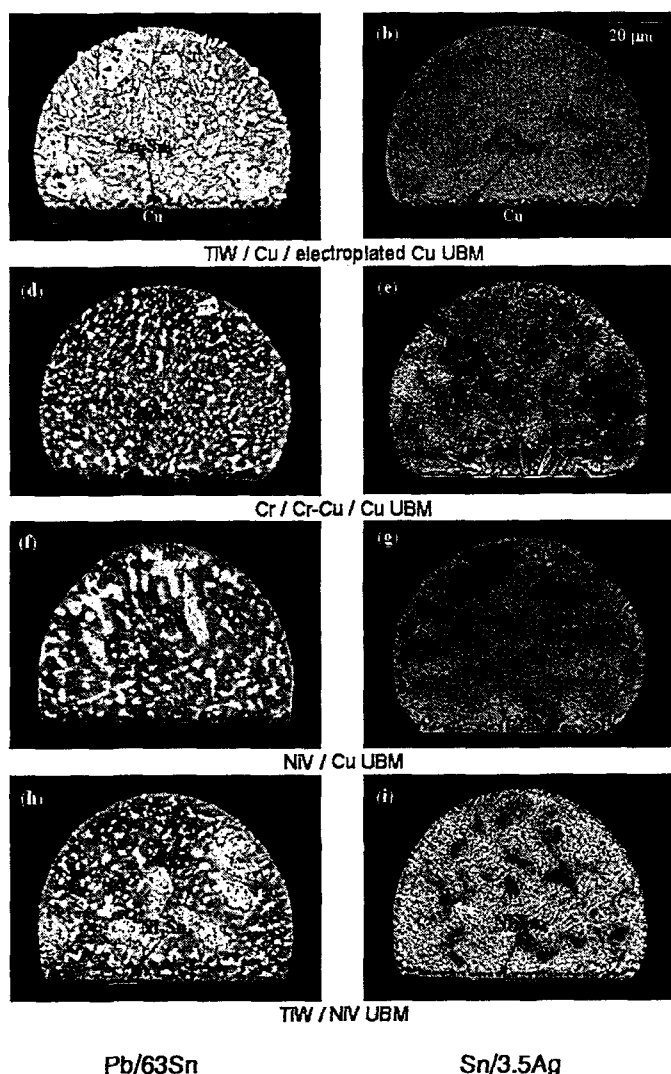
TiW / NiV UBM

Pb/63Sn                    Sn/3.5Ag

Fig.2 Cross-sectional SEM images of eutectic PbSn and SnAg solder bumps on various UBM systems after 1 reflow

## 2-2. Electroless Ni/Au

The electroless Ni/Au is currently used for stencil printing method. The main advantage of this UBM is that it is low cost process using wet-chemical deposition without vacuum and lithography process. The slow reaction rate of Ni to solder is also favorable factor. However, it has a limitation for fine-pitch application (less than 100 $\mu$m pitch), higher internal stress than Cu is also seriously considered to avoid Si cratering issue [6].

## 2-3. Cr/Cr-Cu/Cu

When the flip chip interconnection method, C4 (Controlled collapse chip connections), was first introduced by IBM, the thin-film multiplayer Cr/Cu/Au UBM was used for high Pb content solder. The Cr was used as an adhesion layer, the Cu was adopted as solderable layer, and the final Au flash was used to inhibit surface oxidation. However, the following studies revealed that the solder has a tendency to dewet from the Cr surface when the Cu layer is totally consumed by Cu-Sn IMC growth [7, 8]. In that reason, the phased CrCu layer by evaporation was introduced between Cu and Cr layers, and was expected to serve as an adhesion enhancement layer by lock-in effect [9]. This UBM has been reported to have good interface stability with high Pb content solders Pb/5Sn and Pb/3.5Sn, but recent studies reported that the phased CrCu layer with Pb/63Sn and Sn/3.5Ag solder also showed the Cu-Sn IMC spalling after long time reflow, and it may cause dewetting of solder [10-12].
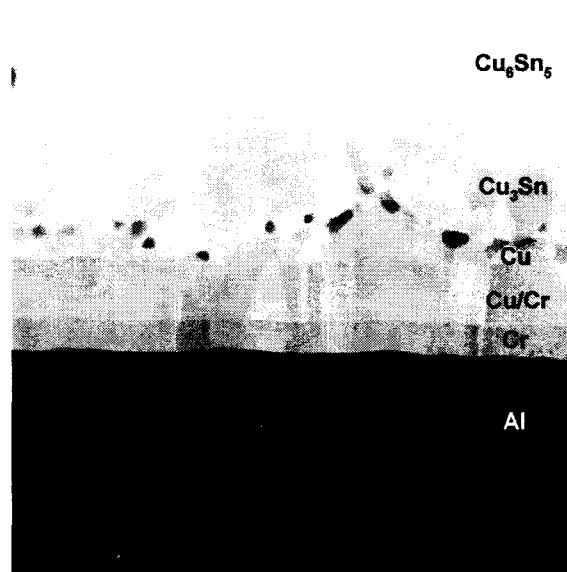


Fig.3 Low magnification High Angle Annular Dark Field (HAADF) STEM image of Cr/Cr-Cu/Cu UBM with Pb/63Sn solder after 5th reflow

## 2-4. Ni(V)/Cu

The Al/NiV/Cu UBM system was introduced by Delco Electronics and is used for screen printed solder bumps [13]. The 7 - 8 wt.% V is added to Ni in order to increase the magnetron sputtering yield because the pure Ni is ferromagnetic material. The basic idea of Ni containing metallurgy in UBM structure is that the Ni forms IMC with Sn, but the IMC growth rate is slower than the most commonly used metallurgy Cu. In this UBM, Al was used as an adhesion layer to Al pad and passivation layer (oxide, BCB, or polyimide material), NiV is introduced as a buffer layer to inhibit Cu-Sn IMC spalling and dewetting issue, and the final Cu is used as solderable surface. *Liu et al.* reported stable adhesion between $Cu_6Sn_5$ IMC and Ni(V) using screen printed Pb/63Sn solder bump [14], and the similar Al/Ni/Cu UBM structure showed good interface stability in our previous UBM investigations using plated eutectic PbSn [15] and eutectic SnBi bumps as well [16].

## 2-5. Ti(W)/Ni(V)

This TiW/NiV UBM is a modified UBM from Toshiba UBM for electroplated Pb/63Sn and Sn/3.5Ag bumps [17, 18]. The basic concept of this UBM is to use slower IMC growth rated Ni layer instead of Cu and to slow down the interfacial reaction rate. And they reported that Ti 0.1 μm/ Ni 1 μm UBM structure showed good interface stability and bump shear strength using electroplated Pb/63Sn.

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## 3. Summary

Real joint failure mechanism analysis of flip chip assemblies exposed to the thermal cycling or power loading is very complicated, and the failure modes are different depending on board material, die size, board surface finish, and underfill condition. However, the reported flip chip joint failure sites are mostly concentrated on chip-side UBM [19-21]. Fig. 3 shows the typical failure modes of flip chip assembly. Cracks are commonly observed between hard IMC and soft solder material. Therefore, the thick IMC layer or the exposure of non solder-wettable layer by excessive reaction should be carefully controlled. Extensive UBM studies are still required, especially for high Sn-content Pb-free solder flip chip application.
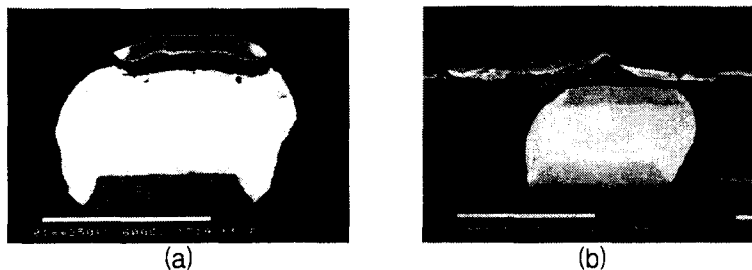
(a)  (b)

Fig.4 Flip Chip Failure Modes (a) Crack between chip-side UBM
and solder (b) Si cratering

## Acknowledgements

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