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Rapid thermal Annealing에 의한 300mm Polished 및 Epitaxial 실리콘 웨이퍼의 슬립 형성
(Slip Formation of 300mm Polished and Epitaxial Silicon Wafer Annealed by Rapid Thermal Annealing)

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Abstract

Slip generation on 300mm polished and epitaxial wafer was reviewed after rapid thermal annealing (RTA). In addition, wafers which were epitaxial heat treated without epi layer deposition also studied. In the RTA system with three supporting pins, slip was produced above 1150°C for polished wafer while it was produced above 1100°C for p/p- and p/p+ epitaxial wafer. The length and density of slip for epitaxial wafer was much higher than that for polished wafer. The deposition of low temperature oxide with 4000Å in thickness on the epitaxial wafer backside does not lessen slip formation. The slip generation in 300mm polished and epitaxial wafers annealed by RTA strongly depends on annealing temperature and annealing time; i.e., higher annealing temperature and annealing time of RTA leads to higher length and density of slip.

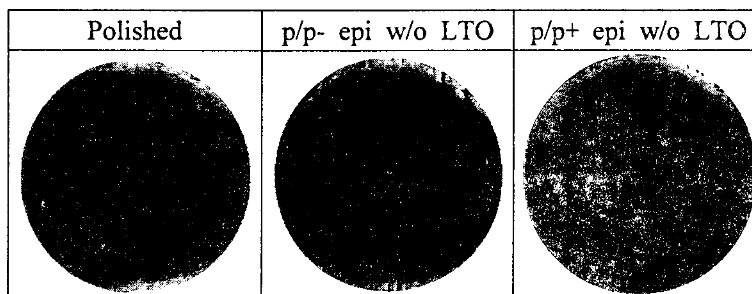

Fig. shows X-ray topography images of rapid theramal annealed wafers. Conditions were ramp up/down rate 50℃, annealing time 60sec, annealing temperature 1150℃, Ar ambient.