Dynamic Characteristic Analysis of SSSC based on Multi-bridge PWM Inverter

Byung-Moon Han, Hee-Joong Kim, Seung-Taek Baek
School of Electrical & Information Control Engineering
Myongji Univ., Yongin 449-728, Korea

Abstract - This paper proposes an SSSC based on multi-bridge inverters in PWM scheme. The proposed system consists of 6 H-bridge inverter modules per phase. The dynamic characteristic of proposed system was analyzed by simulation with EMTP codes, assuming that the SSSC is inserted in the 154-kV transmission line of one-machine-infinite-bus power system. The feasibility of hardware implementation was verified through experimental works with a scaled-model. The proposed system can be directly inserted in the transmission line without coupling transformers, and has flexibility in expanding the operation voltage by increasing the number of H-bridges.

Keywords: STATCOM(Static Synchronous Compensator), SSSC(Static Synchronous Series Compensator), GTO(Gate Turn-Off thyristor), PWM(Pulse Width Modulation)

I. INTRODUCTION

STATCOM was a first FACTS device using voltage source inverter with GTO, which is connected parallel with the bus needed for compensation. SSSC has same configuration of power circuit as STATCOM, but different configuration of control. SSSC injects voltage in series with a transmission line to control the voltage across the transmission line.[1][2]

In order to increase operation voltage of the many GTOs are connected in series. Series connection of GTO is proven technology. However, still there is restriction in maximum allowable number of units. Step-down transformers are normally used for properly matching the inverter operation voltage with the power system voltage.

Multi-level inverter was proposed to increase the system operation voltage avoiding series connection of switching devices. But multi-level inverter has complexity in formation of output voltage and requires many back-connection diodes. In order to complement this weak point, multi-bridge inverter composed of 5 H-bridge modules per phase was proposed by Peng for STATCOM application. The system operation was verified through experimental works with a scaled model.[3][4]

In this paper a multi-bridge SSSC composed of 6 H-bridge modules is proposed. The operation of proposed system is verified through simulations with EMTP codes.[5]

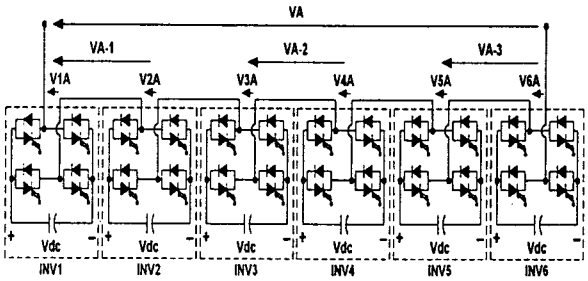
II. MULTI-BRIDGE SSSC

The proposed SSSC consists of 6 H-bridge inverter modules per phase as shown in Fig. 1a. The operational principle of one module can be explained using Fig. 1b. The ideal switch represents GTO switch and back-to-back connected diode.

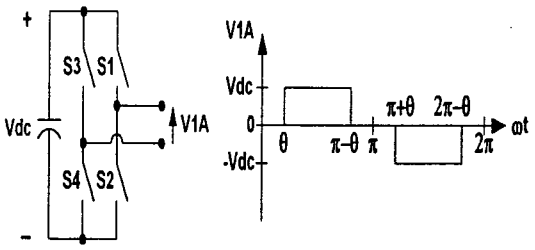
The output of each module has three states $+V_{dc}$, 0, $-V_{dc}$ depending on states of inverter switch S1-S4. Table 1 shows relationship between output voltage and switching state. By adjusting duration time, the output voltage can be adjusted.

Table 1. Switching pattern of multi-bridge invert

V1A	Switching State
V_{dc}	S1, S4 : on and S2, S3 : off
0	1) S1, S3 : on and S2, S4 : off 2) S2, S4 : on and S1, S3 : off
$-V_{dc}$	S2, S3 : on and S1, S4 : off



(a) Multi-bridge SSSC

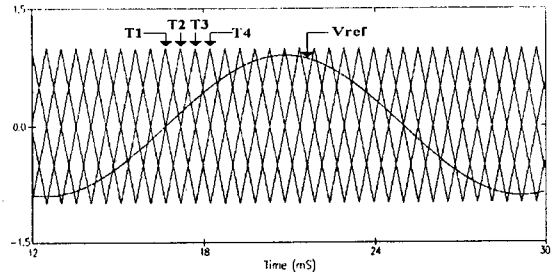


(b) Switching pattern

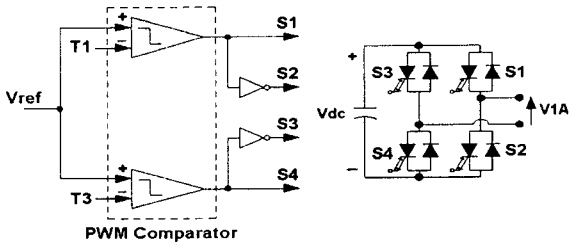
Fig. 1. Principle of multi-bridge inverter

Fig. 2 shows a principle of gate-pulse generation for PWM scheme. Fig. 2a shows four carriers and one reference signal to generate gate pulses for inverter module INV1 and INV2. The frequency of carrier T1, T2, T3, T4 is 480[Hz]. Each of four carriers has 90° phase shift each other. The reference signal V_{ref} has maximum value of 0.9 in per unit and has a sinusoidal waveform of 60Hz. Fig. 2b shows how to generate the gate pulses using reference and carrier. Carrier T1 and T3 are used as input to generate gate pulses for inverter module INV1 shown in Fig. 1a. Fig. 2c Shows four gate pulses supplied for switch S1, S2, S3, and S4, and output voltage of

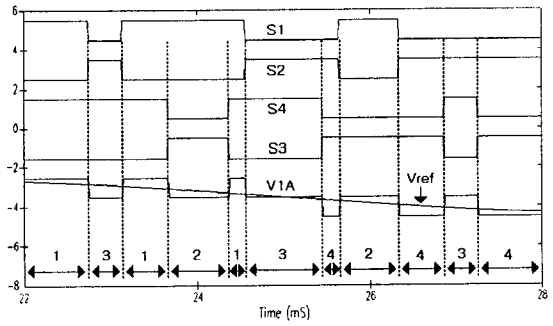
inverter module INV1 with the reference signal V_{ref}. In this figure the switching pattern of each switch S1 ~ S4 is properly operated according to the switching state in Table 1, where the number under waveforms means identification number for each switching state.



(a) Carrier and reference signal



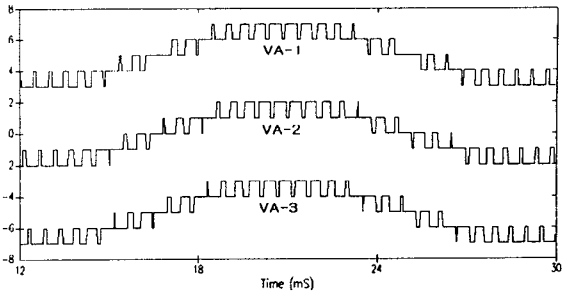
(b)Gate pulse generation scheme



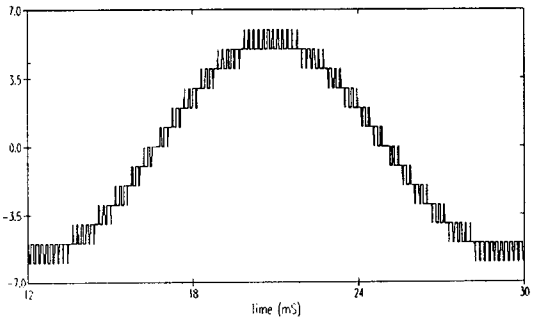
(c) Gate pulse and inverter output

Fig. 2. Principle of gate pulse generation

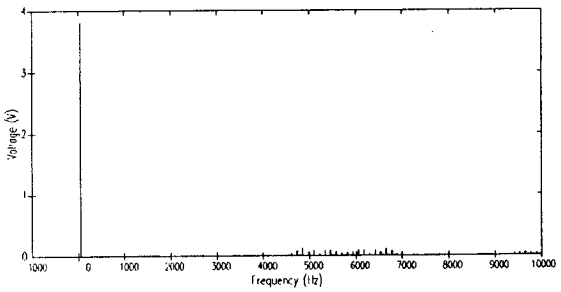
The gate pulses for inverter module INV2 can be obtained using same procedures as those for inverter module INV1except that carrier T1 and T3 is replaced with T2 and T4. It is simple to divide 6 inverter modules into 3 groups, like INV1-INV2, INV3-INV4, and INV5-INV6. Fig. 3a shows the output voltage waveforms of each inverter group, VA-1, VA-2, and VA-3. The dc voltage V_{dc} is 1.0 per unit. As explained before, the carrier shown in Fig. 2a is used to generate gate pulses for building up output voltage VA-1. Two sets of 4 carriers are needed to generate gate pulses for building up output voltage VA-2 and VA-3. These sets of carriers have 120° phase-shift each other. Fig. 3b shows total output voltage of three inverter groups, whose FFT analysis result is shown in Fig. 3c. Since each carrier has a frequency of 480[Hz] and there are 12 carriers, total output voltage VA has an equivalent switching effect of 6[kHz]. THD of output voltage VA is about 10.2% and spectra of harmonics are located around 6kHZ. Therefore, these harmonics can be easily filtered out.



(a) Output waveform of VA-1, VA-2, VA-3



(b) Output Waveform of VA



(c) FFT analysis of VA

Fig. 3. Output voltage build-up

Implementing multi-bridge inverter using currently commercialized GTO, the maximum rating for single H-bridge module without series connection of GTO can be roughly calculated as the following.

Rated DC voltage : $V_{dc} \cong$ 5kV
Rated output voltage : $V_o \cong V_{dc} \cong$ 5kV
Rated power : $S \cong 1/2 \cdot V_{dc} \cdot$ 2kA $\cong$ 5MVA

The above rating is too low to apply one module directly for FACTS devices. Therefore, series connection of inverters module is indispensable. Since the proposed multi-bridge inverter has 6 H-bridge modules, the system rating is calculated as the following.

Rated DC voltage : $6 \cdot V_{dc} \cong 30kV$
Rated output voltage : $V_o \cong V_{dc} \cong 30kV$
Rated power : $S \cong 3 \cdot V_{dc} \cdot 2kA \cong 30MVA$

The above rated output voltage is about 33.74% of phase voltage of 154-kV transmission line. This voltage is enough for satisfying the operation voltage of FATCS devices to be applied for the actual transmission line.

III. EMTP SIMULATION

Fig. 4 shows a single-phase simulation model for whole system. Other phases have same configurations. The power system is represented by one-machine-infinite-bus. The transmission line is modeled with a reactor considering only lumped line reactance.

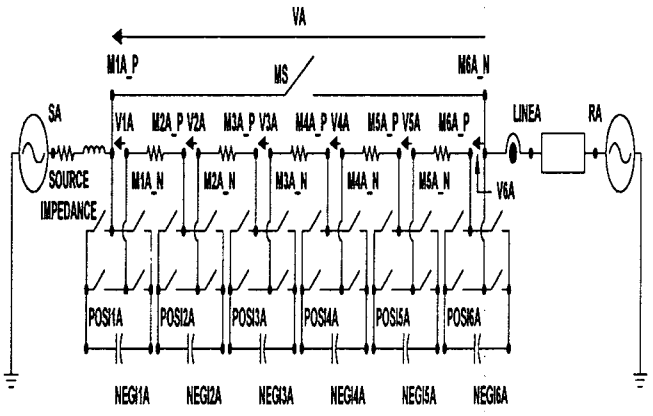


Fig. 4. Simulation model for whole system

Table 2. Simulation line parameter

Base voltage	154[kV]
Base power	400[MVA]
Source frequency	60[Hz]
Line inductance	1.56[pu]
Power angle	30°

The circuit parameters used in simulation are shown in Table 2. All values in simulation results are represented in per unit based on the base values in Table 2.

Fig. 5 shows a controller used for simulation of SSSC with multi-bridge PWM inverter. Since the multi-bridge inverter has a separate dc capacitor for each phase, separate control is needed for each phase.

In simulation controller the line current is measured and sent to the phase-lock loop. The phase-lock loop generates angle signal θ synchronized with the line current. The angle θ is properly adjusted for each phase. Reference value of compensation voltage V_q^* is multiplied by gain K to calculate V_{dc}^*. Reference dc voltage V_{dc}^* is compared with actual dc capacitor voltage of each phase separately. The error voltage is passed through PI controller and limiter to obtain firing angle, which is corrected by phase-lock angle θ. V_{dc}^* is determined by 0.045pu. Measured actual dc voltage is calculated by averaging dc voltages of 6 H-bridge modules. The output signal of PI-Controller is multiplied with mode sign of V_q^*. Mode Sign is used to determine SSSC operation in C-Mode or L-Mode. In simulation mode sign is +1 for C-mode and –1 for L-mode. C-Mode means that the phase angle of injected voltage by SSSC is leading to that of the line current, while L-Mode means that the phase angle of injected voltage by SSSC is lagging to that of the line current.

Synchronized signal with 3-phase line current, control signal for dc capacitor voltage, and mode sign are combined together to generate the reference signal for inverter firing angle. There are 6 sets of controllers which supply gate signals for 3 sets of 6 H-bridge modules.

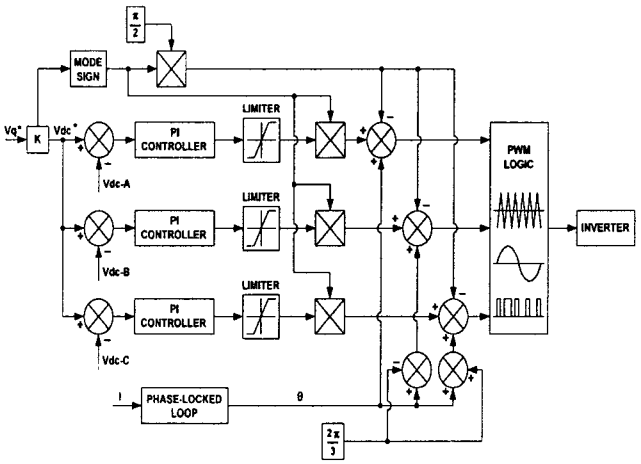
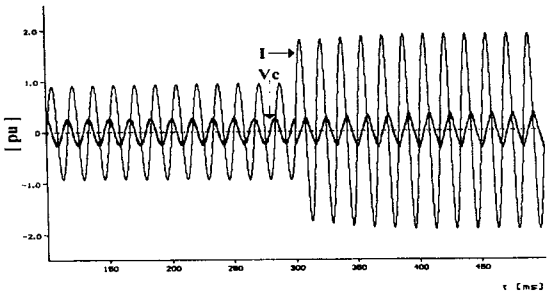


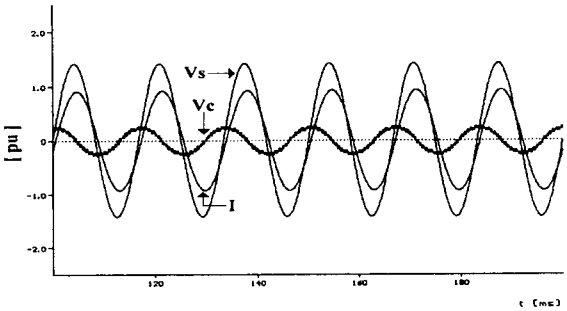
Fig. 5. Simulation controller

The scenario considered in this simulation is as the following. SSSC is on standby state from 0~50ms. The mechanical switch MS is ON state and the switches in multi-bridge inverter are OFF state. During 50ms~300ms the mode Sign is set by –1 and SSSC operates in L-Mode. During 300ms~550ms the mode Sign is set by +1 and SSSC operates in C-Mode.

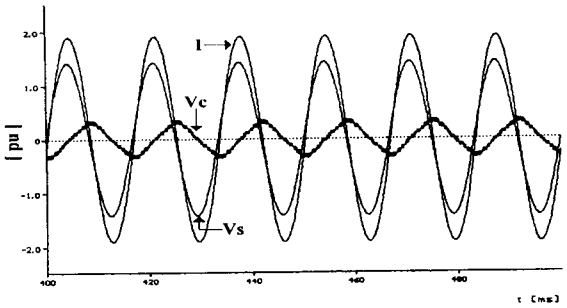
Fig. 6 shows simulation results for dynamic performance analysis of proposed SSSC. Fig. 6a shows inverter injection voltage and line current during transition from L-Mode to C-Mode. The transition is completed within half cycle of power frequency. Fig. 6b shows source voltage, inverter injection voltage, and line current in L-mode when SSSC operates in L-mode with inductive reactance of 0.82pu. Fig. 6c shows source voltage, inverter injection voltage, and line current in C-mode when SSSC operates in C-mode with inductive reactance of 0.51pu. Fig. 6d shows DC capacitor voltages, which are used as input for the controller. Fig. 6e shows variations of the active power Pr and the reactive power Q_r at receiving end. Transmission line supplies active power P_r of 0.93pu and reactive power Q_r of -0.35pu when SSSC operates in standby mode. Active power Pr decreases down to 0.64pu and reactive power Q_r decreases down to -0.21pu in L-mode respectively. Active power Pr decreases down to 1.28pu and reactive power Q_r decreases down to -0.55pu in C-mode respectively.



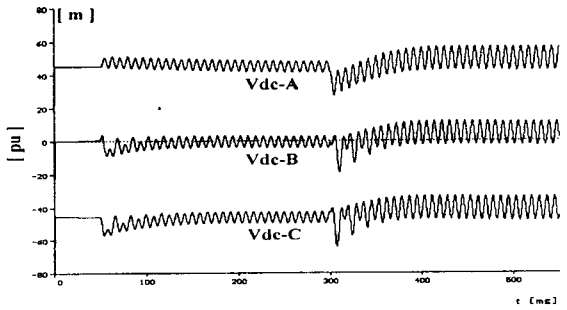
(a) inverter voltage and line current



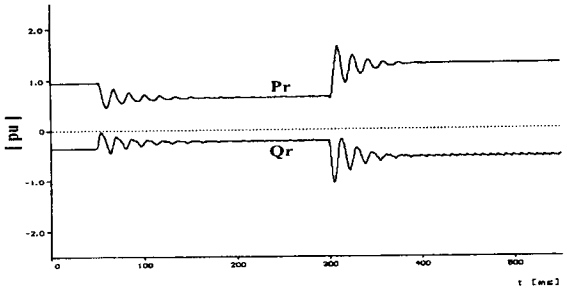
(b) source voltage, inverter voltage, and line current in L-Mode



(c) source voltage, inverter voltage, and line current in C-Mode



(d) DC capacitor voltage



(e) active and reactive power in receiving end

Fig. 6. Simulation results

IV. SCALED-MODEL EXPERIMENT

A hardware scaled-model has been built to confirm the simulation results and to verify the feasibility of actual system implementation.

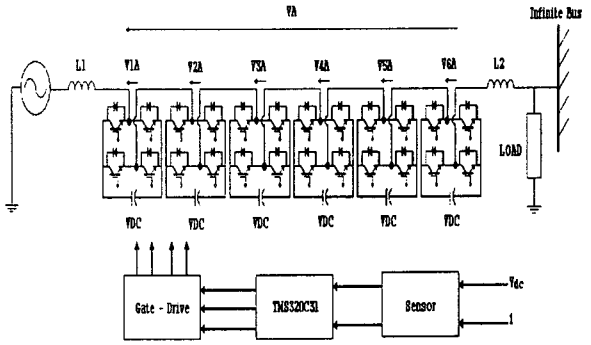
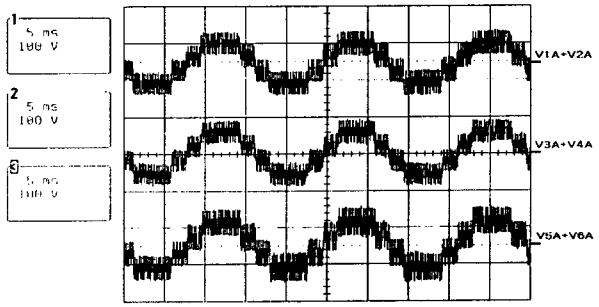


Fig. 7. Hardware configuration of scaled model

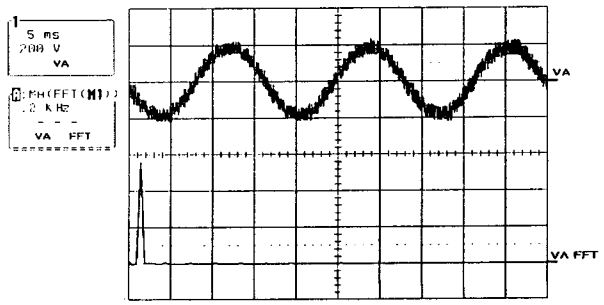
Fig. 7 shows the circuit diagram for the scaled model, which has 6 H-bridge modules. 24 single-type IGBT units per phase were used for the multi-bridge inverter. TMS320C31 was used for whole system control and pulse generation. The reference for gate pulse generation was determined by detecting zero-crossing point of the line current. The firing angle of each inverter module is determined with respect to this reference. The dc voltage of each inverter module is controlled independently. Table 3 shows circuit parameters for the scaled model.

Table 3. Scaled model circuit parameters

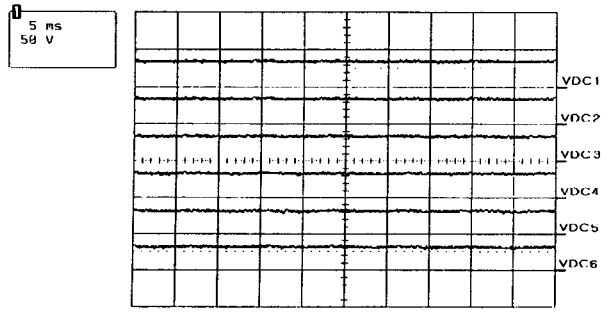
Source voltage	200[V]
Line model L1	15[mH]
Line model L2	28[mH]
Load	50[Ω]
DC link capacitor	2200[uF]



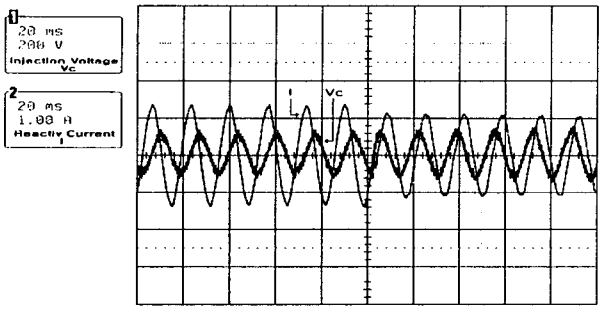
(a) V1A+V2A, V3A+V4A, V5A+V6A voltage



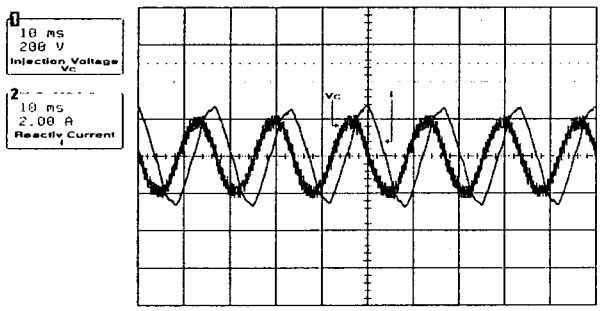
(b) voltage Va & FFT



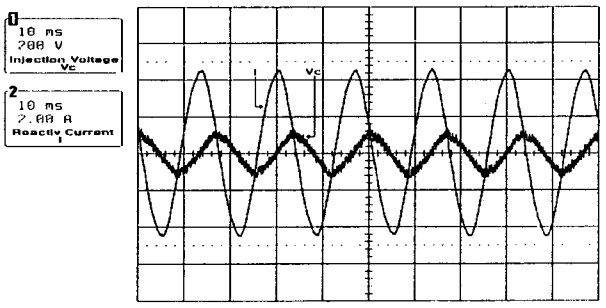
(c) DC capacitor voltage of each module



(d) injecting voltage and reactive current



(e) injecting voltage and reactive current(lag)



(f) injecting voltage and reactive current(lead)

Fig. 8. Experiment results with scaled model

Fig. 8 shows the experimental results for the scaled model. Fig. 8a shows the output voltage waveforms of each inverter group, VA-1, VA-2, and VA-3, which are very close to the simulation results. Fig. 8b shows the total output voltage of three inverter groups and its FFT analysis result. The output waveform is almost sinusoidal, although there is some high frequency noise. Fig. 8c shows variation of the dc capacitor voltage, in which each voltage is almost equally distributed. Fig. 8d shows variation of the injecting voltage and the reactive current, when the proposed SSSC has a sudden state change from supplying lagging reactive power to supplying leading reactive power. Transition from lagging to leading can be completed within one cycle of power frequency. Fig. 8e shows the expanded waveform of Fig. 8d in L-mode, while Fig. 8f shows the expanded waveform of Fig. 8d in C-mode.

V. CONCLUSION

This paper proposes an SSSC composed of multi-bridge inverter, which has 6 H-bridge modules per phase. Dynamic operation of the proposed SSSC is analyzed through computer simulations with EMTP and experimental works with the hardware scaled-model.

The contribution of this paper is to propose a new SSSC to be connected in the transmission line directly without transformer. The proposed system has flexibility in optimizing the operation voltage required in power system by adding or subtracting number of bridges. The developed simulation model and hardware scaled-model can be utilized to obtain the engineering data for the actual system.

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B. Han received the B. S. degree in electrical engineering from the Seoul National University, Korea in 1976, and the M. S. and Ph.D. degree from Arizona State University in 1988 and 1992, respectively. He was with Westinghouse Electric Corporation as a senior research engineer in the Science & Technology Center. Currently he is an associate professor in the Department of Electrical Engineering at Myongji University, Korea. His research interests include the high-power power electronics and FACTS.

H. Kim was born in Seoul, Korea. He received the B. S. and Master degrees in electrical engineering from the Myongji University in 1997 and 1999 respectively. He is currently a Ph. D. candidate in the Myongji University. His research interests include power electronics application for FACTS and Custom Power.

S. Baek was born in Seoul, Korea. He received the B. S. and Master degrees in electrical engineering from the Myongji University in 1997 and 1999 respectively. He is currently a Ph. D. candidate in the Myongji University. His research interests include power electronics application for FACTS and Custom Power.