Design Optimization for High Power Inverters

D. Schröder Chair of Electrical Drive Systems Technical University of Munich Germany H. Kuhn
Chair of Electrical Drive Systems
Technical University of Munich
Germany

ABSTRACT

This paper focuses on a network model for GCTs which can be used to investigate high power circuits with or without using RC-snubbers. The series connection of GCTs is commonly applied in the high power inverter field. Here expensive and space—consuming snubbers are applied, to overcome the problem of an asymmetric distribution of the blocking voltage among the single GCTs. As an alternative to large snubbers, a new active gate drive concept is proposed and investigated by simulation.

Key words:

GCT-model, series connection, active gate drive

1 INTRODUCTION

The GCT (Gate Commutated Thyristor) is a special structured GTO including a n-doped buffer layer to enable high voltage blocking with a relatively short low doped drift zone. Instead of emitter shorts, a transparent anode (very thin p⁺-layer) is used to reduce the injection efficiency of the anode. Both measures result in a good trade off between static and dynamic losses. The GCT can be hard driven, i.e. the gate current rise exceeds 1000 A/ μ s. Operating in this mode, the GCT withstands higher loss power densities compared to conventional GTOs. Consequently it is even possible to omit the RC-snubber [1]. If GCTs without snubbers are chosen for high power systems, the total amount of losses for common switching frequencies will be smaller than using HV-IGBTs [2]. In [3] and [4], a physically based GCT model for the network simulator Saber® was presented. After describing this model briefly, simulated transients, based on this model, are compared to measured ones in section 2. Section 3 provides investigations regarding the series connection of GCTs. The results lead to an active gate drive concept to overcome the asymmetry of the blocking voltages without or at least with a small scale snubber. This will be discussed within section 4. The conclusion in section 5 completes the paper.

2 MODEL VALIDATION

2.1 The GCT Model

The physical model, presented in [3],[4], is implemented in Saber MAST®, so that the main equations of semi-

conductor physics can be considered. Especially the excess charge carrier distribution in the wide low doped drift zone is described as accurately as possible according to its importance for the static and dynamic behaviour. To receive the spatial charge carrier distribution for every time step, the continuity equation for high level injection has to be solved numerically. For that, a one dimensional approach was chosen. This yields a good compromise between an acceptable effort on the one hand and a sufficient accuracy on the other hand. To reduce calculation time, the very effective numerical approach from [5] was taken. Instead of the commonly used ambipolar diffusion equation, a drift-diffusion approximation including electron-hole-scattering mobility by Mnatsakanov is implemented, to receive correct simulation results especially for low temperatures [6]. Moreover the buffer layer has to be modeled. The buffer is integrated into the drift zone module. In contrast to quasistatic approaches, convergence problems can be avoided. Furthermore it is possible to define lifetime profiles, e.g. for the buffer lifetime. In case of snubberless operation, the rise of the blocking voltage depends on device internal physics only. In addition to that the dynamic avalanche effect has to be considered according to the large influence on the transients.

2.2 Simulation Results vs. Experiment

Within [3] and [4], simulation results showed a good agreement with experiment. The influence of dynamic avalanche was also shown. But the fitting process of this model with approximately 15 relevant parameters (of ≈40), needs at least two turn off measurement results to find the parameter set. Meanwhile, the adaptation to new experimental transients results with a later version of a 3kA/4.5kV-IGCT was performed. The schematic for experiment and simulation can be seen from fig. 1. It is a simple buck converter with a clamped turn on snubber inductance. Here, the gate current was additionally measured, so that the delay time, i.e. the time between the decrease of the gate current and the begin of the voltage increase, is known exactly. From this, the excess charge concentration at the drift zone/p-base-junction can be adjusted precisely. With the dV/dt of the anode-cathode voltage, it is possible to estimate the high injection lifetime and together with the tail current, the anode-side hole injection into the buffer/drift zone.

Proceedings ICPE '01, Seoul

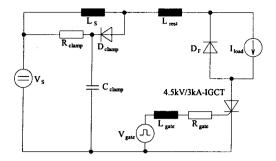


Fig. 1: schematic for measurement and simulation

This lead to a much easier and faster parameter fitting process (within some hours instead of days) because only one experiment is needed. Fig. 2 depicts the adaptation process in this case. Here, the solid lines represent the turn off transients (3kA vs. 2.8kV) of the measurement, the dashed lines that of the simulation (also in fig. 3, 4). Here V_{ac} is the anode–cathode voltage, I_a the anode current and I_g the gate current.

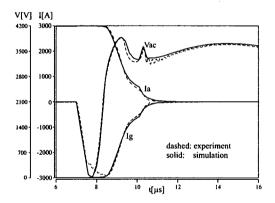


Fig. 2: snubberless hard turn off: 3kA vs. 2.8kV

After finding the parameter set, the calculations of the turn off processes for other currents were performed. From fig. 3, a good agreement with the experimental results can be seen.

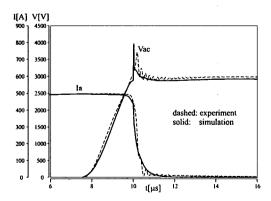


Fig. 3: snubberless hard turn off 500A vs. 2.8kV

According to the fact that the transients for 3kA (fig. 2) are influenced by dynamic avalanche, the parameter set had to be modified to a small degree. The second type of dynamic process is the switch on behaviour. From fig. 4, which depicts the turn on process of 3kA vs. 2.8kV, it can be verified that measurement and simulation results also match nearly exactly. The differences between the anode current curves after $t=12\mu s$ are caused by a not perfectly adapted diode model concerning the turn off behaviour of the free wheeling diode.

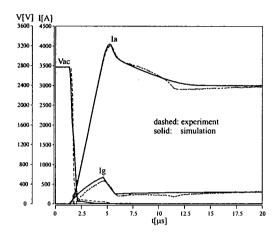


Fig. 4: turn on 3kA vs. 2.8kA

As the presented GCT model enables accurate calculations of the transient behaviour, it can be used to investigate the consequences regarding certain limits of more complex power electronic circuits with or without additional snubbers. This will be discussed for the case of series connection of GCTs in the subsequent section. Finally it is worth mentioning that in spite of the high accuracy, the simulation time of the presented calculations is very low (approximately 14 seconds with a Pentium III, 500MHz and Saber 5.0).

3 SERIES CONNECTION

This section deals with the series connection of GCTs to increase the system voltage of inverters [7]. Here, potential problems regarding the series connection will be analyzed. As mentioned in section 1, the main advantage of the GCT is the possibility of snubberless operation. This seems to be no problem if circuits with only one GCT per unit is considered. In case of more series connected GCTs per unit, an asymmetric distribution of the blocking voltage during and after the turn off process occurs. This unpleasant situation can be caused by

- 1. differences regarding the device geometries or the physical parameters of the single GCTs
- 2. time delays between the gate signals (turn off impulses)
- 3. different gate inductances
- 4. any combination of 1.-3.

It has to be noted that even small differences yield large effects. In fig. 5 two identical GCT elements (GCT_1,2) and two identical gate signals are assumed, but the gate inductance of GCT_2 is about 10% higher. From this figure it can be seen that the effect of asymmetry even for small differences can be simulated by applying the presented model. In contrast to that, the calculation with the standard GTO model of the Saber library, based on the lump charge approach [8], do not correspond to reality.

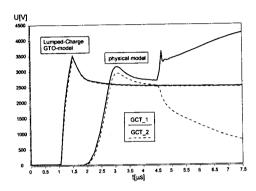


Fig. 5: simulated turn off process of two GCT with distinct L_g : physical model vs. lumped charge model

According to physical constraints of the dynamic process, the whole asymmetry arises not before the charge within the low doped drift zone is pulled out (for $t \ge 4.5 \mu s$ in fig. 5). To overcome this problem, RC snubbers are commonly applied. For this purpose, the amount of the snubber capacity can be chosen smaller than in the case of soft switching, but at least $1 \mu F$ seems to be obligatory to ensure symmetry. To show this, a buck converter consisting of three GCT elements in series (GCT_1,2,3), three free wheeling diodes, a clamped turn on snubber inductance, a remaining parasitic inductance and three turn off RC-snubbers due to fig. 6, is chosen. Here a load current of 3kA vs. a DC-link voltage of 6kV is switched.

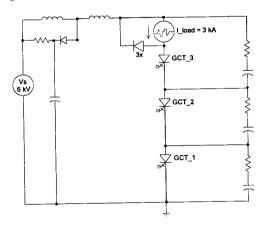


Fig. 6: simulation schematic of 3 GCTs in series

GCT_1 and GCT_2 and the corresponding gate drives are identical. GCT_3 stores more charge during the on state than GCT_1,2 according to a 5% higher lifetime au_H within the low doped drift zone. Furthermore the gate inductance of GCT_3 is about 10% higher than for GCT_1,2. Thus GCT_3 turns off slower than GCT_1,2. Although the distinction is not grave, GCT_1,2 will take the whole blocking voltage (3kV each) in case of snubberless operation. If the individual blocking voltage of the fastest GCT turns too high, the device may be damaged. This asymmetric behaviour can be seen in fig. 7, which depicts the simulation results with RC-snubber (dashed lines) and without (solid lines). Here a snubber capacity of $3\mu F$ is used yielding a symmetrical distribution of the voltages with a remaining difference of approximately 100V. In addition to that HV-capacities of some μF are expensive and need a large amount of space. Therefore an alternative concept will be discussed within the next section.

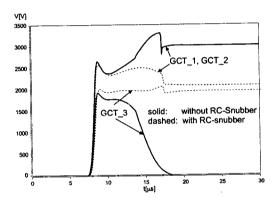


Fig. 7: turn off 3kA vs. 6kV: GCT-voltages with and without snubber

4 ACTIVE GATE DRIVE

4.1 The Concept and the Circuit

For voltage controlled IGBTs, active gate control circuits are commonly used to obtain symmetric behaviour [9]. Within this section a concept for an active gate control of the current controlled GCT is presented. The concept is based on an idea which is explained as follows. If there are n GCTs in series, then the ideal voltage drop for each GCT V_{GCT}(t) will be the total voltage across all GCTs $V_{tot}(t)$ divided by the quantity n. If the voltage drop of a certain GCT is larger than V_{tot}(t), i.e. GCT_i switches "too fast", an overvoltage $V_{\Delta}(t) = V_{GCT_{-i}}(t)$ - $V_{tot}(t)/n$ can be measured by voltage detection. This $V_{\Delta}(t)$ can be fed back and processed by a controller that supplies the gate with a short positive gate impulse, which is superposed to the regular negative turn off signal, in order to slow down this GCT_i. Although the characteristic of the GCT is rather complex, this idea leads to a simple proportional controller concept which is shown in fig. 8.

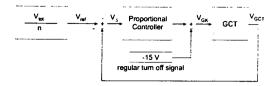


Fig. 8: active gate controller for one GCT

To realize this concept, a circuit was developed and investigated [10]. Fig. 9 depicts a block diagram with all components of this circuit for one representative GCT_{-i}. The circuit consists of n voltage detection units, n controller units, n linear amplifiers to supply the gates with enough current and the n on/off-modules. These blocks will be explained below.

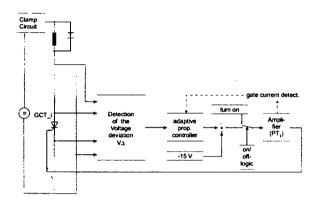


Fig. 9: block diagram of the active gate drive

First, it should be mentioned that all used models for the single components are chosen as realistic as possible. i.e. including offsets, bias currents, cut-off frequencies, delays and parasitic components. Second, the requirements have to be clarified, to obtain a gate drive that works as desired. In fig. 7 it can be seen that directly after the beginning of the voltage rise ($t\approx7.5\mu s$), the differences between the voltages are small (few volts). Since the gate current is approximately at its maximum at this time, the influence of the gate drive is large. Later, i.e. $t\approx 12\mu s$, the voltage deviations are very large, but the influence of the gate control vanishes according to the gate current which is almost zero at this time. Consequently, the voltage detection unit even have to act for voltage deviations of few volts. In addition to that a better stability of the control loop can be expected if the balancing action starts as early as possible. This can be ensured only if the signal propagation delay through the components is small enough. Moreover the overall cut-off frequency must be in the range of some MHz due to fast turn off process.

The voltage detection unit for GCT \perp i has to subtract $V_{tot}(t)/n$ from the actual voltage at the GCT \perp i. To subtract two voltages, circuits with operational amplifiers (OpAmps) are commonly used. But OpAmps are too slow here and yield wrong subtraction results ac-

cording to offsets, bias currents and time delays. Here, the two mentioned voltages are transformed into equivalent currents which are subtracted almost ideally at a node (Kirchhoffs Current Law) without any loss of time. As mentioned above, a proportional controller is used. But the amplification factor is not constant but depends on the gate current which is measured at the amplifier (see dashed arrow in fig. 9). This gate current is an indicator for the time status of the turn off process, i.e. if the process is at its beginning, at its end. or somewhere in between. The amplification factor starts from a maximum and decreases towards the end. "controlled" by the gate current. This adaptive controller yield a good performance and stability at the same time. The output amplifier is a linear amplifier consisting of p-channel and n-channel MOS-FETs that are switched parallel. They are driven by a Current-Controlled-OpAmp, which consists of bipolar transistors, and supplies the MOS-capacities with enough charge to avoid remarkable time delays. The gate-source voltage of the p-MOSFETs is proportional to the gate current I_q of the GCT and is used to adapt the controller (see above). With available components, e.g. OpAmps, MOSFETs, BJTs, JFETs, etc. an overall cut-off frequency of 3MHz can be achieved.

4.2 Simulation Results

As mentioned above, only realistic models are used, i.e. no ideal sources, transistors, OpAmps, etc., to obtain responsible predictions. Here the same situation as in section 3 (cf. fig. 6, 7) is assumed, i.e. the high injection lifetime and the gate inductance of GCT_3 are higher than of GCT_1,2. Fig. 10 depicts the corresponding simulation result for the anode-cathode-voltages.

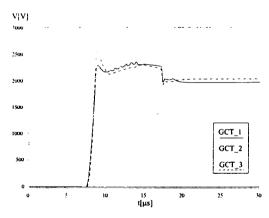


Fig. 10: turn off 3kA vs. 6kV: anode-cathode-voltages with active gate control

The asymmetry has almost vanished. The difference between the single voltages after the turn off process is smaller than in the case of applying RC snubbers (see fig. 7). Together with fig. 11, which depicts the gate currents of GCT_1.2.3, the compensation process can be seen clearly. The voltages begin to rise at $t\approx 7.5 \mu s$

and due to $V_{GCT_1.2}(t) - V_{tot}(t)/n > 0$, the compensation process slows down GCTs_1,2 (dotted lines). But GCTs_1.2 are slowed down too strong, so that GCT_3 (solid lines) is too fast now. This can be seen from the fact that the maximum of V_{GCT_3} exceeds that of $V_{GCT_1.2}$. Thus, $V_{GCT_3}(t) - V_{tot}(t)/n > 0$ and this will be compensated again. The turn off process ends and a small voltage deviation remain.

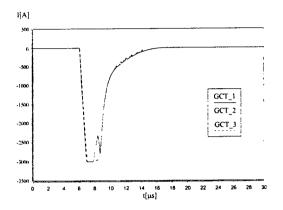


Fig. 11: gate currents with active gate control

4.3 Discussion

In section 4.2, it was proven that the active gate drive works as a favourable option. Here, a blocking voltage 2kV per GCT (6kV total) was chosen. But as it can be seen in section 2, one single GCT can withstand higher voltages ($\approx 3kV$). Then, a second peak after the maximum arises during turn off (see e.g. fig. 3 at $t=10\mu s$). This peak will occur if the electric field reaches the buffer layer before the anode current is equal to zero. This yield a very fast change of the voltage deviation V_{Δ} . In this case, an overall cut-off frequency of more than 100MHz is necessary to ensure correct operation. But such a restriction cannot be achieved with available components. Therefore a RC snubber is suggested, but the capacity can be very small ($\approx 30nF$). Fig. 12 shows the simulation results.

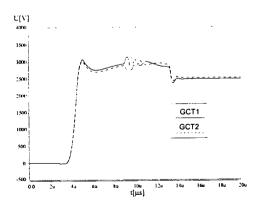


Fig. 12: voltages of 2 GCT in series with active gate and a "small" snubber: turn off 3kA vs. 5kA

In power systems, redundant elements are added often. This ensures secure operation if one GCT is damaged, i.e. shorted [7]. Thus the reference voltage is no longer $V_{tot}(t)/n$, but $V_{tot}(t)/n-1$ and the active gate drive circuit has to be extended to enable this mode.

5 CONCLUSION AND OUTLOOK

Within this paper a physical model was presented. Comparison with experiment yield a excellent agreement of the transients dynamic processes. The model was used for basic investigations on series connection of GCTs. A new active gate drive concept which enables snubberless, or at least small snubber operation, was presented. Within the next months, investigation to find a systematic algorithm for an optimal adjustment of the controller amplification is intended. Furthermore the circuit has to be extended to include the case that one redundant GCT is damaged. A practical realization and a succeeding validation is also planned, but this depends on a potential cooperation with industrial partners.

REFERENCES

- S. Klaka, M. Frecker, H. Grüning "The Integrated Gate-Commutated Thyristor: A New High-Efficiency, High-Power Switch for Series or Snubberless Operation", PCIM, Nürnberg, 1997
- [2] E. Krafft. A. Steimel. J. Steinke "Three-Level High-Power Inverters with IGCT and IGBT Elements Compared on the Basis of Measurements of the Device Losses", Proc. of EPE, Lausanne. 1999
- [3] H. Kuhn and D. Schröder "Circuit Simulation of Hard-Driven IGCT for Snubberless Operation using a Physically Based Model", Proc. of IPEC, Tokyo, 2000
- [4] H. Kuhn and D. Schröder "A New Validated Physically Based IGCT Model for Circuit Simulation of Snubberless and Series Operation", Proc. of IEEE IAS, Rome, 2000
- [5] D. Metzner, T. Vogler and D. Schröder, "A Modular Concept For The Circuit Simulation Of Bipolar Power Semi-conductors", Proc. of EPE, Brighton, 1993
- [6] A. Schlögl, T. Mnatsakanov, H. Kuhn and D. Schröder "Temperature Dependent Characterization of Silicon Power Semicondutors - A New Model Validated by Device-Internal Probing between 400K and 100K", Proc. of PESC, Kyoto, 1998
- [7] P. Steimer, H. Grüning, J. Werninger and D. Schröder, "State-of-the-Art Verification of the Hard Driven GTO Inverter Development for a 100 MVA Intertie", PESC. Baveno, 1996
- [8] C.L. Ma. P.O. Lauritzen, J. Sigg, "A Physics-based GTO Model For Circuit Simulation", IEEE PESC, Atlanta, 1995
- [9] C. Gerster. "Fast High-Power/High-voltage Switch Using Series-connected IGBTs with Active Gate-controlled Voltage-balancing", Proc. of IEEE APEC, Orlando, 1994
- [10] J. Biela, "Erstellung, Untersuchung und Implementierung von Konzepten zur aktiven Ansteuerung von seriengeschalteten IGCT-Bauelemente", Diploma Thesis, Universität Erlangen-Nürnberg in cooperation with Technical University of Munich, 2000