

# A Study on PFC of Active Clamp ZVS Flyback Converter

Tae-Young Choi\*, Jeong-Joon Ahn\*, Dong-Kyun Ryu\*, Woo-Suk Lee\*  
Chung-Yuen Won\*, Soo-Seok Kim\*\*

\*Sung Kyun Kwan University, \*\*Seoul National University of Technology

300 Chunchun-dong, Jangan-Ku, Suwon, 440-746, Korea

Phone +82-31-290-7169 Fax +82-31-290-7169

**Abstract**-- This paper analyzed PFC of active clamp ZVS flyback converter by adding two methods PFC (Power Factor Correction) circuit - two-stage and single-stage. The addition of active clamp circuit also provides a mechanism for achieving ZVS of both the primary and auxiliary switches. ZVS also limits the turn off  $di/dt$  of the output rectifier, reducing rectifier-switching loss and switching noise, due to diode reverse recovery.

As a result, the proposed converters have characteristics of the reduced switching noise and high efficiency in comparison to conventional flyback converter.

The simulation and experimental results show that the proposed converter improve the input PF of 300W ZVS flyback converter by adding single-stage, two-stage PFC circuit.

## 1. INTRODUCTION

Recently, the international activities for energy saving have been intensively executed. To keep in step with this trend, the adoption of the switching power conversion has been extensively expanded in the home appliance, such as T.V., lighting systems, computers and motor drive systems. However, conventional switching power systems usually include the full-bridge rectifier and large filter capacitor at their input stage. This initial solution produces significant harmonics, which cause the poor power quality and problems of public utility network, demanding an additional price to maintain the network. [1]

The conventional flyback converter has the loss increasing by switching, noise increasing and high switch stress. These disadvantages are improved by soft switching method.[2] However, conventional flyback converter usually includes the full-bridge rectifier and large filter capacitor at its input stage. This initial solution produces significant harmonics problems.

Recently, many efforts make to develop PFC (Power Factor Correction) rectifiers and mainly investigated rectifiers are pulse-width-modulated converters. Among them, the most popular topologies for active current wave

shaping are boost converter and single-phase half-bridge converter.

Two-stage approach PFC circuit as Boost converter makes a regulated DC voltage and this narrow-range-varying voltage ( $V_B$ ) improves the efficiency of an optimized  $DC/DC$  output stage. The  $DC/DC$  output stage is the isolated output stage that is implemented with at least one switch, which is controlled by an independent PWM controller to regulate the output voltage tightly. These PFC converters have advantages of high input power factor, continuous line current and tight output regulation characteristics. Although the electrical performance of this scheme is good, it is not acceptable in low power applications since power is converted twice and two independent control loops are required, which increases the cost and size.

Compared with the two-stage approach, the single-stage approach uses only one switch and controller to shape the input current and to regulate the output voltage. This approach has advantages of high input power factor-it is good enough to meet the IEC 61000-3-2 standard, low cost and small size. But this approach has disadvantages of large low frequency output voltage ripple, large increase of the voltage across the storage capacitor at light load. [3], [4]

PFC of active clamp ZVS flyback converter by adding two approaches PFC circuit - two-stage and single-stage - are analyzed in this paper.

## 2. PFC BY TWO-STAGE APPROACH

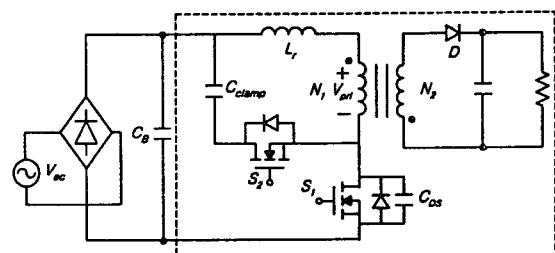


Fig. 1 Active Clamp ZVS flyback converter.

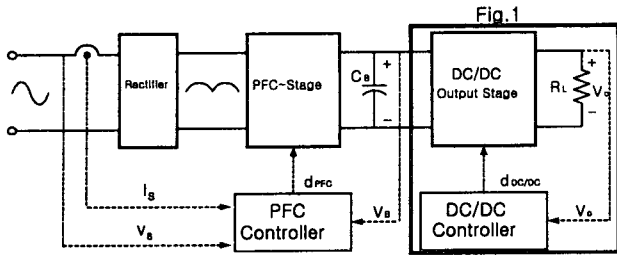


Fig. 2 Structure of two-stage PFC converter.

Fig. 1 shows the conventional active clamp ZVS Flyback converter. In the Fig. 2, the PFC-stage is inserted to improve poor power factor and rich harmonics and *DC/DC* stage uses active clamp ZVS Flyback converter. This two-stage approach has independent controllers - voltage regulation stage and PFC stage. This paper used the average current control and fixed frequency control strategy in the front-end PFC stage. In this strategy, the PFC controller senses the line voltage waveform and forces the input current to track the input voltage to achieve the unit input power factor. [5]

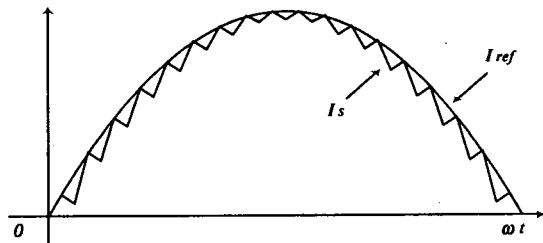


Fig. 3 The average current control and fixed frequency control.

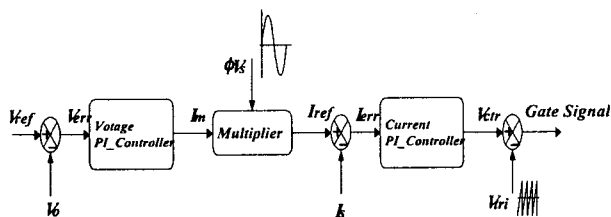


Fig. 4 Block diagram of PFC stage controller.

Fig. 5 shows the boost converter's operation modes used by PFC converter. The overall operation can be divided into two half cycles depending on polarity of AC input voltage. The current waveform is the same as the voltage one. For unity power, only combination of  $S, D_1, D_4$  works as main switches in positive half cycle, while during negative half cycle  $S, D_2, D_3$  work. For each half cycle, each combination of main switches operates as a basic boost converter. During mode 1, switch ( $S$ ) is turned-on, and input current

through the inductor  $L_B$  increases linearly until the  $S$  is turned off. At the same time, bulk capacitor's voltage is discharged to the load. During mode 2, switch is turned-off, and the input current decreases linearly and the stored energy in inductor will be transferred to the load through the diode. During mode 3 and mode 4, negative cycle operation is equal to positive cycle.

Fig. 6 shows the input current and voltage waveforms of a two-stage PFC converter, whereas Fig. 6(b) shows the duty-cycle variations of the front-end PFC stage and the *DC/DC* output voltage during a rectified-line cycle. Since the input and output voltage of the *DC/DC* converter are constant, the duty cycle of the *DC/DC* converter,  $d_{DC/DC}$ , is also constant as shown in Fig 6(b). [6]

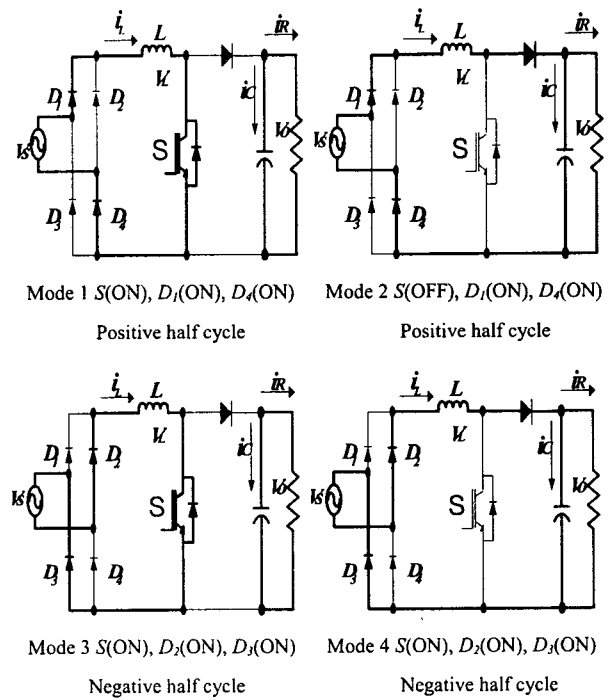


Fig.5 Proposed PFC converter (Boost) and operation modes.

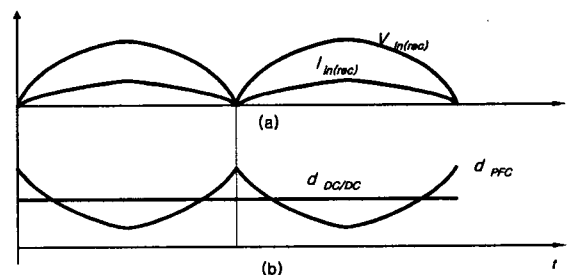


Fig. 6 Ideal waveforms of the two-stage PFC converter.

(a) Rectified input voltage and current

(b) Duty cycle of the PFC and *DC/DC* switch

### 3. PFC BY SINGLE-STAGE APPROACH

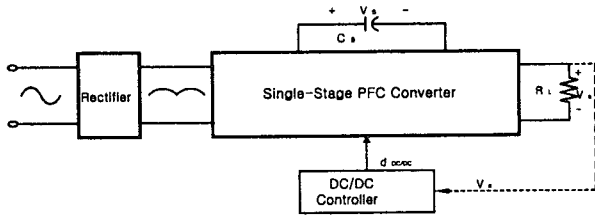


Fig. 7 Structure of single-stage PFC converter.

The conceptual structure of the single-stage PFC converter is shown in Fig. 7. Compared to the two-stage approach, the single-stage approach uses only one switch and controller to shape the input current and to regulate the output voltage. Fig. 8 shows the circuit diagram of a single-stage PFC converter with flyback output. This converter uses an additional inductor  $L_1$  to achieve the CCM(Continuous Conduction Mode) operation. In other words, without PFC controller such as two-stage approach,  $L_1$  progress the variation of effective duty ratio depending on input voltage magnitude.

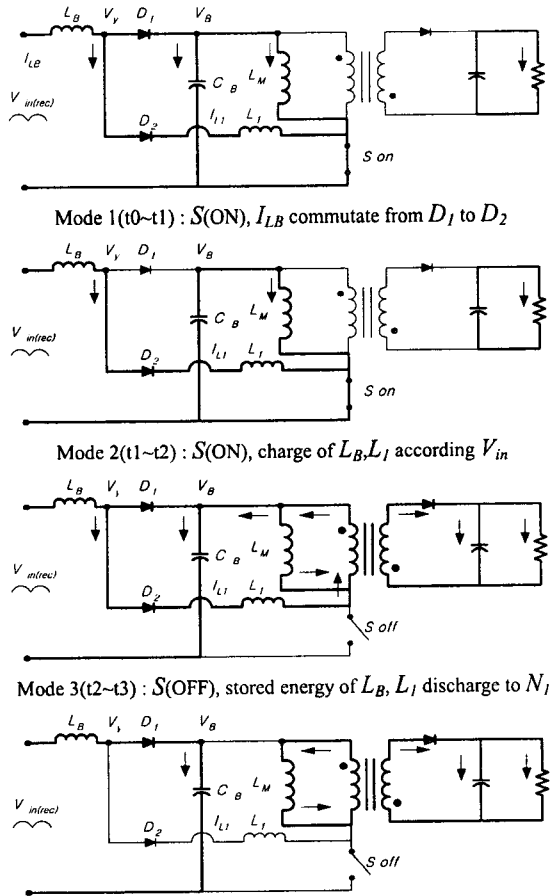
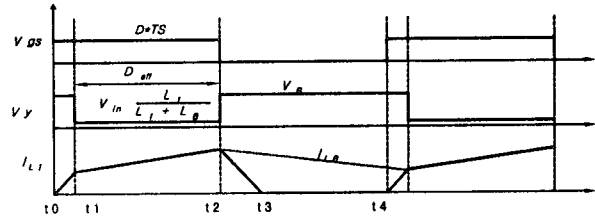
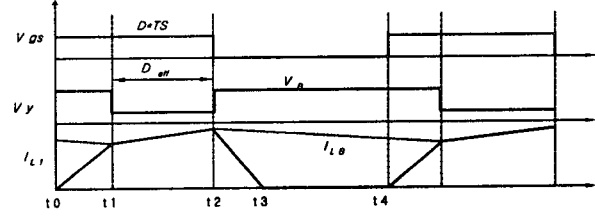


Fig.8 Proposed single-stage converter and operation modes.



(a) Waveforms according to input voltage (ta)



(b) Waveforms according to input voltage (tb)

Fig. 9 Waveforms according to the input voltage.

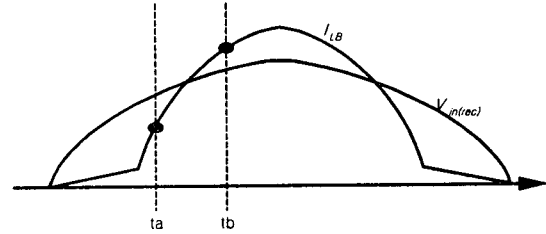


Fig. 10 Input current Waveform according to input voltage magnitude.

Looking into the operation of the proposed approach, its operation can be divided into 4 operation modes for one switching period without consideration of the active clamp circuit.

During mode 1, switch ( $S$ ) is turned-on at  $t=t_0$  and the boost inductor current  $I_{LB}$  starts commutating from  $D_1$  to  $D_2$ . According to Fig.9, the node voltage  $V_Y$  is governed by  $V_Y = V_{in(rec)} \times L_1 / (L_1 + L_B)$ . Finally, interval of  $t_0-t_1$  is determined by  $L_1$  and the instantaneous input voltage. After the commutation is completed at  $t=t_1$ , next mode starts. During mode 2,  $I_{LB}$  flow only to the  $D_2$  and the current through the inductor  $L_B, L_1$  increase linearly until  $S$  is turned off. As input voltage magnitude gets higher, mode 1 period longer while mode 2 period gets shorter. As a result, parameter  $L_1$  modulate the efficiency duty ratio ( $D_{eff}$ ) by  $V_Y = V_{in(rec)} \times L_1 / (L_1 + L_B)$ . In Fig.9, 10 variation of  $D_{eff}$  is shown according to input voltage magnitude without PFC controller such as two-stage approach. During mode 3, switch is turned-off at  $t=t_2$ , and the charged energy of  $L_B, L_1$  start discharging and the energy stored in the core causes the current to flow to the secondary winding. During mode 4, stored energy of  $L_1$  is discharged completely.

Fig.11 shows typical input voltage and current waveform of a single-stage PFC circuit. In this Fig, the duty cycle of the switch is constant during a line cycle. [3], [7]

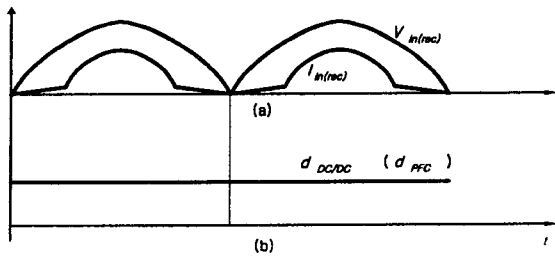


Fig. 11 Waveforms of the single-stage PFC converter.

- (a) Rectified input voltage and current
- (b) Duty cycle of the integrated switch

#### 4. SIMULATION AND EXPERIMENTAL RESULTS

In this paper AC 110[V] of input voltage is used the rated power of 300[W]. Table 1 indicates parameters used in active clamp ZVS flyback converter

Fig. 13 and 14 show input voltage, current waveform and harmonic of input current, which is compared with IEC-61000-3-2 standard. At this time, power factor is 0.71.

Simulation and experiment are executed to improve the power factor by two types of approach.

Table 1 Design parameters of active clamp ZVS flyback converter.

Input voltage $V_{in} (rms)$	110[V]	Bulk capacitor $C_B$	1000[ $\mu$ F]
Output voltage $V_o(DC)$	48[V]	S1Body capacitor $C_{s1}$	700[nF]
Switching frequency $f$	100[kHz]	Leakage inductor $L_r$	20[ $\mu$ H]
Turns ratio $n_T$	4:1	Duty ratio $D$	0.5-0.7

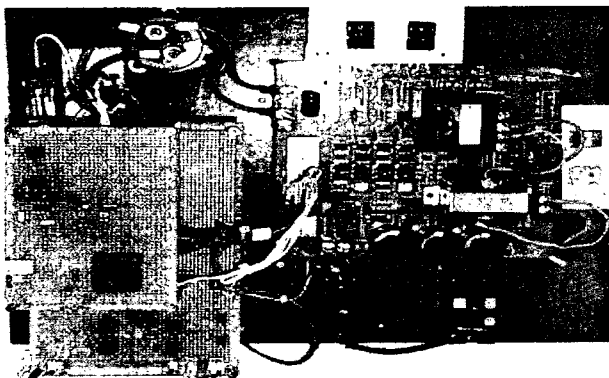


Fig. 12 Photograph of active clamp ZVS flyback converter.

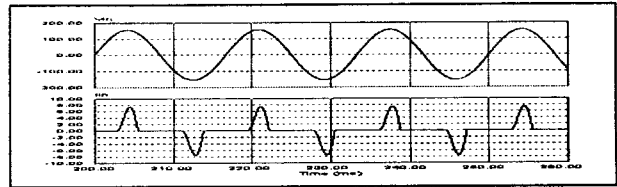


Fig.13 Simulation (conventional active clamp ZVS flyback converter)

Input voltage and Input current waveforms.

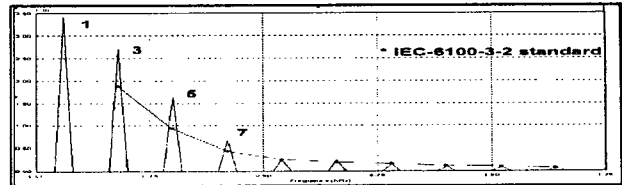


Fig. 14 Measured harmonic content of input current.

(Compared with IEC 61000-3-2 standard)

Fig. 15 shows the simulation of boost PFC converter inserted in PFC-stage. It is supposed input AC 110[V], boost inductor ( $L_B$ : 600[ $\mu$ H]) and the voltage across bulk capacitor ( $C_B$ :2000[ $\mu$ F]) is charged to 190[V]. Input voltage and current waveforms are shown in Fig. 16. Fig 17 shows the harmonic analysis, compared with IEC-61000-3-2. Fig.18 shows the average current control and fixed frequency control waveforms,  $I_{ref}$  and  $I_s$ .

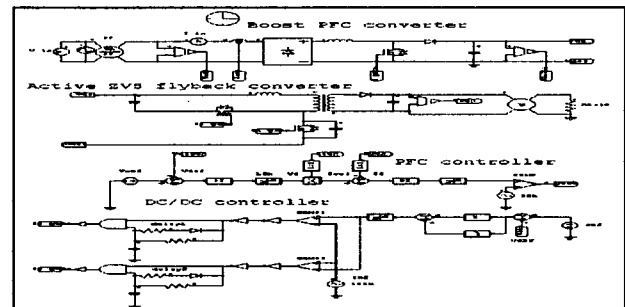


Fig. 15 Simulation circuit by two-stage approach.

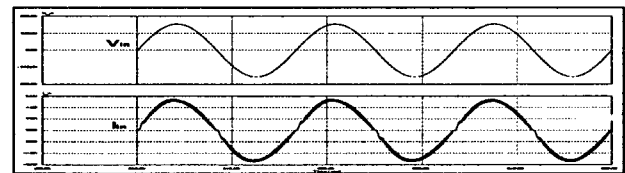


Fig. 16 Simulation (two-stage approach)

Input voltage and line current waveforms (PF:0.98).

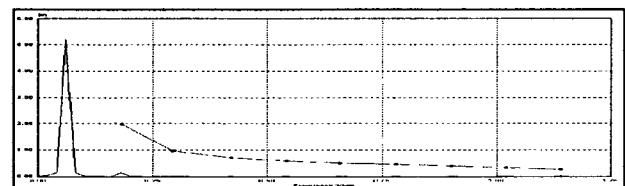


Fig. 17 Measured harmonic content of input current.

(Compared with IEC 61000-3-2 standard)

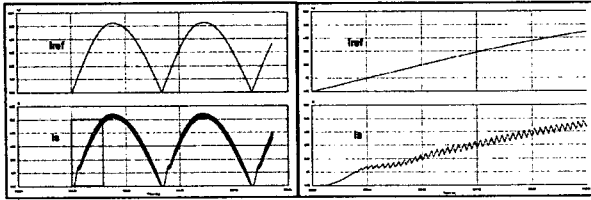


Fig. 18 Waveform of  $I_{ref}$  and  $I_s$ .

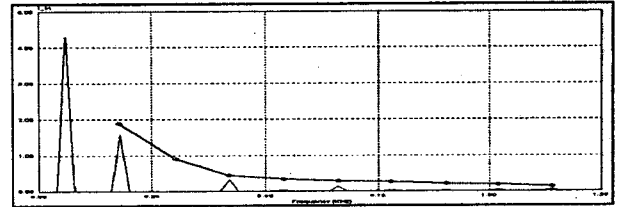


Fig. 21 Measured harmonic content of input current.

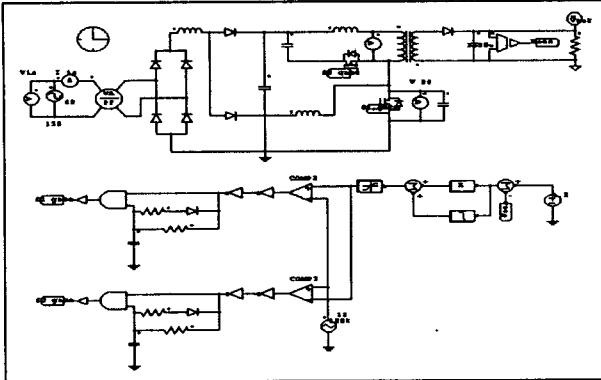


Fig. 19 Simulation circuit by single-stage approach.

Table 2 Design parameters of single-stage approach.

Input voltage $V_{in} (rms)$	110[V]	Bulk capacitor $C_B$	1500[ $\mu$ F]
Output voltage $V_o(DC)$	48[V]	$S_1$ Body capacitor $C_{s1}$	700[nF]
Inductor $L_B$	600[ $\mu$ H]	Leakage inductor $L_r$	20[ $\mu$ H]
Inductor $L_l$	30[ $\mu$ H]	Duty ratio $D$	0.5-0.7
Turns ratio $n_T$	4:1	Switching frequency $f$	100[kHz]

Fig. 19 shows the simulation circuit of proposed single-stage approach and Table 2 indicates parameters used in single-stage approach. PFC circuit is placed between diode rectifier and bulk capacitor and it consists of  $L_l$ ,  $L_B$ ,  $D_1$ ,  $D_2$ . Fig. 20 shows input voltage and current waveform. The harmonic analysis compared with IEC-61000-3-2 is shown in Fig. 21. In Fig. 22,  $D_{eff}$  varies with input voltage magnitude.

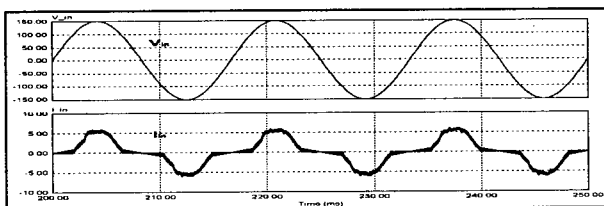
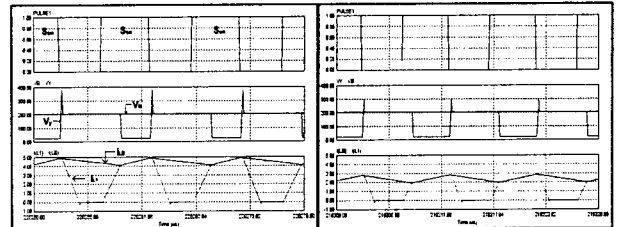


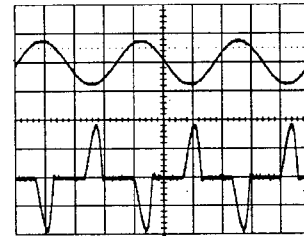
Fig. 20 Simulation (single-stage approach)  
Input voltage and Input current waveforms (PF:0.90).



(a) Input voltage magnitude is high (b) Input voltage magnitude is low

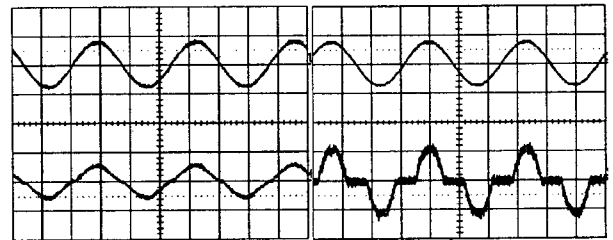
Fig. 22 Simulation waveforms of  $SW_1$ ,  $V_y$ ,  $V_b$ ,  $L_l$ ,  $L_b$ .

Active clamp ZVS flyback converter was implemented with rating power 300[W], the single-stage and two-stage approaches were tested with same condition as the simulation.



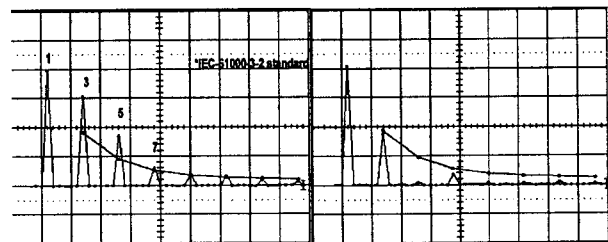
Upper waveform: Input voltage Bottom waveform: Input current

(a) ZVS flyback converter (PF:0.71) (200V/div), (5A/div)



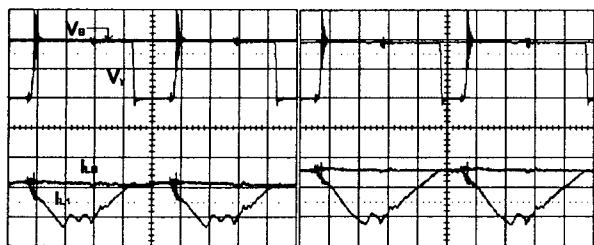
(b) Two-stage approach (PF:0.98) (c) Single-stage approach (PF:0.90)

Fig. 23 Experimental Input voltage and Input current waveforms.



(a) Active clamp ZVS flyback converter (b) Single-stage approach (1A/div)

Fig. 24 Measured harmonic content of input current. (compared with IEC)



(a) Input voltage magnitude is low (b) input voltage magnitude is high  
 Fig.25 Experimental waveforms of  $SW_1$ ,  $V_v$ ,  $V_b(100V/div)$ ,  $I_{L1}$ ,  $I_{L2}(2A/div)$

## 5. CONCLUSION

In this paper, 3 types of 300[W] (Input voltage 110[V], output voltage 48[V]) active clamp ZVS flyback converter are tested and compared in power factor.

Simulation and Experimental results are as follows.

1. Single-stage approach, which controls PF and output voltage is controlled by a single-stage has acceptable harmonics and Power Factor (0.90). And, this approach is recommendable for light size and low cost power converter.

However, at the light load it has the defects of high DC link voltage and 120[Hz] ripple output voltage.

2. Two-stage approach, in which approach Power Factor and output voltage is controlled separately, has good Power Factor (0.98) and tight output regulation characteristics.

However, it is not acceptable in low power applications since power is converted twice and two independent control loops are required, which increases the cost and size.

## REFERENCES

- [1] J.Y.Lee, "New Single-Phase Power Factor Correction Topologies with High Efficiency and Wide Input voltage Ranges", KAIST, doctoral thesis, 2000.
- [2] J.H.Kim, "A Study on the Design of the High Power Active Clamp ZVS Flyback Converter for Semiconductor Plasma Etching" 2000 Korea Power Electronics Annual Conference pp. 400-403, 2000, 7.
- [3] Electromagnetic Compatibility. Part 3: Limits-Sect. 2: Limits for Harmonic Current Emission (Equipment Input Current  $\leq 16A$  Per Phase), IEC 61000-3-2
- [4] Jindong Zhang, Milan M. Jovanovic, and Fred C.Lee, "Comparison Between CCM Single-Stage And Two-Stage Boost PFC Converters" APEC '99. Fourteenth Annual, pp. 335-341 vol.1, 1999, 1.
- [5] Lloyd H. Dixon, "Average Current Mode Control of Switching Power Supplies", Unitrode Application Note U-140, pp. 10-398~10-411.
- [6] Martinez. R, and Enjeti. P.N, "A high-performance single-phase rectifier with input power factor correction", Power Electronics, IEEE Transactions on, pp, 311-317 vol.11, 1996, 3.
- [7] T.J.Kim, "Single phase Single-Stage AC/DC Forward PFC Converter with PFC" 2000 Korea Power Electronics Annual Conference pp. 396-399, 2000, 7.