

Double Two Switch Forward Transformer-Linked Soft-Switching PWM DC-DC Power Converter with Tapped Inductor Filters

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Abstract: This paper presents a novel circuit topology of the double two-switch forward type high frequency transformer linked soft-switching PWM DC-DC power converter with tapped inductor filters that can operate under a condition of the low peak voltage stress across the power semiconductor devices and lowered peak current stress through the transformer for some high power applications. This circuit topology of an interleaved two-switch forward soft-switching power converter is proposed in the order to minimize an idle circulating current due to the tapped inductor filter without of any additional active auxiliary resonant-assisted snubber circuits, such as active resonant DC link snubbers and AC link snubbers, active resonant commutation leg link snubbers. The unique advantages of this power converter are less power circuit components and power semiconductor devices, constant frequency PWM scheme, cost effective configuration and wider soft-switching PWM operation range under PWM power regulations load variations. The practical effectiveness of the proposed soft-switching converter circuit topology is tested by simulations and is proved by experimental results received from the 500W-100kHz breadboard setup.

Keywords: DC-DC power conversion, Two-Switch forward transformer link, Double forward circuit topology, High frequency transformer links, Soft switching PWM, Lowered idle circulating current, Tapped inductor type smoothing filter.

I. INTRODUCTION

With a great advance of power semiconductor devices and control devices, the variety of the high performance DC-DC power converter circuit topologies have been proposed and developed for practical requirements of the increasing power density and power conversion efficiency. In high power applications, the soft-switching PWM full-bridge DC-DC power converters using the latest high-frequency IGBTs have attracted special interest because of their low switching losses, constant frequency PWM operation and simple standard control scheme. However, in many soft-switching PWM DC-DC power converters relatively large idling and/or circulating current generally flows through switching power semiconductor devices and transformer to achieve soft-switching commutation conditions. Owing to the idling and circulating currents, the conduction power losses in the active power switching devices and isolated high-frequency forward transformer are much higher than those of conventional hard-switching PWM DC-DC power converters using IGBTs. [1]-[8]

This paper presents a new prototype topology of the interleaved two-switch forward type high frequency transformer linked soft-switching PWM DC-DC power converter with each channel tapped inductor filter using high-frequency IGBTs, which can simply minimize the idling and circulating currents without the additional power resonant circuit components. The operation principle of this power converter and its steady-state operating characteristics are illustrated on the basis of simulation and experimental results. To verify the practical effectiveness of the proposed soft-switching DC-DC power converter with a high-frequency transformer link, a 500W-100kHz prototype breadboard setup is actually

implemented and tested.

II. CONVERTER DESCRIPTION AND OPERATION PRINCIPLE

A. Circuit Topology and Gate Timing Pulse Sequences

Fig.1. shows a basic circuit topology of the proposed soft-switching power converter using IGBTs, which can operate under the conditions of a zero voltage and zero current soft switching, ZVS and ZCS respectively. This soft switching DC-DC power converter circuit configuration is a combination of two units of the identical interleaved two-switch forward type DC-DC power converters. One of two forward power conversion channel consists of the active switches S_1, S_4 (IGBTs), antiparallel diodes D_2, D_4 , low side forward transformer T_2 with rectifier diode D_6 and tapped inductor filter L_{d3}/L_{d4} in its secondary side. Another forward power conversion stage

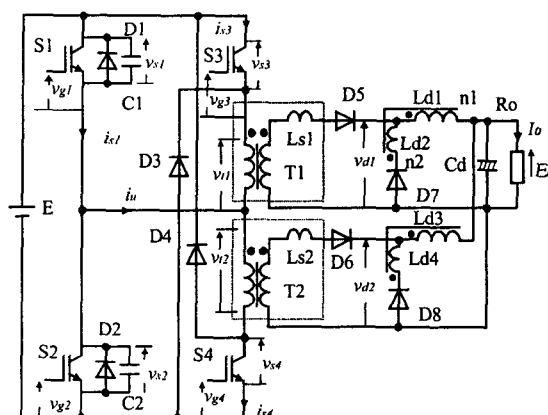


Fig.1. Basic circuit of the proposed converter

consists of the active switches S_2, S_3 (IGBTs), anti-parallel diodes D_1, D_3 , transformer T_1 and rectifier diode D_5 and tapped inductor filter L_{d1}/L_{d2} in its secondary side. The output tapped inductor filters (L_{d1}/L_{d2} and L_{d3}/L_{d4}) are used as a low-pass filter in the parallel to the smoothing capacitor C_d in order to prevent the idling current flowing through power devices and circuit components. The double arrangement of the two-switch forward type DC-DC power converter circuits enabled to achieve a number of advantages such as easy reachable soft-switching conditions, good quality of output current, high power density. In comparison with a previous circuit version of the soft-switching DC-DC power converter with one mutual tapped inductor filter in the new scheme topology each two-switch forward power conversion stage has its own tapped inductor type smoothing filter. [9]-[10] It allows reducing the power capacity and the physical size of the output smoothing capacitor.

A basic control principle of the proposed power converter is based on the duty-cycle PWM. Figure 2 illustrates a gate pulse timing sequences for the switch control strategy. The active power switch S_4 (or S_3 in the other power conversion channel) is turned off after switch S_1 (or S_2) is turned off with a short delay time t_δ . Moreover, the active power switches S_1 and S_2 are driven with a short blanking time t_d that provides complete closing the active power switch before giving signal to another one. By varying interval t_0 as a control variable, the output voltage of the power converter can be continuously regulated under PWM strategy with a constant switching frequency.

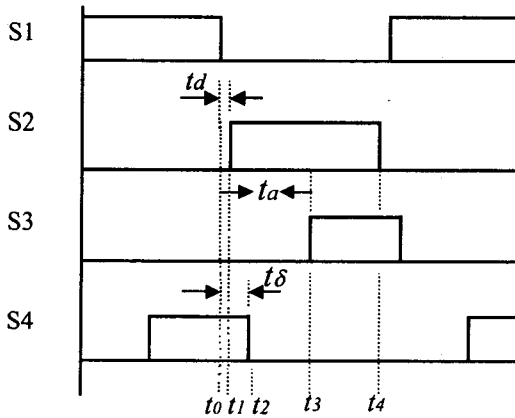


Fig.2. Timing pulses for gate control

B. Steady State Operating Principle

To explain steady-state operation principle of the converter it is assumed that,

- All the active power and passive power semiconductor switches are ideal.
- Parasitic resistances of the circuit components are

equal to zero.

- High frequency transformers T_1 and T_2 as the electrical isolation link and voltage conversion are identical, so that the magnetizing inductances and leakage inductances of T_1 and T_2 are represented as $L_{p1} = L_{p2} \equiv L_p$, $L_{s1} = L_{s2} \equiv L_s$, respectively.
- Capacitances C_1, C_2 of the lossless snubber capacitors are identical: $C_1 = C_2 \equiv C$.
- Inductances L_{d1}, L_{d2} and L_{d3}, L_{d4} of the tapped inductors, moreover L_{d1}, L_{d2} and L_{d3}, L_{d4} respectively are tightly coupled and its electromagnetic coupling coefficient with $k \equiv 1$.

It is also supposed that before time t_0 the active power switches S_1, S_4 and rectifier diode D_6 are conducting. The circuit operation principle in a steady state is given in detail below;

Mode 1 - Interval 1 (t_0, t_1): At the moment t_0 , the active power switch S_1 is turned off under a principle of zero-voltage soft switching due to the lossless capacitive snubbers C_1 connected in parallel with S_1 . The capacitor C_1 is charged and the voltage v_{c1} across this capacitor increases as,

$$v_{c1} = \frac{i_{p2}(t_0) + \{i_{d6}(t_0)/N_T\}}{2C} (t - t_0) \quad (1)$$

Therefore, the rectified voltage v_d in the secondary side of the forward transformer T_2 decreases as follows;

$$v_d = (E - v_{c1})/N_T \quad (2)$$

where, N_T : the turn ratio of the transformer T_2 .

Because the tapped inductors L_{d3} and L_{d4} are tightly coupled with each other, the freewheeling diode D_8 starts to conduct when v_d reaches a value $N_L E_o$, where N_L is the turn ratio of the tapped coupling inductors L_{d3}/L_{d4} , in other words, an autotransformer, is defined as $N_L = n_2 / (n_1 + n_2)$. In this case, n_1 and n_2 are the winding turn numbers of the inductors L_{d3} and L_{d4} , respectively. The load current flows through D_8, L_{d4} and L_{d3} ; therefore, the output current reflected to the transformer primary side decreases gradually.

When voltage v_{c2} falls down to zero, anti-parallel diode D_2 starts to conduct. After the rectified current i_{D6} reaches zero, the total output current of the

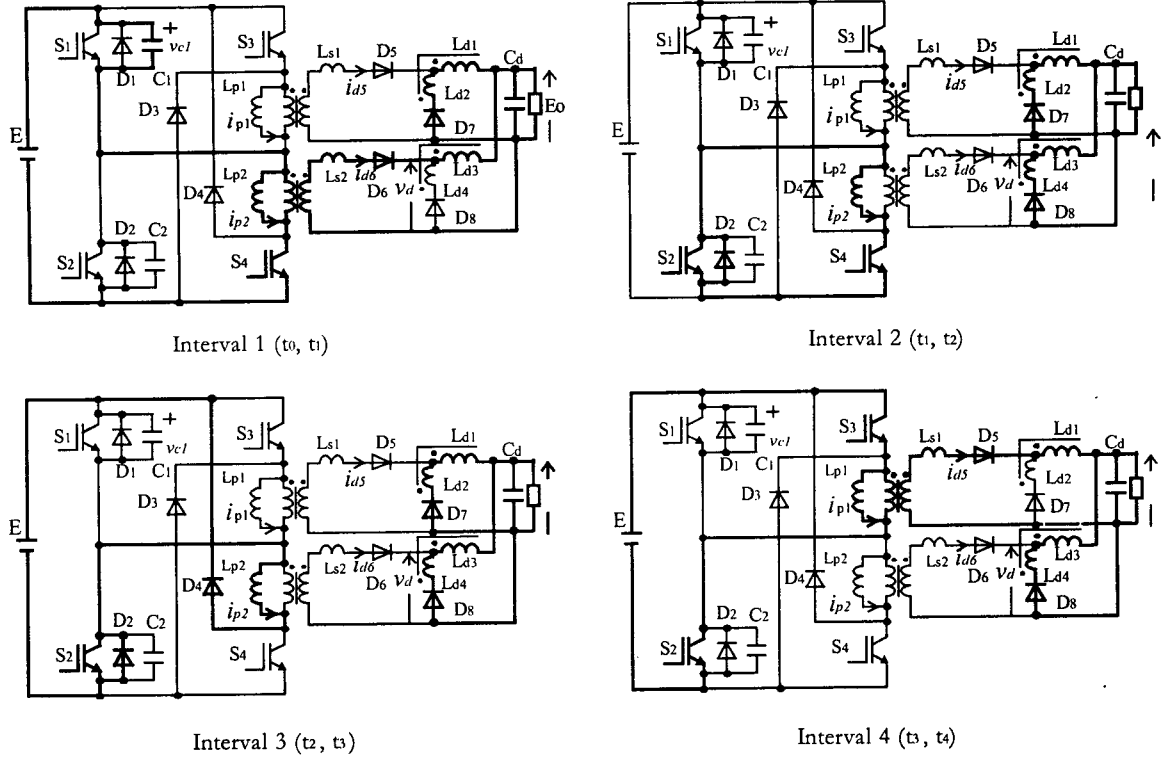


Fig.3. Topological equivalent circuit during each interval of the half cycle of steady-state operation

power conversion stage flows through the diode D_8 and the coupled inductances L_{d4} and L_{d3} . Only a small magnetizing current i_{LP2} of the forward transformer T_2 freewheels through the active power switch S_4 and anti-parallel diode D_2 .

Mode2 - Interval 2 (t_1, t_2): After shot blanking time t_d at the moment t_1 gate signal is applied to the active switch S_2 . The current of the active power switch S_4 equals the magnetizing current of the forward type transformer T_2 . This interval ends when the active power switch S_4 is turned off under ZCS condition.

Mode3 - Interval 3 (t_2, t_3): At time t_2 corresponding to a delay time t_δ , the active power switch S_4 is turned off under a principle of the ZCS. Delay time t_δ is necessary to have time interval until rectified current i_{D6} reaches zero value and current of the active power switch S_4 reduces to the magnetizing current i_{p2} of the forward transformer T_2 . After the active power switch S_4 is opened, the magnetizing current i_{p2} starts to flow through diode D_2 and freewheeling diode D_4 to DC supply voltage source E as a reset action of the forward transformer T_2 and to decrease gradually with a constant slope

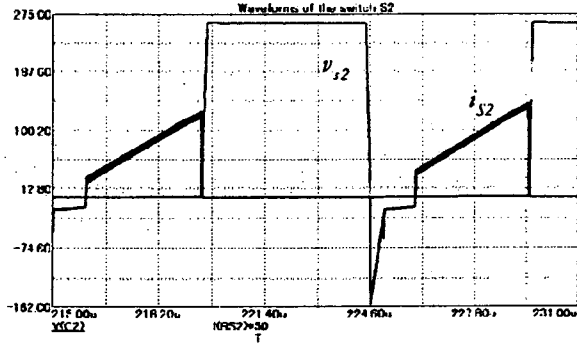
$$di_{p2}/dt = -E/L_p \quad (3)$$

Mode4 - Interval 4 (t_3, t_4): At time t_3 , depending on the duty cycle PWM control strategy of the proposed power converter proportional to controllable time t_{on} the active power switch S_3 is turned on under ZCS mode due to the leakage inductance L_{s1} of the transformer T_1 , which softens current as,

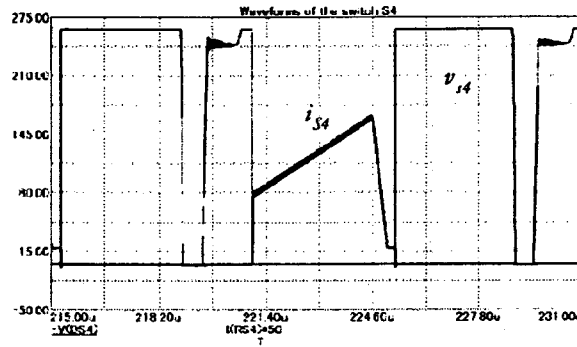
$$di_{S3}/dt = E/L_s \quad (4)$$

The active power switch S_2 is also turned on with ZVS and ZCS modes as the gate signal was applied to this switch in the moment when the antiparallel diode D_2 was conducting. The magnetizing current i_{p1} and the output current reflected to the primary side of the forward transformer T_1 flows through the active power switches S_2 and S_3 ; the power is applied to the load via the transformer T_1 . The rectified current i_{D5} in the output side of the transformer T_1 begins flowing through the diode D_5 . On the other hand, the current i_{Ld4} through the inductance L_{d4} decreases and the diode D_7 turns off. The whole output current of this power conversion stage flows through D_5 and L_{d1} . The energy from electrical DC voltage source is being delivered through S_3, S_2, T_1 , and D_5 at the same time some part of the total load current circulates through L_{d4} and L_{d3} . The next half period of the steady state operation starts at the moment corresponding to time t_4 .

The second half cycle period of the power converter operation ends at time t_4 . The process occurs during the



(a)



(b)

Fig.4. Simulated voltage and current waveforms

- a) v_{s2} : voltage across switch S_2
- i_{s2} : current through switch S_2
- b) v_{s4} : voltage across switch S_4
- i_{s4} : current through switch S_4

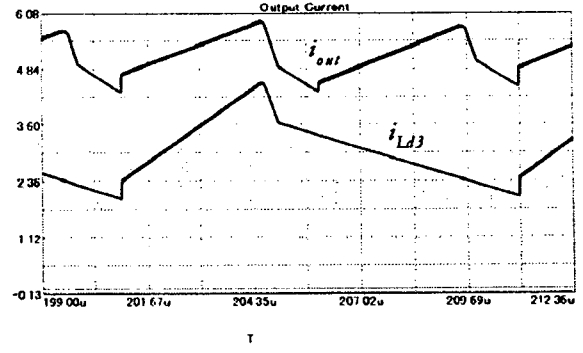
next half-cycle are completely symmetrical with that during the previous half-cycle period. As described above, the active power switches S_1 and S_2 are turned on and turned off with a ZVS commutation, while the active power semiconductor switches S_3 and S_4 operate with a ZCS commutation at both turn-on and turn-off points. The idling and circulating currents in both primary side and secondary side of the high frequency forward type transformers T_1 and T_2 are substantially lowered with no additional auxiliary resonant snubber circuits.

III. SIMULATION AND EXPERIMENTAL RESULTS

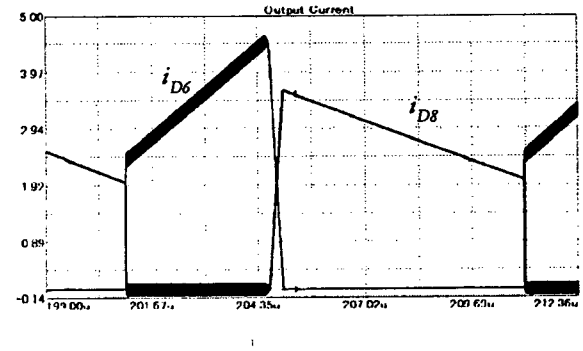
The simulation results received by using software MicroCapVI are presented in the Fig.4. and Fig.5.

In order to verify the operating principle and steady state operating characteristics of the proposed DC-DC power converter the breadboard setup using the high frequency IGBTs was built and tested. The circuit parameters of this power converter are respectively designed for the following design specifications;

$$C1=C2=820pF, \quad N_T=1.71, \quad L_{p1}=L_{p2}=2.8mH, \\ L_{s1}=L_{s2}=0.68\mu H, \quad L_{d1}=L_{d3}=148\mu H, \quad L_{d2}=L_{d4}=6.7\mu H, \\ N_L=0.174, \quad k=0.933, \quad C_d=180\mu F, \quad t_d=0.5\mu s, \quad t_0=0.8\mu s.$$



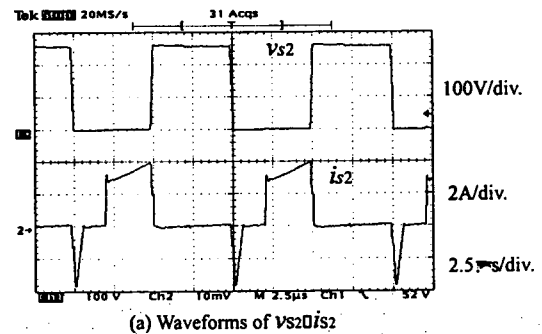
(a)



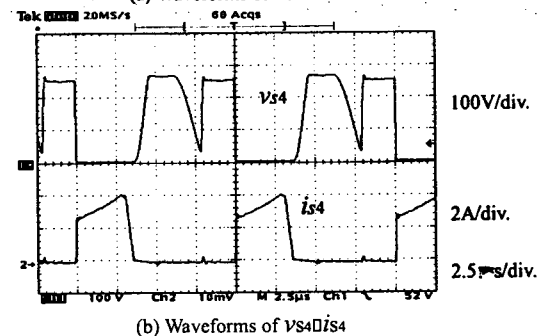
(b)

Fig.5. Simulated current waveforms

- a) i_{ont} : total output current
- i_{LD3} : output current of the one conversion channel
- b) i_{D8} : current through diode D_8
- i_{D6} : current through rectifier diode D_6



(a) Waveforms of Vs2Is2



(b) Waveforms of Vs4Is4

Fig.6. Observed waveforms of the converter

Experimental results are demonstrated in Fig.6. The

experimental results are identical with simulation ones.

IV. CONCLUSIONS

The novel circuit topology of the interleaved double two-switch forward transformer type soft-switching PWM DC-DC power converter with the tapped inductor filters has been represented in this paper. The operation principle of the converter has been illustrated; the characteristics of the power converter were verified by the 100kHz 500W breadboard setup.

The proposed soft-switching power converter has the following unique features: lowered switching power losses in a wide load variation ranges, small value of the idling and circulating currents, resulting in low conduction power losses, constant frequency PWM scheme for output regulation, recovery current of rectified diodes is relatively low due to zero current soft switching.

In the future the steady state performances of soft switching power DC-DC converter using advanced IGBTs such as High Conductivity IGBTs (HiGT), Barrier Storage Trench Gate IGBTs (CSTBT) and IEGTs should be evaluated from a practical point of view.

REFERENCES

- [1] Undeland, T. M.: "Snubbers for pulse width modulated bridge converters with power transistors or GTO's". IEE-Japan Int. Power Electronics Conference (IPEC), Tokyo, Japan, Vol.1 pp. 313-323, March 1983.
- [2] Patterson O. D. and Divan D. M.: "Pseudo-resonant full bridge DC/DC converter". Proceedings of IEEE Power Electronics Specialists Conference (PESC), Blacksburg VA, USA, Vol.2 pp.424-430, June 1987.
- [3] Sabate J. A., Vlatkovic V., Ridley R. B., Lee F. C., and Cho B. H.: "Design considerations for high-voltage high-power full-bridge zero-voltage switched PWM converter". Proceedings of IEEE Applied Power Electronics Conference (APEC), Los Angeles, USA, Vol.1 pp.275-284, March 1990.
- [4] Cho J. G., Rim G. H., and Lee F. C.: "Zero voltage and zero current switching full bridge PWM converter using secondary active clamp". Proceedings of IEEE Power Electronics Specialists Conference (PESC), San Jose, USA, Vol.2 pp.657-663, June 1996.
- [5] Kim Eun-Soo, Joe Kee-Yeon, Kye Moon-Ho, Kim Yoon-Ho, and Yoon Byung-Do: "An improved soft-switching PWM FB DC/DC converter for reducing conduction losses". IEEE Transactions on Power Electronics, Vol.14, No.2, pp.258-263, 1999.
- [6] Hamada S., Ogino Y., and Nakaoka M.: "Saturable reactor assisted soft-switching full-bridge DC-DC power converters". IEE Transactions - Electric Power Applications, Vol.138, No.2, pp.95-103, 1991.
- [7] Hamada S., Maruyama Y., and Nakaoka M.: "Saturable reactor assisted soft-switching technique in PWM DC-DC converters". Proceedings of IEEE Power Electronics Specialists Conference (PESC), New York, USA, Vol.1 pp.93-100, 1992.
- [8] Hamada S., Maruyama Y., Nakaoka M., and Murakami Y.: "An improved soft-switching PWM full-bridge DC-DC converter modification operating at reduced conduction loss". Proceedings of IEEE Power Electronics Specialists Conference (PESC), Seattle, USA, Vol.1 pp.165-170, 1993.
- [9] Hamada S., Morimoto T., Matsushige T. and Nakaoka M.: "Feasible evaluation of non-resonant soft-switching duty factor controlled DC-DC power converter with reduction losses". Proceedings of IEEE International Power Electronics and Motion Control (IPEMC), Beijing, China, Vol.3 pp.915-920, August 2000.
- [10] Hamada S., Gamage L., Morimoto T. and Nakaoka M.: "A novel zero-voltage and zero-current soft-switching PWM DC-DC converter with reduced condition losses". Proceedings of IEEE Applied Power Electronics Conference (APEC), New Orleans, USA, Vol.3 pp.741-74, February 2000.