Properties of Thin Film a-Si:H and Poly-Si TFT's

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Abstract

A-Si:H and poly-Si TFT characteristics were investigated using an inverted staggered type TFT. The poly-Si films were achieved by various anneal techniques ; isothermal, RTA, and excimer laser anneal. The TFT on as-grown a-Si:H exhibited a low field effect mobility, transconductance, and high gate threshold voltage. Some films were annealed at temperatures from 200℃ to 1000 ℃. The TFT on poly-Si showed an improved I_{on}/I_{off} ratio of 10^6, reduced gate threshold voltage, and increased field effect mobility by three orders. Inverter operation was examined to verify logic circuit application using the poly-Si TFTs.

Key words(중요용어) : Poly-Si, Thin Film Transistor (TFT), field effect mobility, inverted staggered type

1. Introduction

Present a-Si:H thin film transistors (TFTs) are not fast enough to handle peripheral circuits of liquid crystal displays (LCDs) since the field effect mobility is low. On the other hand, the field effect mobility for poly-Si TFTs is sufficiently high to permit implementation of on-board logic circuits [1]. Presviously, crystallization of a-Si:H films on glass substrates were limited to anneal temperature below 600℃, over 10 h to avoid glass shrinkage. Our study indicates that the crystallization is strongly influenced by anneal temperature and weakly affected by anneal duration time. Conventionally, poly-Si was achieved by either film growth at high substrate temperature or high temperature anneal treatment after the thin film Si growth. Because of the high temperature process and nonconducting substrate requirements for poly-Si TFTs, the employed substrates were limited to quartz, sapphire, and oxidized Si wafer.

We reported on poly-Si TFTs using high temperature anneal on a-Si:H/Mo structures. The metal Mo substrate was stable enough to allow 1000℃ anneal. A novel TFT fabrication was achieved by using part of the Mo substrate as drain and source ohmic contact electrode. The as-grown a-Si:H TFT was compared to anneal treated poly-Si TFTs. Defect induced trap states of TFTs were examined using the thermally stimulated current (TSC) method. In some case, the poly-Si grain boundaries were passivated by hydrogen.

2. Experimental

The a-Si:H films were deposited onto 4"×8" Mo metal substrates by dc glow discharge decomposition of silane. Deposition temperature varied from 225 to 300℃ giving a deposition rate of around 0.5 ㎛/min. Prior to a-Si:H growth, a highly doped layer was deposited to achieve a good ohmic contact. Investigated sample structure was intrinsic a-Si:H/n^+ a-Si:H/Mo (i/n^+/Mo). The

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employed anneal techniques are anneal in nitrogen atmosphere, anneal in a vacuum, RTA, and excimer laser anneal. A novel TFT fabrication process was developed by using the Mo substrate as source and drain contact. The Si film side was bonded to a foreign substrate and source and drain were defined by chemically removing to Mo substrate ; then the n^+ layer between source and drain was removed by isotropic Si etching. Inverted staggered type TFT output is strongly influenced by series resistance from source to channel and drain to channel. A film thickness less than 0.5 ㎛ was employed for the study. The investigated insulators were evaporated SiO, RF deposited SiO_2, RF magnetron sputter deposited amorphous $BaTiO_3$, Si_3N_4 and MgO. TFT output influencing factors were examined such as anneal temperature, gate dimension, Si film thickness, insulator thickness, and grain boundary passivation. Anneal temperature ranged from 200 to 1100℃ with an increasing step of 100℃. Gate length effect was studied by varing the gate length from 25 to 200 ㎛ and fixing the gate width at 500 ㎛. The insulator thickness effect study was carried out with oxide thickness ranging from 50 to 1000 nm. The poly-Si grain boundary traps were examined by thermally stimulated capacitance (TSCAP) and thermally stimulated current (TSC) measurement The device was first cooled and then heated at a constant rate. Electron and hole traps were detected as the sample was heated. The poly-Si films formed by RTA 950℃, 2 min. were exposed to hydrogen grain boundary passivation. The investigated parameters of the grain boundary passivation were substrate temperature effect(275~400℃), hydrogen exposure time (10min.~7h), and distance between electrode and substrate holder.

3. Results and Discussion

To optimize TFT insulator quality, a study was carried out on MIS capacitors. SiO and Si_3N_4 showed the existence of positive fixed charge and the effect of relatively high mobile charge. For RF sputter grown SiO_2, we observed negative fixed charge for high RF power (400 Watt) and positive fixed charge for low RF power (200 Watt). Fixed charges are compensated by using double layers of SiO_2 doposited at low and high RF power. Flatband voltage shift indicated oxide trapped charges to be greatly reduced with the double layer of RF SiO_2 [2]. The MIS capacitor high frequency and quasistatic C-V result on evaporated SiO with oxygen introduction showed a low interface density ranging from 10^{11} to 10^{12} $cm^{-2}eV^{-1}$. The MIM structure capacitor I-V measurements were performed to find capacitance per unit area and low leakage current characteristics of the insulating layer. The thermally grown oxide capacitor exhibited the lowest leakage current and a high breakdown voltage. The second best was with double layer SiO_2 and the evaporated SiO in oxygen gas.

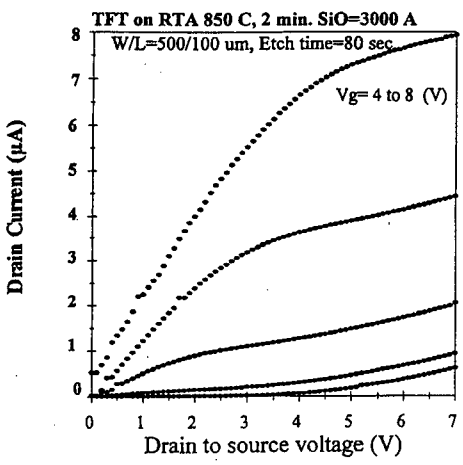

Figure 1. The TFT Id-Vds characteristics on 0.3㎛ thick poly Si

The oxide thickness influences the gate threshold voltage (V_T) and capacitance per unit area (C/A) As oxide thickness increased, the V_T increased (V_T=1.5 V for t_{SiO}=50 nm and V_T=10 V for t_{SiO}=800 nm) and the C/A was reduced. This indicates that the TFT switching voltage can be controlled by manipulating oxide thickness. As Si film thickness was reduced, the gate threshold Voltage was reduced. The optimum Si film thickness for TFT application was 0.3 ㎛. Figure

1. shows the TFT output for a 0.3 μm thick film with increased drain current and transconductance. As Si film thickness was less then 0.1 μm, TFT output degradation was observed. This may have come from Si film non-uniformity due to the Mo substrate surface conditions. The TFT on a 0.1 μm thick Si film exhibited reduced drain current, reduced transconductance, reduced field effect mobility, and the drain current kink effect.

The TFT on as-grown Si:H exhibited a field effect mobility of 1.6×10^{-3} $cm^2/V\cdot s$ with and evaporated SiO gate insulator layer. The TFT on as-grown intrinsic a-Si:H shows a relatively high threshold voltage of 12 V and a low I_{on}/I_{off} ratio of about 10. TFT output characteristics after RTA 600℃, 2min. exhibited well saturated drain current (I_d), improved transconductance, and reduced gate threshold voltage. A further improvement of TFT device performance was observed for high temperature (above 700℃) anneal of an intrinsic Si film which gave high ON current and low OFF current. The I_{on}/I_{off} ratio of 10^5 was achieved after RTA 850℃, 2min.

Table 1. Trap type and Activation Energy from TSC Study

Anneal (°C)	T_m (K)	Trap type	ΔE(eV)
As-grown	T_{m1}=345 T_{m2}=370	Hole Electron	0.45 0.49
600	T_{m1}=330 T_{m2}=370	Hole Electron	0.42 0.49
700	T_{m1}=170 T_{m2}=200 T_{m3}=225 T_{m4}=235 T_{m5}=370	Electron Hole Electron Electron Electron	0.18 0.22 0.25 0.27 0.49
850	T_{m1}=370	Hole	0.49
850 H^+ passivation 300℃ , 4 h	T_{m1}=370	Hole	0.49

Table 1. shows only two trap states (e,h) for as grown-Si:H, increased trap states with activation energy of 0.2 to 0.5 eV after RTA at 700℃, and hole trap states to dominate after high temperature anneal (>850℃) . Hydrogen grain boundary passivation was made on RTA 850℃, 2

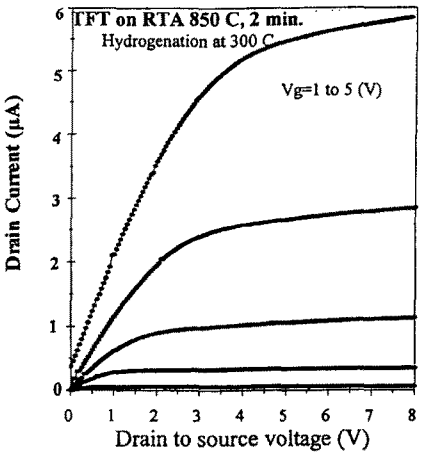

Fig. 2. The TFT I_d-V_{ds} characteristics on thin-film Si RTA 850 °C, 2 min. annealed and r.f rehydrogenated at a substrate tempeature of 300°C, 4 h.

min anneal treated poly-Si. The RF plasma rehydrogenation was 300℃. As hydrogen exposure time increased, mobility improvement was observed. The optimized exposure time for the RF plasma rehydrogenation was 6 hours at a substrate temperature of 300℃. The optimized distance between electrode to substrate holder using the RF plasma was 1/2 inch. A RF plasma rehydrogention at 300℃, 4 h improved the I_{on}/I_{off} ratio to 10^6. An increased drain current and transconductance contributed to improve field effect mobility after hydrogen grain boundary passivation (Fig.2). Table 2. Shows a summary of the anneal temperature effect on the TFT output characteristic parameters. As anneal temperature increased, the transconductance was increased and the drain voltage was reduced for TFT drain current saturation, The RF plasma hydrogen passivation on the poly-Si film improved the transconductance and field effect mobility. The field effect mobility was determined from the transconductance. Figure 3 shows a summary of change in mobility with anneal temperature. Mobility stays in the order of 10^{-3} $cm^2/V\cdot s$ for anneal temperature below 600℃. An anneal temperature highest than 700℃ gave 3 order

Table 2. A Summary if TFT Anneal Temperature Effect.

	Temp (°C)	W/L (μm)	C/A (F/cm)	V_{ds} (V)	g_m (moh)	μ_{fe} ($cm^2/V \cdot s$)
RTA	No heat	500 /114	1.2×10^{-8}	25	1.6×10^{-9}	1.6×10^{-3}
	400	500 /200	1.3×10^{-8}	15	18.3×10^{-9}	39.0×10^{-3}
	600	500 /200	1.2×10^{-8}	6	7.0×10^{-9}	22.7×10^{-3}
	850	500 /200	1.9×10^{-8}	6	2.0×10^{-6}	3.6
	H^+ 300	500 /200	1.9×10^{-8}	5	4.5×10^{-6}	19.4
VAC	200	500 /200	1.6×10^{-8}	12	7.0×10^{-10}	2.2×10^{-3}
	400	500 /200	1.9×10^{-8}	8	1.1×10^{-9}	2.9×10^{-3}
	600	500 /200	1.9×10^{-8}	4	3.0×10^{-10}	8.1×10^{-3}
	700	500 /200	1.9×10^{-8}	5	9.0×10^{-6}	24.3

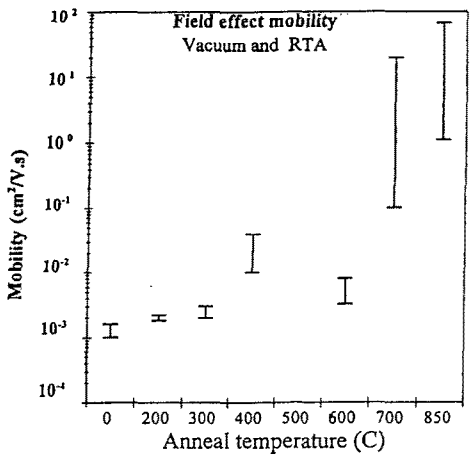

Figure 3. The summary of field effect mobility as a function anneal temperature.

improved field effect mobility. The inverter switching characteristics were strongly influenced by gate transfer characteristics (V_T), drain resistance (R_d), anneal temperature, and rehydrogenation treatment. Inverter switching voltage was increased as oxide thickness increased. The poly-Si TFTs with oxide thickness below 250 nm can be readily operated for gate bias less than 5 V. Drain resistance R_d must be chosen less than TFT off resistance and larger than TFT ON resistance. Generally inverter switching characteristics exhibited very sharp ON and OFF transitions for a high R_d and slow transition for a low R_d value. Rehydrogenation treatment reduced inverter switching voltage was reduced after high temperature anneal reduced insulator thickness, and reduced gate length.

4. Conclusions

A novel method of TFT fabrication was developed using the Mo substrate as drain and source contact, while removing other portion of the Mo. The Mo substrate was stable for high temperature processing and removable for TFT fabrication. We have shown TFT improvement after high temperature anneal treatments. The thermally grown oxide capacitor exhibited the lowest leakage current and high breakdown voltage. The second best was with double layer SiO_2 and the evaporated SiO in oxygen gas. The gate threshold voltage was increased as insulator thickness increased. The best working Si film thickness was 0.3 μm thick. As anneal temperature increased the TFT exhibited increased gm and reduced V_{ds}, V_T. The high temperature annealed poly-Si TFT output characteristics were very stable against external light illumination. The field effect mobility was improved by three orders after high temperature anneal. The poly-Si grain boundary passivation with hydrogen increased the field effect mobility to as high as 67 $cm^2/V \cdot s$. Grain boundary trap type and activation energy of 0.49 eV dominated after the high temperature anneal. The optimized conditions of the RF plasma rehydrogenation require a substrate temperature of 300℃, exposure time of 6 h, and electrode distance of 1/2 inch spacing from the substrate holder.

References

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