Influence of reset pulse form on electrical characteristics in AC-PDP

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After the square type reset pulse, the condition of remaining wall charge has been experimentally investigated in AC-PDP with **VDS** (Versatile Driving Simulator) system, in which arbitrary driving waveform and sequence can be used. After the self-discharge process, almost wall charges are eliminated. But some wall charges are not and its quantity is dependent on the voltage of the reset pulse. When the voltage of the reset pulse is growing, its quantity is decreased. But if the voltage of the reset pulse is above 300V, the wall voltage due to remaining wall charge is constant and its value is found out 6V. Also it is found that its polarity is always same with the one made by the reset pulse. It means that the polarity is not changed by the self-discharge.

Keywords : AC-PDP, Reset pulse, wall charge, wall voltage, driving

1. Introduction

The multi-subfield technique is widely used for the realization of 256 gray level in AC-PDP driving. In this method, 1 TV-field is divided into 8 ~10 subfields which have different length of display period. But, in conventional AC-PDP driving method, ADS or AWD, the relationship between display information of each subfield has not been used until now. So the reset period should be used in the starting part of each subfield. This 'reset' means the elimination of wall charge information that each AC-PDP cell has. That is to say, it makes the same wall charge condition of all cells in AC-PDP. Generally, a high voltage pulse above firing voltage, named reset pulse, has been used in the reset period for this reason. The basic research about the reset pulse is necessary for optimization of AC-PDP driving because the operational characteristics of AC-PDP, such as address voltage or contrast, can be strongly affected by it. Presently, 3 types of reset pulse are mainly used, such as square type, long ramp type and exponential type. Also they could be divided into two species, such as full erasing pulse and full writing pulse, according to the wall charge condition after these reset pulse. In the case of using a writing address method, the full erasing reset pulse should be used. In this paper, the square type reset pulse, as a full erasing pulse, are dealt with.

If the square type reset pulse is applied in PDP cell, the strong discharge is occurred and a large amount of wall charge is piled up on the sustain electrodes. Then these wall charges induce the high wall voltage, and a self-discharge due to the wall voltage could be occurred when the applied reset voltage goes down to zero. It is known that this self-discharge has a erase function, which most of wall charges are eliminated. In this research, according to the conditions of square type reset pulse, the remained wall charge conditions

after the reset pulse, have been experimentally investigated.

2. Experimental Configurations

This experiment has been performed with VDS (versatile driving simulator) system developed in our center, which high voltage arbitrary waveform and arbitrary sequence can be easily used. **Figure 1** shows the experimental setup. The driving waveform and sequence have been edited by Win98 based waveform editing program. Then it has been converted into high voltage driving signals for PDP by multi-D/A system and HV-amp. The used test panel is a 6 inch, VGA class AC-PDP(1080 μm pitch). The number of used cells is 80 x RGB.

For finding out the remained wall charge conditions after the reset period, a firing voltage check method has been used. This method is based on the variations of firing voltage by the wall voltage. After the self-discharge, if there are some remained wall charges, the firing minimum voltage is varied by its quantity and polarity. So they can be checked by applying a proper detecting pulse which has two polarity.

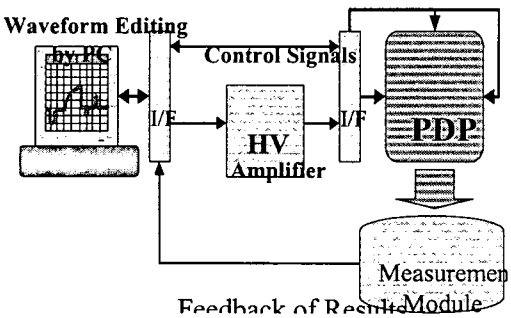

Figure 1. Block diagram of VDS system which can use arbitrary waveform and sequences. It is consisted of HV-amp, pc-based arbitrary waveform generator and interfacing units.

Figure 2 shows the full driving sequence of firing voltage check method.

All pulses are symmetrically designed relative to X-Y sustain electrodes and address electrodes have been maintained in floating level to minimize the influence of address electrodes. The square type reset pulse has a constant pulse width, 20 μs and its voltage height is varied from 270V to 350V. A firing voltage detecting pulses are also designed to square type with two polarities and those pulse width is 10μs. Also avoiding the influence of priming particles on the firing voltage, the 200μs zero period is inserted between the reset and detecting pulse. And a erase pulse group is inserted in last part of the sequence for erasing the wall charge. A full length of the sequence is 600μs.

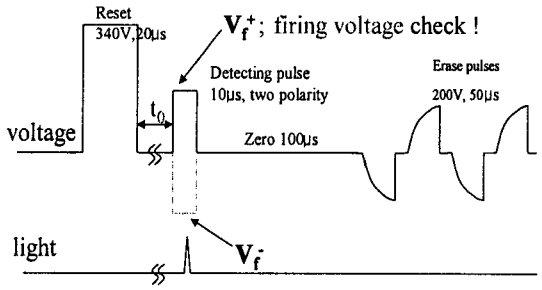

Figure 2. The full driving sequence of firing voltage check method.

The firing voltages are checked in two cases ; V_f^+ (when the detecting pulse has a same polarity with reset pulse) and V_f^- (when the detecting pulse has a inverse polarity with reset pulse). In a given reset pulse condition, the voltage of detecting pulses has been controlled from low to high voltage, until there is a evidence of weak discharge during the detecting pulse period. So according to the reset voltage, the variations of two firing voltages, V_f^+ and V_f^- have been alternatively checked. A sensitive IR-probe and a differential voltage probe are used as measuring devices in this case. The reference of firing is the evidence of weak discharge during the detecting pulse, measured by the

sensitive IR-probe in a given reset pulse condition. By comparing the two firing voltages, V_f^+ and V_f^-, the polarity of remained wall charge and its wall voltage can be found out.

3. *Experimental Results & Discussions*

Figure 3 shows the experimental results. The upper line is the firing voltage variation in case of applying the positive detecting pulse, while lower line is in case of applying the negative detecting pulse. Both two lines are approaching the constant value when the voltage of reset pulse is above 300V. The minimum voltage gap between the two lines is 12V. The condition of remaining wall charge can be clearly found out from these data.

First, the polarity of remaining wall charge is same with the polarity of wall charge in reset period. Because the firing voltages when the negative detecting pulse is applied, are lower than the case of positive detecting pulse. It means that the wall charge is not clearly eliminated by the self-discharge after the reset pulse.

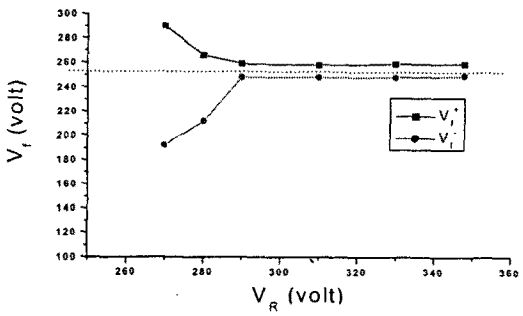

Figure 3. Variation of firing voltage according to the voltage of reset pulse. The upper data is in case of applying the positive detecting pulse.

Second, the quantity of wall charge is strongly dependent on the voltage of the reset pulse. It can be easily known from the variation of the two firing voltages. The voltage gap between two lines is caused by the wall voltage due to remaining wall charge. The wall voltages by the remaining wall charge can be estimated by a simple equation, $(V_f^+ - V_f^-)/2$. These value are decreased when the voltage of reset pulse is increased, and approached the constant value, 12V above 300V. It means that the erase effect of self-discharge is dependent on the voltage of the reset pulse.

4. Conclusion

After the square type reset pulse, the condition of remaining wall charge has been experimentally investigated in AC-PDP with **VDS** (Versatile Driving Simulator) system, in which arbitrary driving waveform and sequence can be used.

After the self-discharge process, almost wall charges are eliminated. But some wall charges are not and its quantity is dependent on the voltage of the reset pulse. When the voltage of the reset pulse is growing, its quantity is decreased. But if the voltage of the reset pulse is above 300V, the wall voltage due to remaining wall charge is constant and its value is found out 6V. And its polarity is always same with the one made by the reset pulse. It means that the polarity is not changed by the self-discharge.

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