The Study on the Trap Density in Thin Silicon Oxide Films

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Abstract

In this paper, the stress and transient currents associated with the on and off time of applied voltage were used to measure the density and distribution of high voltage stress induced traps in thin silicon oxide films. The transient currents were due to the discharging of traps generated by high stress voltage in the silicon oxides. The trap distributions were relatively uniform near both cathode and anode interface. The trap densities were dependent on the stress polarity. The stress generated trap distributions were relatively uniform the order of $10^{11}\sim10^{21}$[states/eV/cm^2] after a stress. The trap densities at the oxide silicon interface after high stress voltages were in the $10^{10}\sim10^{13}$[states/eV/cm^2]. It appear that the stress and transient current that flowed when the stress voltage were applied to the oxide was caused by carriers tunneling through the silicon oxide by the high voltage stress generated traps.

Key Words : stress current, transient current, trap density, trap distribution, silicon oxide

1. Introduction

The stressing current of thin silicon oxide films during and after high voltage have been studies. It has been shown that tunneling currents through thin silicon oxides at high stressing voltages generated electron traps within the silicon oxides. Traps have been observed to be generated at the anode and cathode by the high stress voltage. It has been shown that the trap generation at the cathode decreased as the fluence of electrons through the silicon oxide increased and was independent of stress polarity. The stress induced trap generation has been an increase in the low level pretunneling current. Low level pretunneling current has been attributed to a lowering of the tunneling barrier or to the increase at the cathode trap density.

The time decay of the threshold voltage shifts caused by traps generated by avalanche injection was modeled by the tunneling discharge of the trapped electrons in the silicon oxides. The tunneling discharge of irradiation generated trapped electrons has been shown to be a function of the applied voltage. The discharging of shallow traps in Fowler Nordheim stressed thin silicon oxides has been traced to tunneling into the traps located near the cathode interface.

The tunneling front model could be used to analyze the low level currents and pretunneling currents that have been observed in stressed silicon oxides. The transient currents associated with the during and removal of low voltage to the stressed silicon oxides were determined to be the charging and discharging of the traps generated in the silicon oxides. these low level transient currents were analyzed to determine the distribution of the stress generated traps in the silicon oxides near the anode and cathode interfaces.

2. Results and Discussion

A current density vs. voltage characteristic of an unstressed silicon oxide measured to breakdown has been shown in figure 1.

The current was composed of three regions, the low level, pretunneling region, the tunneling region, and the breakdown region. Prior to the onset of tunneling the currents were in the low ampere range. Constant voltages with high tunneling currents were used to stress the oxides. The stress currents were measured during the stress and integrated to obtain the fluence through the oxide. The transient currents associated with the turn off of the stress voltages were measured. The transient currents were measured during the voltage pulse after the voltages had been removed.

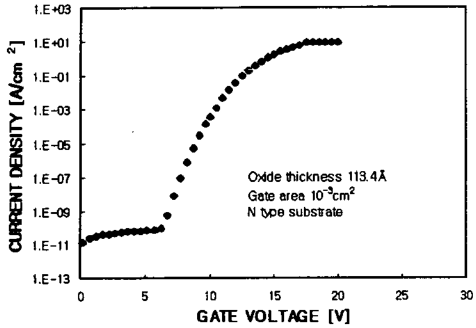


Fig. 1 A typical current voltage characteristic for a thin silicon oxide

The stress currents through an unstressed oxide measured during application of constant positive gate voltage and the transient currents through an unstressed oxide measured after application of constant positive gate voltage has been shown in figure 2.

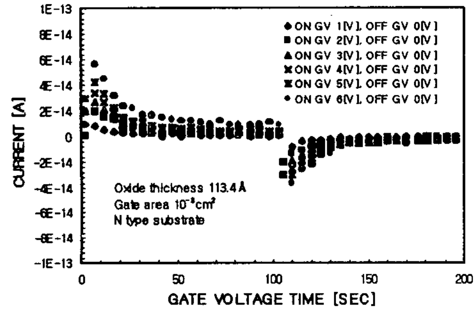
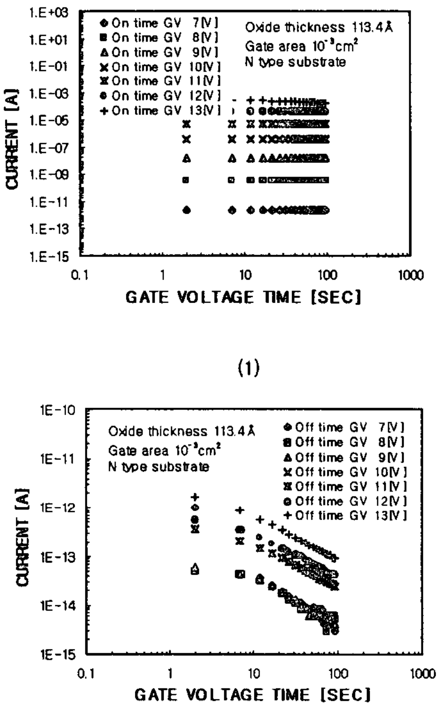


Figure 2 The stress and transient currents through an silicon oxide after/during the applied positive gate voltage for the Modified Fowler Nordheim(MFN) tunneling

The constant gate voltage were on time when the positive currents flowed and were off time when the negative currents flowed. As long as the applied voltages were less than the onset voltage of the tunneling current, the transient currents were represented by the exponential charging and discharging. The central 0 value of vertical axis was used in order to plot both positive and negative currents on the same scale. The central 0 value of vertical axis was 10^{-15}[A] for the positive currents shown in the figures and -10^{-15}[A] for the negative currents shown in the figures.

The transient currents were not exponential decay when the applied voltages were made larger than the onset of tunneling but the transient currents were exponential decay when the applied voltages were made less than the onset of tunneling. The transient currents were subsequently measured at low voltages below the onset voltage of tunneling.

When the voltages applied to the oxide were increased, the stress currents and the transient currents were measured, as shown in figure 3.



(1)

(2)

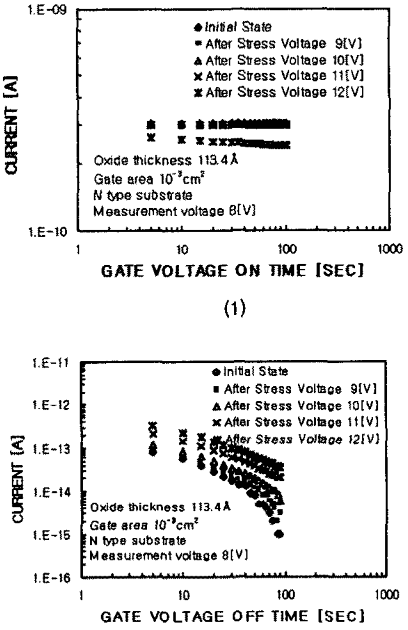
Figure 3 The stress and transient currents through an silicon oxide after/during the applied positive gate voltage for the Fowler Nordheim(FN) tunneling

(1) The stress currents through an silicon oxide during the applied positive gate voltage

(2) The transient currents through an silicon oxide after the applied positive gate voltage

The transient currents when the voltage stresses were on time for the voltages for which FN tunneling was significant. The stress tunneling currents reflected the changes reflected the changes in the shape of the tunneling barrier due to trapping of electrons in the oxides. The transient currents after stress voltage were off time were decayed very slowly. The transient currents followed an exponential decay.

The stress and transient current could be measured was to stress the capacitor at high voltages and then measure the stress and transient currents through the capacitor at applied voltages after the stresses as shown in figure 4.



(1)

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Figure 4 The stress and transient currents through an silicon oxide after stress voltage

(1) The stress currents through an silicon oxide during the applied positive gate voltage 8[V] after stress voltage 9[V], 10[V], 11[V] and 12[V]

(2) The transient currents through an silicon oxide after the applied positive gate voltage 8[V] after stress voltage 9[V], 10[V], 11[V] and 12[V]

The capacitor in this case was stressed at 9[V], 10[V], 11[V] and 12[V] for 100[sec] respectively. The stress and transient currents were measured after the stress at 8[V] for 100[sec].

Higher stress voltages produced higher fluences through the oxides and associated with higher transient currents subsequently measured at low voltages. Both the charging and discharging currents measured at the low voltages rose as the stress fluence rose.

The stress and transient current could be measured was to stress the capacitor at high voltages and then measure the stress and transient currents through the capacitor at applied voltages after the stresses as shown in figure 5.

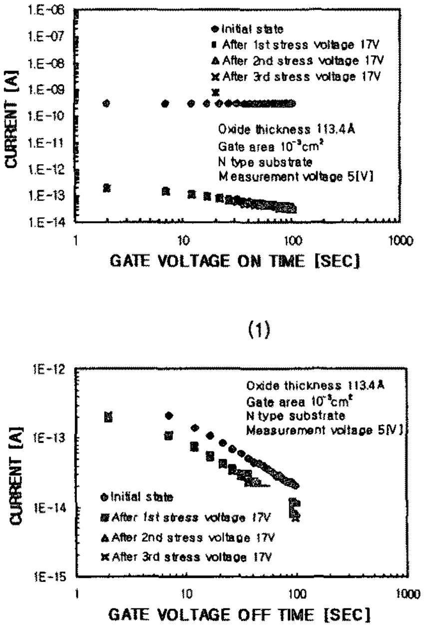

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Figure 5 The stress and transient currents through an silicon oxide after stress voltage

(1) The stress currents through an silicon oxide after the applied pulse voltage 17[V]

(2) The transient currents through an silicon oxide after the applied pulse voltage 17[V]

The capacitor in this case was stressed at 17[V] for 100[sec] respectively. The stress and transient currents were measured after the stress at 5[V] for 100[sec]. Higher stress voltages or longer stress times produced higher fluences through the oxides and associated with higher transient currents subsequently measured at low voltages. Both the charging and discharging currents measured at the low voltages rose as the stress fluence rose.

The stress and transient currents after application of a voltage pulse for an oxide that had been stressed with either positive stress voltage or negative voltage has been shown in figure 6.

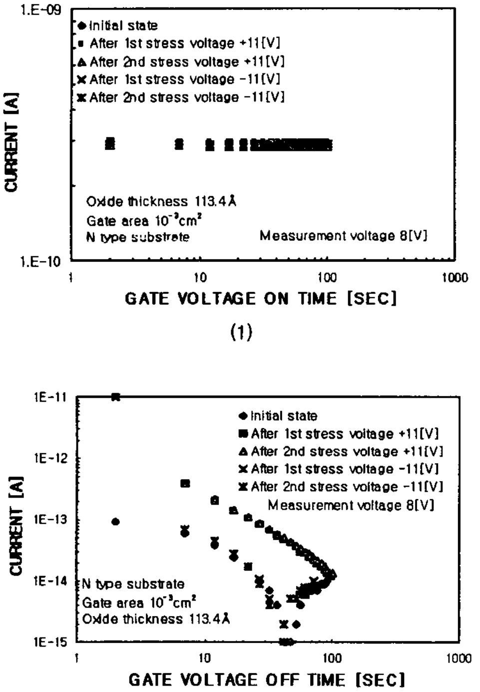

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Figure 6 The stress and transient currents through an silicon oxide after stress voltage

(1) The stress currents through an silicon oxide after the applied pulse voltage ±11[V]

(2) The transient currents through an silicon oxide after the applied pulse voltage ±11[V]

The transient currents following the removal of a ±11[V] pulse have been plotted in figure 6 after both positive gate voltage stressing and negative gate voltage stressing at fluence level of 4.88×10^{-1}C/cm^2 and -6.04×10^{-7}C/cm^2. The capacitor in this case was stressed at ±11[V] for 100[sec] respectively.

The stress and transient currents were measured after the stress at 8[V] for 100[sec]. Higher stress voltages or longer stress times produced higher fluences through the oxides and associated with higher transient currents subsequently measured at low voltages. Both the charging and discharging currents measured at the low voltages rose as the stress fluence rose.

The stress and transient currents measured following high voltage stress were analyzed in terms of the currents predicted by the tunneling front model. The currents equation was used to evaluate whether the transient discharge currents following the turn off of voltage pulses were due to the tunneling front discharging the traps in the oxides.

3. Conclusions

The stress and transient currents associated with voltage pulses applied to thin oxide MOS capacitors have been analyzed in terms of the charging and discharging of stress generated traps in the oxide. The tunneling front model was used to explain the 1/t time dependence of the decay current after application of a voltage pulse. The trap densities derived within the oxide were of the same order of magnitude as the interface trap densities measured at the silicon oxide interface on stressed oxides.

Acknowledgements

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