

Organic Thin Film-Transistor using Pentacene

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Abstract

We fabricated the thin-film transistors using organic semiconductor, pentacene, on SiN_x gate insulator. X-ray diffraction experiments were performed for the sample after heat-treatments at higher temperatures. We confirmed that we obtained “thin-film phase” from the condition used here. From the electrical measurements, we also confirmed that no charges are accumulated at the interface between organic and insulating layer, and FET characteristics of the organic FET using pentacene was discussed.

Introduction

Organic and polymer light-emitting diodes (LEDs) have been investigated for a number of years for possible use in back lighting and display applications. [1] In a simple passive addressing approach, the individual light pixels must be operated at a brightness of $100,000 \text{ cd/m}^2$ for a 1000-line display to maintain the display brightness of 100 cd/m^2 . In this case, the life-time of the device cannot be long enough. An alternative addressing is an active matrix approach. In recent reports, field-effect transistors (FETs) with polycrystalline Si [2] and amorphous Si [3] active channel materials have been integrated with organic LEDs. However, the deposition of the active layers of those FET need high temperature and therefore, it is not good for the flexible display. For the use of flexible substrates, we need room temperature or at least low temperature processes. Organic FET can be one of the solutions. Organic FETs have attracted attention for use in a number of large area applications where high switching speeds are not essential. The performance of organic TFTs has improves dramatically over the last twelve years [4], and optimised organic TFTs now show electrical characteristics similar to those obtained with hydrogenated amorphous silicon (a-Si:H) devices.

There are two major materials for the organic TFTs: one is thiophene based materials and the other is pentacene. The organic TFTs using pentacene have being studied actively by Jacson's group in the Pennsylvania State University and shows very high performances. [5] To improve the quality of the organic/dielectric interface, they had explored self-organizing materials, particularly octadecyltrichlorosilane (OTS). OTS can form well ordered two-dimensional single-monolayer film on SiO_2 . Furthermore, they fabricate the pentacene films twice: one at the substrate temperature of 90°C and the others at 27°C . By this way, the device demonstrated field-effect mobility near $1.5 \text{ cm}^2/\text{V}\cdot\text{s}$, on/off current ratio near 10^8 , near-zero threshold voltage, and subthreshold slope less than 1.6 V/decade .

In this study, we fabricated the TFTs using pentacene on silicon nitride (SiN_x) gate dielectrics, and structural and electrical characteristics were measured after heat treatments on higher temperatures.

Device Fabrication

All transistors were fabricated on N-type silicon using the device structure shown in Fig. 1. The circuits were fabricated in an “upside-down” geometry. The source/drain contacts to the organic active player materials were defined immediately above the gate insulator, and the active materials sublimed above the contacts. The source/drain contacts were defined by photolithography technique.

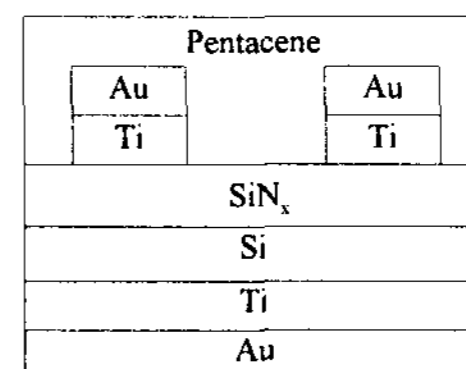


Fig. 1. A schematic cross-section of pentacene TFT

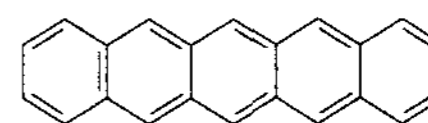


Fig. 2. Pentacene molecule structure

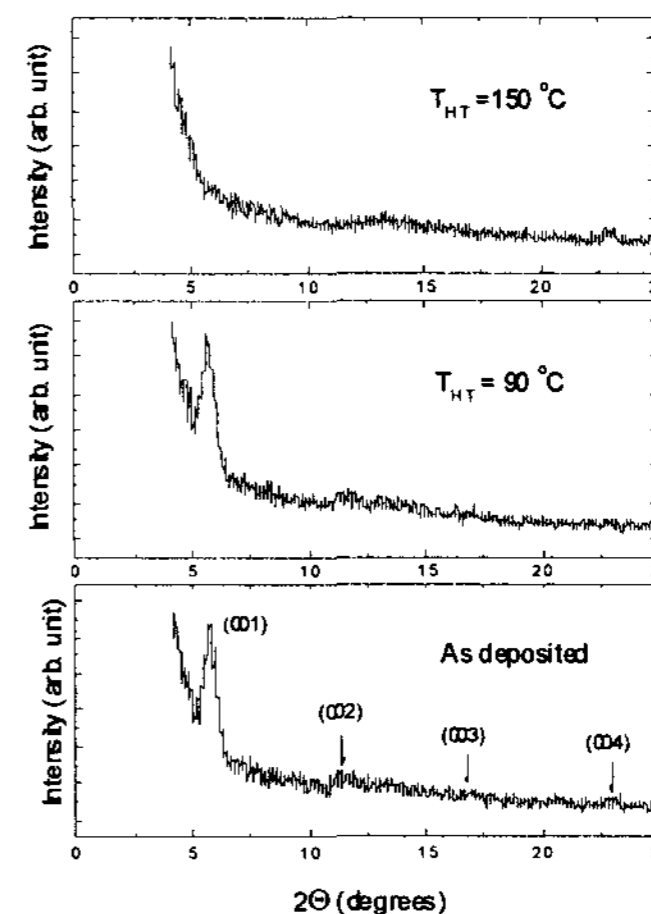


Fig.3. XRD data of pentacene thin films fabricated on SiN_x substrates after heat treatment at given temperatures.

The other side of the Si wafer that acts as a gate contact was coated by Ti/Au bilayer.

Results and Discussion

As shown in Fig. 2, pentacene is small-molecule aromatic hydrocarbon with five benzene rings fused in a straight line. As with α -sexithiophene, evaporated thin film of pentacene tend to show a high degree of molecular ordering.

Fig. 3 shows the x-ray diffraction patterns (XRD) of pentacene thin-films fabricated on SiN_x substrates after heat-treatments at given temperatures. Single-crystal structure of

pentacene is triclinic with space group of C_i^1 . The lattice parameters are as follows [6]: $a=7.90 \text{ \AA}$, $b=6.06 \text{ \AA}$, $c=16.01 \text{ \AA}$, $\alpha=101.9^\circ$, $\beta=112.6^\circ$, and $\gamma=85.8^\circ$. In such structure, the (001) plane spacing d_{001} is about 14.5 \AA . However, as shown in Fig. 3, a crystalline peak was observed at $2\theta=5.78^\circ$ which corresponds to $d=15.33 \text{ \AA}$, and this result must be attributed to a phase different than the single-crystalline phase. This different phase was referred as "thin-film phase". [7] It was reported from the previous report that the "thin-film phase" was dominant at the deposition conditions of low substrate temperature and high deposition rate while the single-crystal phase was dominant at the conditions of high substrate temperature and low deposition rate. [7] In this study, the pentacene films were deposited at room temperature with the deposition rate of about 0.8 \AA/s . The previous work [7] also reported only "thin-film phase" with similar condition with this work.

The pentacene films were heat-treated after deposition at room temperature in vacuum at 90°C and 150°C , respectively, and the XRD data of those films were also shown in Fig. 3. The film heat-treated at 90°C showed almost same XRD pattern with as-deposited film while the film heat-treated at 150°C did not show any peaks corresponds to the crystalline phase. These results are similar with the previous report [8] in which the pentacene films were fabricated on pre-heated substrates. Fig. 4 shows the $I_{DS}-V_{DS}$ curves of the as-deposited sample according to the gate voltage increase. Channel length L and channel width W was 20 \mu m and 3.5 cm , respectively. The pentacene used in the present devices

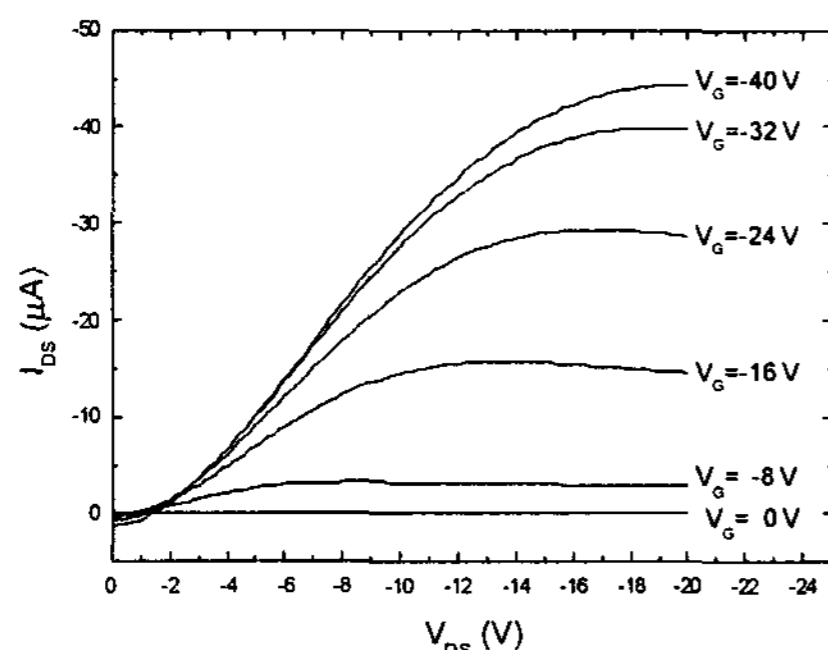


Fig. 4. Plot of drain current vs drain voltage at various gate voltage values.

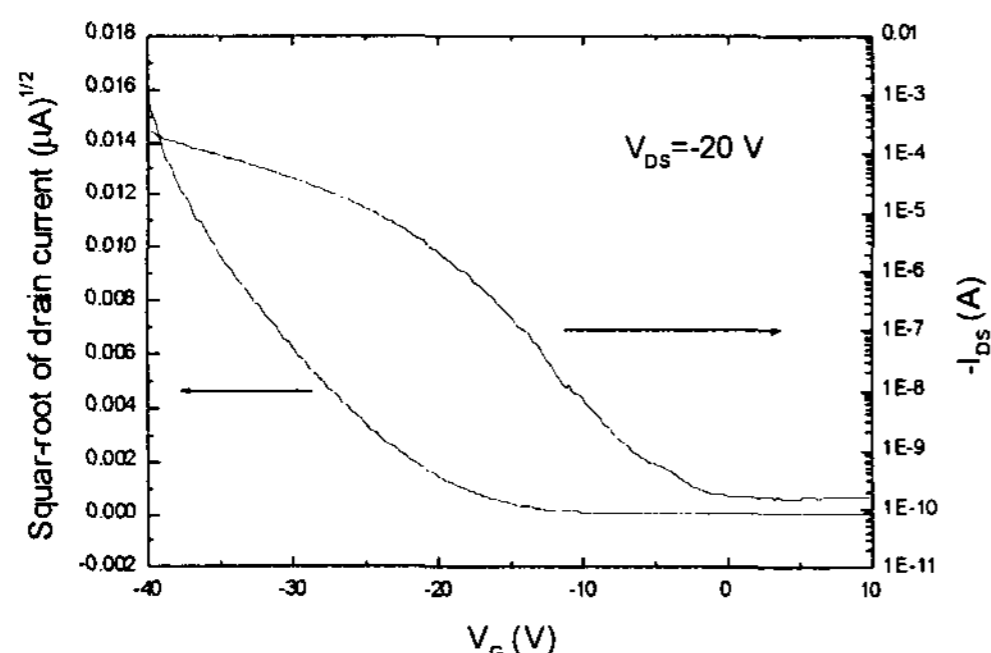


Fig. 5. Plot of drain current (right, y axis) and the square root of drain current (left, y axis) vs gate voltage at a constant drain voltage of -20 V .

behaves as a p-type semiconductor. When the gate electrode is biased negatively with respect to the source electrode (grounded), pentacene FETs operate in the accumulation mode and the accumulated charges are holes.

Fig. 5. Shows the gate voltage dependence of the drain current at the drain voltage of -20 V . As shown in this figure, the drain current increased rapidly when the gate electrode biased negatively. This result is somewhat different from the previous report. [5] According to the report, although the pentacene is an excellent insulator, evaporated pentacene films have a tendency to form a carrier accumulation channel at the substrate interface, and a positive gate voltage is often necessary to deplete the channel. One can say that, from the view of current result, this statement is not general.

From the sample heat-treated at 90°C , we found very similar behavior with figure 4, but the saturation drain current was less than as-deposited sample. From the sample heat treated at 150°C , almost insulating behavior was observed.

Conclusion

Pentacene TFTs on SiN_x gate dielectrics were fabricated at room temperatures and the heat-treatments were performed at 90°C and 150°C , respectively. No XRD pattern change was observed from the sample heat-treated at 90°C , but no peaks were observed from the sample heat-treated at 150°C . From the electrical measurements, FET characteristics with good saturation behavior were observed.

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