Implementation of a Low Power and Reduced EMI Signaling Circuit For a LCD Controller-to-Source Driver Interface

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Abstract

We propose a signaling circuit that can reduce power consumption and Electromagnetic Interference (EMI) in a Liquid Crystal Display (LCD) controller-to-source driver interface. The proposed signaling circuit consists of a coder/decoder that can minimize temporal bit transitions in a transmission line and a current-mode driver that can convert voltage swing into a very small amount of current.

We have simulated the proposed signaling circuit using the HSPICE and the proposed signaling circuit has been designed in a 0.25 μm CMOS technology.

I. Introduction

With rapid progress of the electronic technology, the size of LCD increases. Moreover, the operating frequency, the data width, and the amount of data to transmit of the LCD driving system have increased. In case that a LCD driving system displays a 24-bit true color image, for example, 34 ~ 36 bus lines including three 8-bit data lines (RGB data with 256 gray level), 9 ~ 11 control lines, and clock signal is required at least between a LCD controller and LCD drivers (source and scan driver). To make matters worse, since the maximum frequency of source driver that transmits an image data to LCD is less than 80 MHz, the data width of the driver must be double width (two 24-bit bus lines) of the above example in order to display the resolution of UXGA class. Therefore, it is very important to minimize the power consumption and EMI problem in a LCD driving system.

In order to solve the above problems, we consider reducing the dynamic power dissipation of a CMOS circuit that is dependent upon a load capacitance (C_{load}), a supply voltage (V_{dd}), an operating frequency (f), and activity factor (P_t) as given by Eqn. (1). That is, in order to implement a low power/EMI circuit, we must minimize the C_{load}, V_{dd}, f, or P_t.

$$P = C_{load} \cdot V_{dd}^2 \cdot f \cdot P_t \qquad (1)$$

Since the external capacitances of I/O pins are very larger than the internal capacitance of a chip, the power dissipated in I/O is as low as 10% and as high as 80% of the total power dissipation [1]. In this paper, we propose a signaling circuit that consists of a coding circuit and a current-mode driver in order to reduce power consumption and EMI on highly capacitive inter-chip I/O lines such as a LCD controller-to-source driver interface.

In section II, we propose the proposed coder/decoder that can minimize the switching activities (P_t) and simulation results that is compared the number of transitions. We account for the proposed current-mode driver that converts voltage swing (V_{dd}) to a very little current in section III. In section IV, we explain implementation of the proposed signaling circuit.

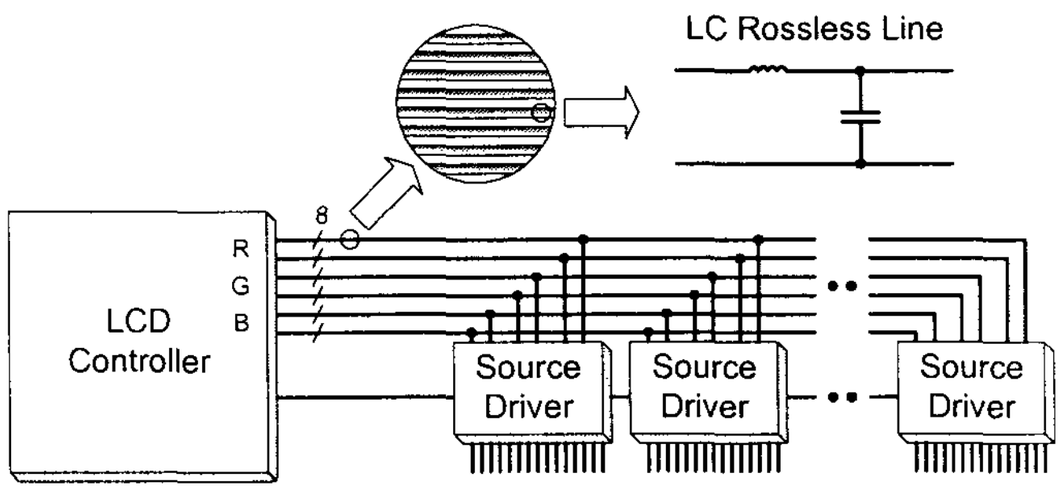


Fig. 1 Interface between a LCD controller and a LCD drivers

II. The Proposed Coder/Decoder

Since the proposed coding/decoding algorithms of the coder /decoder are considered the statistics of the sequence of image data, the proposed methods are a non-redundant coding scheme that does not require any additive control lines and can be easily implemented with less hardware.

We have simulated the proposed methods for three general text images and one landscape image, and compared the number of temporal bit transitions of the proposed methods with those of other coding methods as shown in Fig. 2

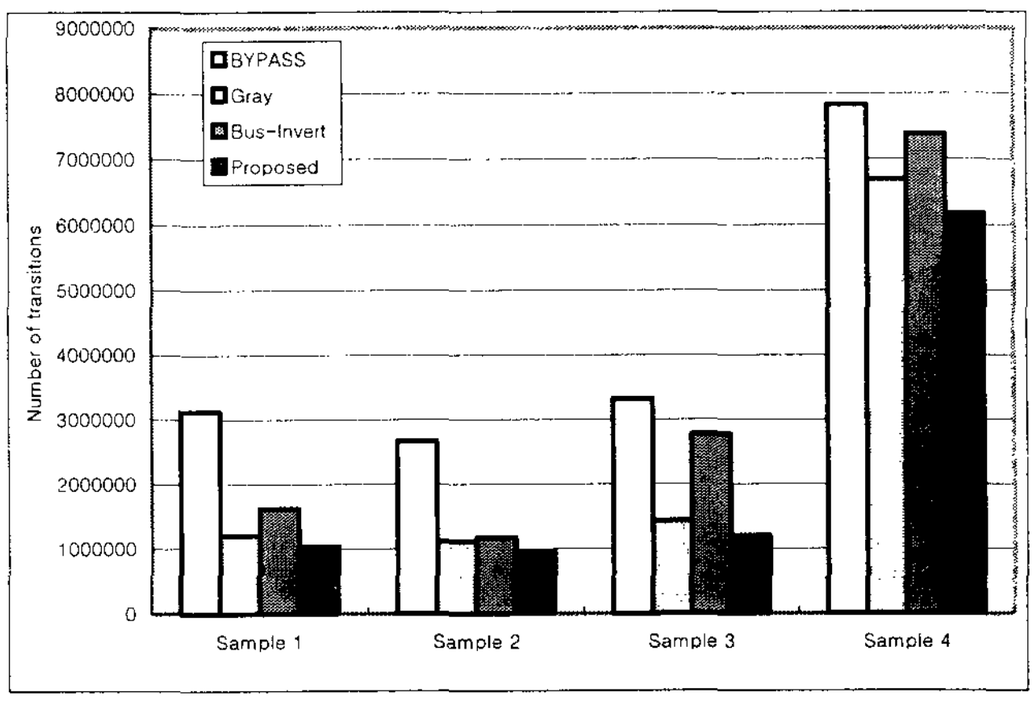


Fig. 2 Comparison of the number of temporal bit transitions for 4 samples

In Fig. 2, we can easily find that the proposed method can significantly reduce the switching activity for both text and landscape images. In particular, the switching activity can be reduced up to 65% in the case of raw text images [2].

III. The Proposed Current-Mode Driver

The proposed current-mode driver drives a very small current that is converted from its corresponding voltage swing in transmission line. Since the structure of the interface between a LCD controller and source driver is similar to a sequential multi-drop bus, the impedance of the transmission line is variable. Therefore, it is required a terminator that prevents a signal reflection in the both transmission line end as shown in Fig. 3.

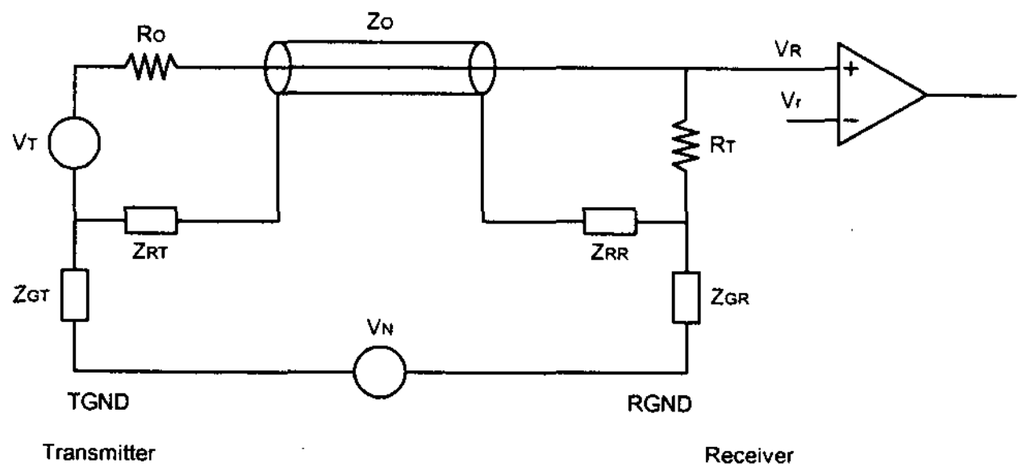
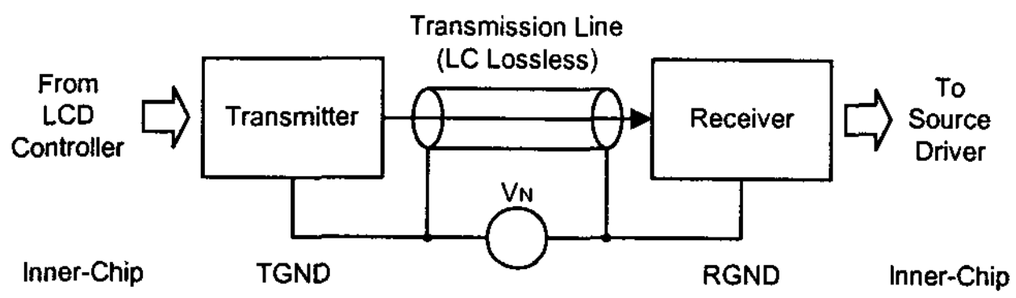


Fig. 3 Structure of the proposed current-mode driver

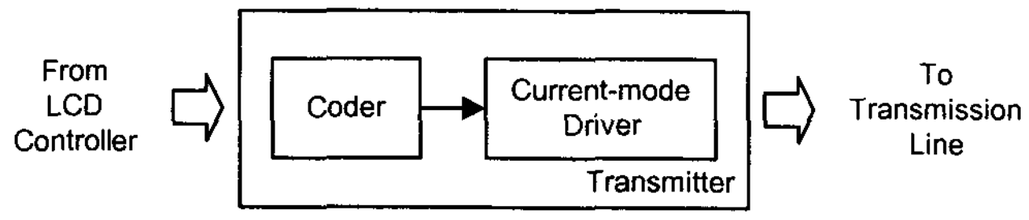
In Fig. 3, the proposed current-mode driver consists of the circuit to remove a noise that is produced in power supply and the reference generator in order to detecting data in receiver. In addition, the proposed driver controls the return impedance by considering cross talk, noise immunity, and traveling wave delay.

IV. Implementation

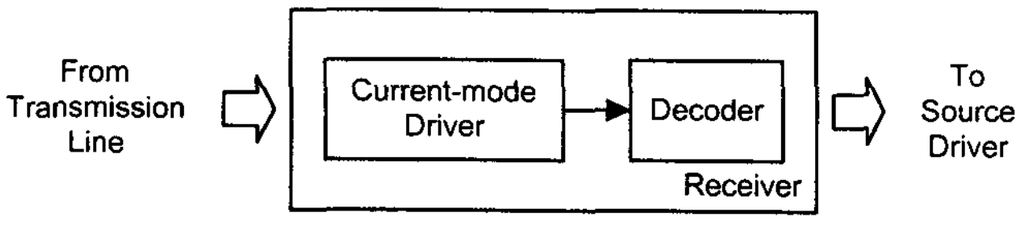
The proposed signaling circuit consists of a transmitter that includes the proposed coder and the current-mode driver and a receiver that consists of the proposed the current-mode driver and decoder as shown in Fig. 4.



(a) Overall Structure of the proposed signaling circuit



(b) Transmitter



(c) Receiver

Fig. 4 The Structure of the proposed signaling circuit

We have simulated the proposed signaling circuit using HSPICE and the proposed signaling circuit has been designed in a 0.25 μm CMOS process.

V. Conclusion

In this paper, we proposed a signaling circuit that can minimize the power consumption and EMI in the PCB lines between a LCD controller and source drivers. The proposed signaling circuit includes the proposed coder/decoder and current-mode driver. The proposed coder/decoder used a non-redundant coding scheme and can significantly reduce the switching activities for both text and landscape images. In addition, the proposed current-mode driver can converts voltage swing into a very little current and have capability to minimize power dissipation and EMI in the transmission line such as interface between a LCD controller and source drivers.

We have simulated the proposed signaling circuit thoroughly using HSPICE. The proposed signaling circuit has been designed in a 0.25 μm CMOS process.

Acknowledgement

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