

# Poly-Si TFT LCD using p-channel TFTs

Yong-Min Ha, Jae-Deok Park, Ju-Cheon Yeo, and Dong-Gil Kim

P-Si process Team, LG.Philips LCD Co., Ltd., 642-3, Jingpyung-dong, Kumi-city, Kyungbuk, 730-360 Korea

## Abstract

Large size poly-Si TFT-LCDs have been fabricated using p-channel thin film transistors for notebook PC application. We have designed and implemented the data sampling circuit and gate drivers that operate with low power consumption and high reliability. The gate driver has a redundant structure. We have realized the uniform and excellent display quality comparable to that of CMOS module. The reliability of panel is investigated and discussed by measuring the bias stability of transistors.

## Introduction

Polysilicon thin film transistor liquid crystal displays have been developed for many years and by many working groups. However, the applications are quite limited to the small size displays such as view finder of camcorder and digital still camera and light valve of projection display while a-Si TFT-LCDs find various applications by improving the quality and the screen size and reducing the cost. The main issues that hindered poly-Si TFT-LCD from penetrating into larger size display market were the less matured technology and the high fabrication cost.

Recently, it has been proved that low temperature poly-Si (LTPS) TFT technology can be applicable to commercial notebook PCs[1]. The progress in the process technology and the equipment for excimer laser crystallization and ion doping enabled the commercialization of LTPS TFT-LCDs. In addition, the product value is improved by making the panel more compact and enhancing the resolution of display. Thus, LTPS TFT-LCDs came to penetrate into the larger size display market for notebook PC.

Nonetheless, the cost competitiveness of large size LTPS has to be improved much more in order to win in the long run. It can not be called as a promising technology for next generation AMLCD without obtaining cost competitiveness with a-Si TFT-LCD since most of a-Si makers rush developing high resolution panels using fine pitch TAB technology.

The main factor of cost increase is fabrication cost. The conventional LTPS TFT process requires much more steps than a-Si TFTs[2,3]. And additional processes such as laser crystallization and ion doping are required, which increases the fabrication cost very much. Further more, as the process steps increase, the process yield decreases. Thus, in order to obtain the cost competitiveness in large size TFT-LCDs over 10 inches, it is needed to simplify the process steps.

We have developed LTPS TFT-LCD using only PMOS transistors instead of CMOS as pixel array switches and driving circuits. It is shown that the PMOS technology can be successfully applicable to the large area TFT-LCDs by investigating the important issues such as the stability of driving circuit, the power consumption in the gate driver, and the performance of TFT-LCD module.

## Panel structure

Fig. 1 shows the schematic diagram of developed LTPS panel. Both pixel switches and peripheral circuitry are implemented only by p-channel TFTs. The gate driving circuit and the data sampling circuit are integrated on the glass. Two gate drivers are integrated on the both edge of panel for redundancy. Normally, both drivers are operating but if there are fails in any stage of the circuits, the

failed output lines are to be cut for repair. The data sampling circuit and the precharge circuit are located on the upper and the lower peripheral area of the display, respectively.

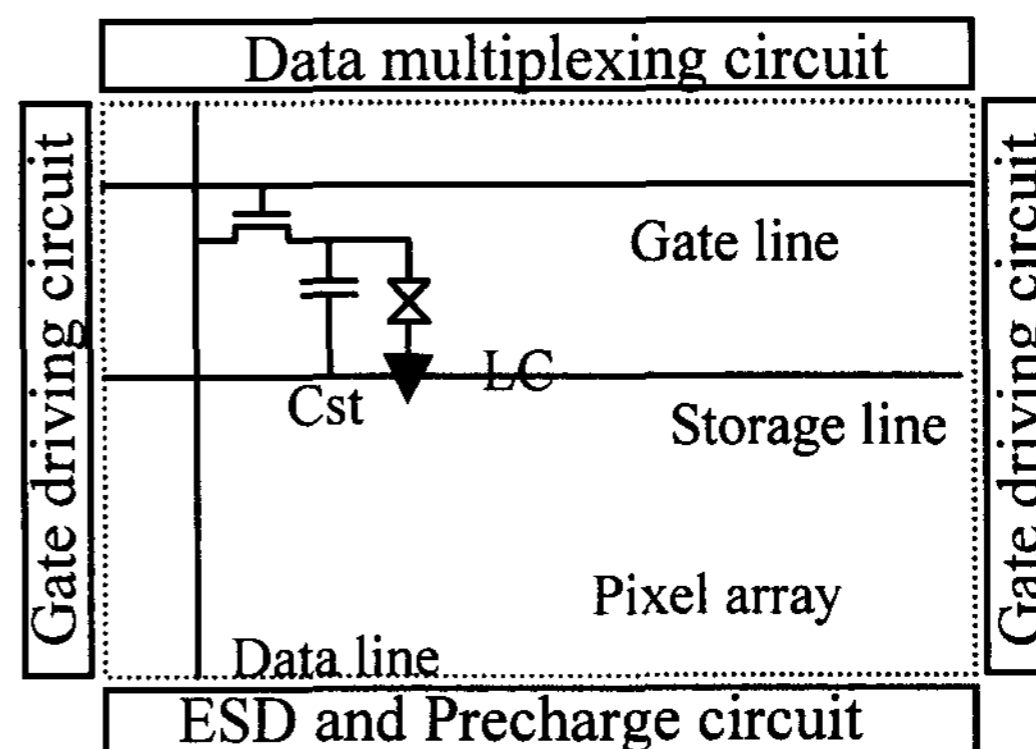


Fig. 1. Schematic diagram of LTPS TFT-LCD.

## Peripheral Circuits

Multiplexing data driving scheme is designed and implemented to reduce the routing area of video signals. Fig. 2 shows the schematic diagram of the data sampling circuits. Only sampling switches are integrated to simplify the circuit. A block sequential driving method has been widely used for conventional poly-Si TFT LCD[4]. However, as the display size increases, the increase of data line delay in video signal can deteriorate picture quality. Multiplexing method can minimize the length of the video line between the data sampling switch and the connecting pad. Furthermore, this scheme has some advantages in obtaining the yield of circuit and testing the driver after the TFT fabrication.

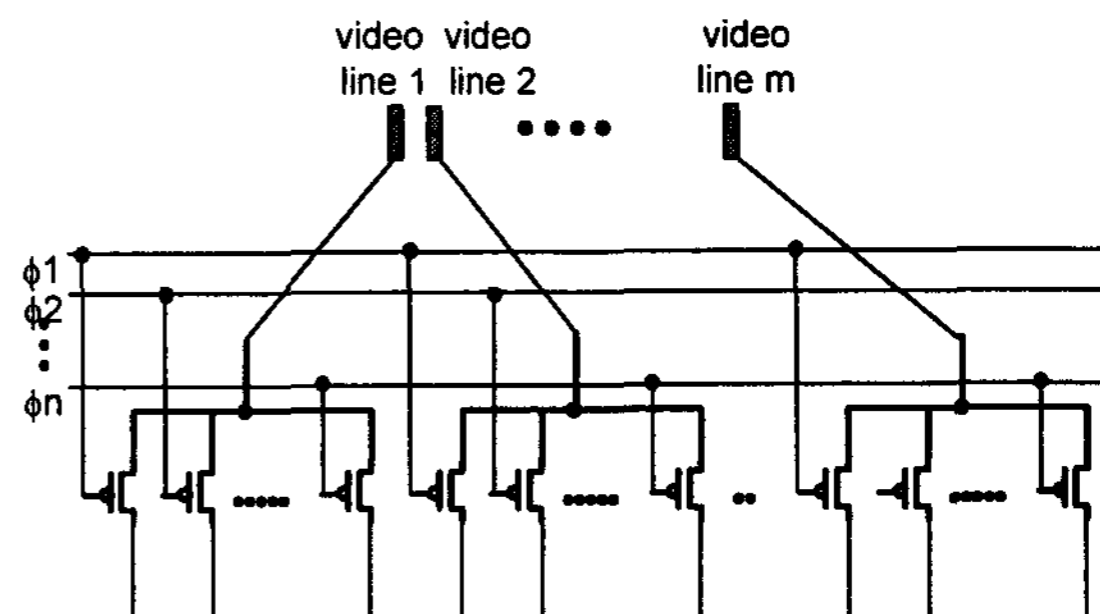


Fig. 2 The schematic circuit diagram of data sampling circuits.

Fig. 3 is the timing diagram of data driving circuit. While a gate bus line is enabled, the data lines are sequentially charged to an analog video data voltage. Before the sampling switches are activated, all data bus lines are charged to a intermediate voltage between positive field and negative field through the pre-charge

circuits on the lower part of pixel arrays.

One of the disadvantages of p-type data sampling circuit is that the current driving capability of p-type switch is lower than that of CMOS switch. The higher gate turn-on voltage is required to maintain the similar series resistance with CMOS switch. But, it is very difficult to increase the gate voltage to the same turn-on resistance level, so the maximum MUX phase of p-type panel is much lower than that of CMOS.

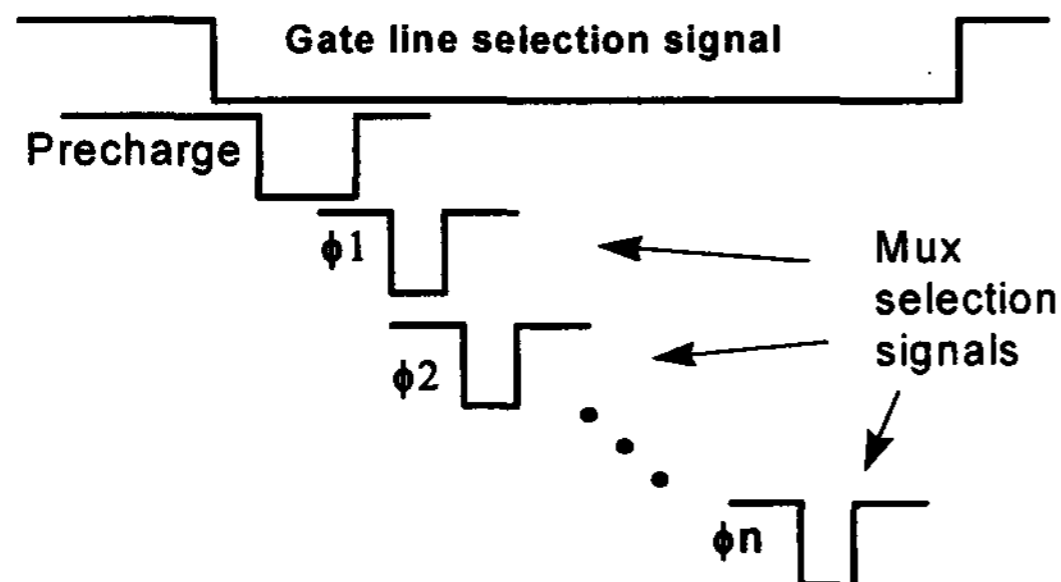


Fig. 3 Timing diagram of data sampling circuit.

We have developed stable and low power consuming shift register as the circuit diagram is shown in Fig. 4. Only 6 transistors are used for one stage and 4 phase clock signals are used to enhance the stability of the shifter register. The shifter register is designed to operate well even though the clock delay occurs on the panel. Further more, the power consumption in the shift register is very low since there is no steady state current path.

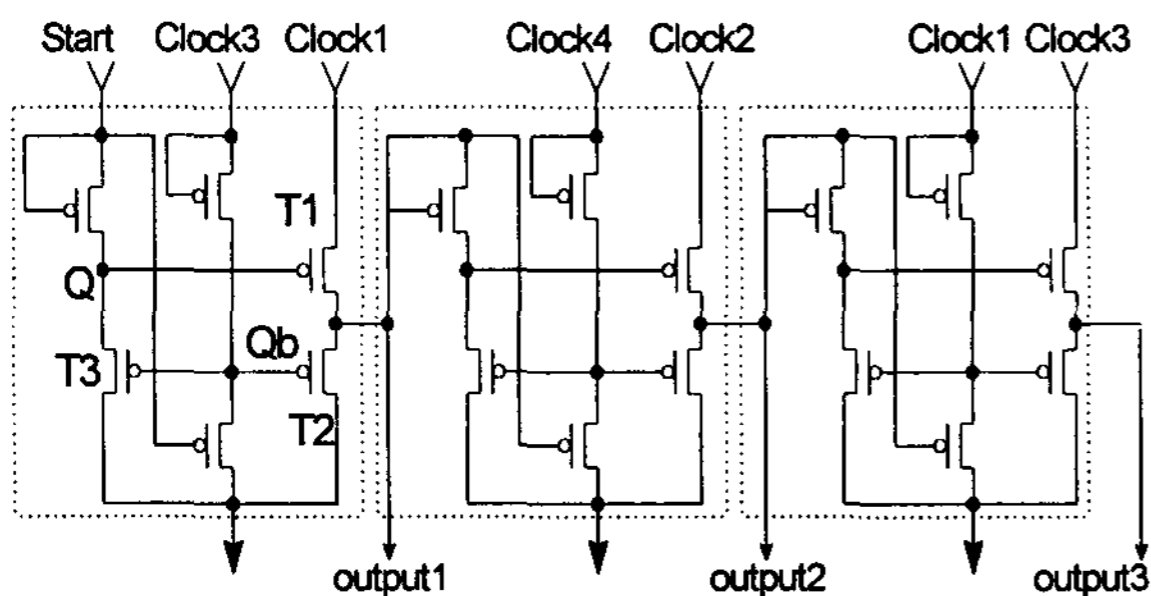


Fig. 4 The circuit diagram of a shifter register.

#### Reliability of PMOS Panel

Since p-type poly-Si TFTs are more immune to the hot carrier stress than n-type devices, p-type circuits can be more stable than CMOS circuits. However, the driving voltage of p-type circuits should be higher than CMOS circuits to overcome the lower switching capability of p-type TFTs. Thus, we have investigated the bias stability of p-type TFTs at high voltage bias conditions.

The reliability has been investigated by measuring the threshold voltage shift after high voltage stress at various gate turn-on biases. Fig. 5 is the threshold voltage variation according to the stress time. We have made simple fitting of experimental data and have estimated the lifetime of the LTPS TFT-LCD panel. Since we have designed the panel to allow the threshold voltage shift of 1.0V, over the lifetime of 10 years can be guaranteed.

#### Characteristics of Module

12.1 XGA module is implemented with only PMOS technology as shown in Fig. 6. The display quality is comparable to that of the CMOS module. Since we have used a conventional

TN mode cell, the picture quality such as contrast ratio, viewing angle, and response time is similar to that of a-Si TFT-LCD. However, since the pixel resolution of LTPS is higher than the commercial 12.1 SVGA, the image is clearer.

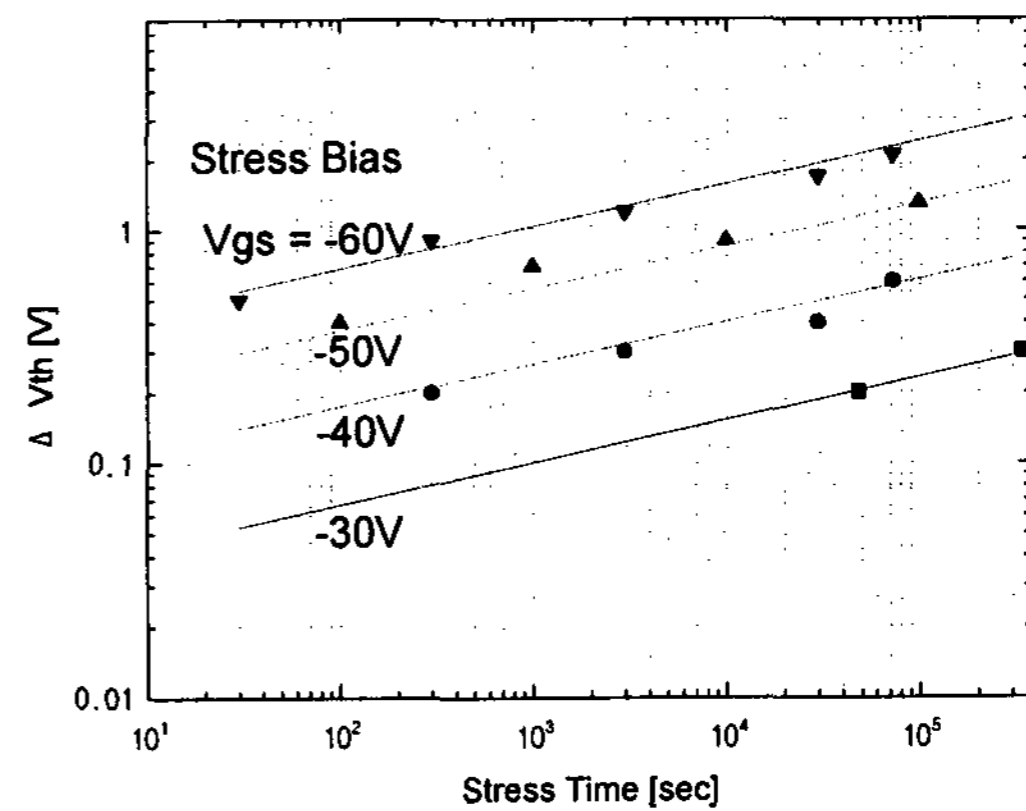


Fig. 5 The variation of threshold voltage after the different gate turn on bias stress. Symbols and solid lines are the measured and the estimated data by simple degradation modeling, respectively.

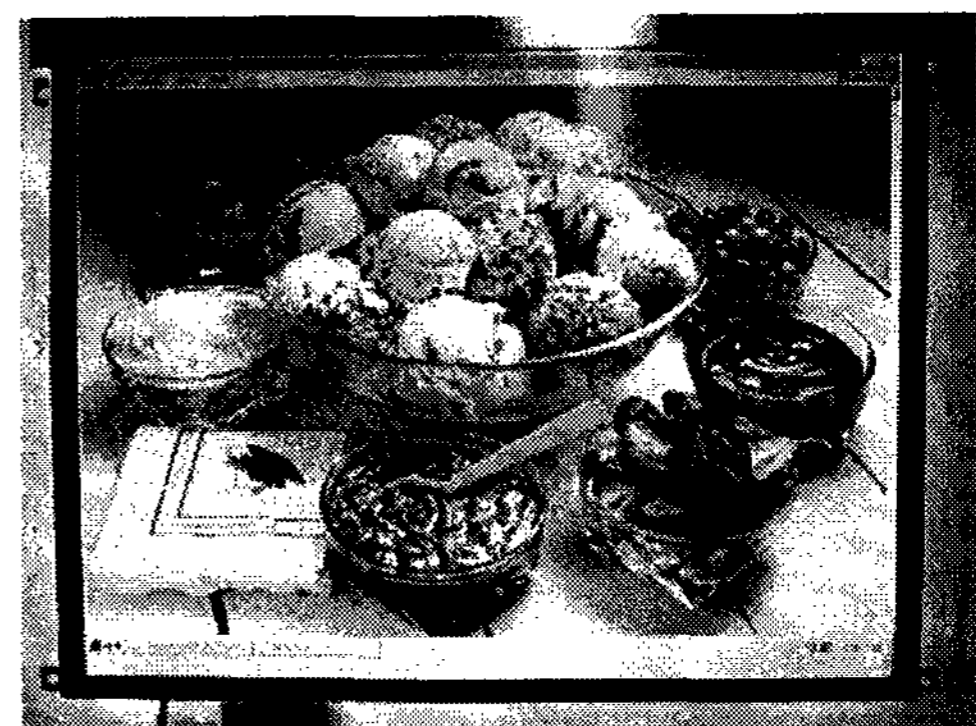


Fig. 6 The photograph of 12.1XGA module.

#### Conclusion

We have shown that the p-channel TFTs can be used for the pixel switches and the peripheral driving circuits of large size poly-Si TFT-LCDs. The picture quality is good enough to be used in notebook PCs. Furthermore, we have investigated the reliability of panel by measuring the stability of transistors after high voltage stress. Our p-type technology can improve the performance and reduce the fabrication cost.

#### Acknowledgement

This work was supported by G-7 project program.

#### References

- [1] Y. Aoki; T.Iizuka; S. Sagi; M. Karube; T. Tsunashima; S. Ishizawa; K. Ando; H. Skurai; T. Ejiri; T.Nakzono; M. Kobayashi; H. Sato; N. Ibaraki; M. Sasaki; N. Harada, SID 99 Digest, pp176-179.
- [2] M. Itoh; Y. Yamamoto; T. Morita; H. Yoneda; Y. Yamane; SS. Tsuchimoto; F. Funada; K. Awane, SID 96 Digest, pp17~20.
- [3] K. Yoneda, Workshop Digest of the 18<sup>th</sup> IDRC (Asia display 98), pp75-82.
- [4] F. Okumura, et. al, SID 94 Digest, pp79~82.