Electrical Characteristics of Pentacene Thin Film Transistors.

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Abstract

There are currently considerable interest in the applications of conjugated polymers, oligomers, and small molecules for thin-film electronic devices. Organic materials have potential advantages to be utilized as semiconductors in field-effect transistors and light-emitting diodes. In this study, pentacene thin-film transistors (TFTs) were fabricated on glass substrate. Aluminums were used for gate electrodes. Silicon dioxide was deposited as a gate insulator by PECVD and patterned by reactive ion etching (R.I.E). Gold was used for the electrodes of source and drain. The active semiconductor pentacene layer was thermally evaporated in vacuum at a pressure of about 10^{-8} Torr and a deposition rate 0.3 Å/s. The fabricated devices exhibited the field-effect mobility as large as 0.07 $cm^2/V.s$ and on/off current ratio as larger than 10^7.

Keywords: Organic thin film transistors; pentacene; evaporation; field-effect mobility; on-off current ratio.

1. Introduction

Some organic materials have received considerable attention as semiconductors for the device applications such as light emitting diodes[1] and thin film transistors (TFTs)[2]. They can offer potential advantages in terms of the processing simplicity and cost. The field of flat panel display is one of the most attractive applications for organic semiconducting materials. In active matrix liquid crystal displays (AMLCDs), for example, where amorphous silicon thin film transistors are used as a pixel-switching device, the adoption of organic TFTs would allow the all-organic display system, which is easy and cheap to fabricate, and flexible[3]. In this study, pentacene TFTs were fabricated on glass substrate. Aluminum and gold were used for the gate and source/drain electrodes respectively. Silicon dioxide was deposited as a gate insulator by PECVD and etched by R.I.E. for patterning. Electrical characteristics of the TFTs were represented by the field-effect mobility, threshold voltage and on-off current ration.

2. Device Fabrication

The schematic cross-sectional structure of a pentacene TFT is shown in Fig 1. Aluminum was used for the gate electrode, which was deposited on the glass substrate by the conventional thermal evaporation at a pressure of about 10^{-6} Torr, patterned by the lift-off method, and annealed during 1Hr at 400℃. Silicon dioxide was deposited by PECVD, which is the gate insulator. During the SiO_2 deposition, the substrate was held at 300℃. The gate insulator layer was patterned by reactive ion etching (RIE), where CF_4/O_2 chemistry was used with 25W rf power. The etching rate was about 53 nm/min at a pressure 0.1 Torr. Silicon dioxide thickness was about 100 nm. Then, gold was deposited on the gate insulator by the conventional thermal evaporation to be used for the source/drain electrodes. The thickness of the source/drain metal was 130 nm.

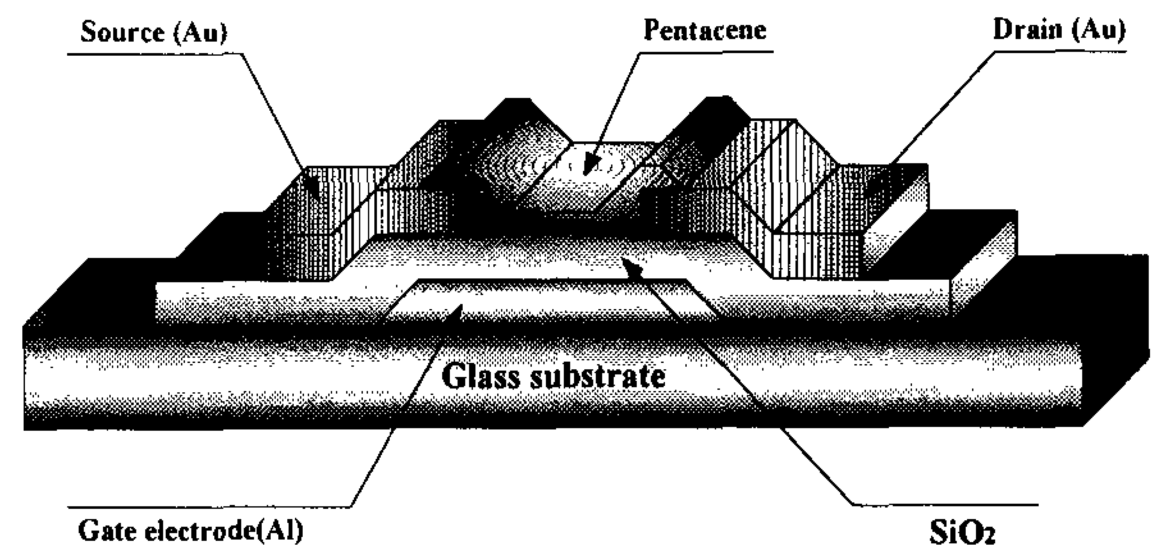

Fig. 1. The schematic cross-section of the pentacene TFT fabricated in this study.

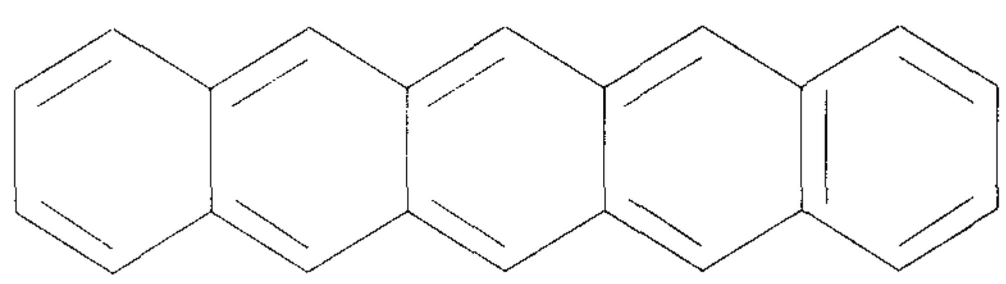

Fig. 2. The molecular structure of pentacene.

3. Results and Discussion

The transfer characteristics of pentacene thin film transistors, whose channel lengths are 50, 100, 200, and 250 ㎛ respectively, are presented in Fig 3. The channel width of all the devices is 5 ㎜. The drain bias was 2 V and the gate bias varied from 0V to –20V for the measurements. The on/off current ratio of those devices is as large as 10^7, which are one of the best data. The mobility and threshold voltage were extracted from the I_D vs. V_G data measured in the saturation regime, where the drain is shorted to the gate of the TFT, based on the equation [4]:

$$I_{DS} = \frac{W}{L}\frac{C_i}{2}\mu (V_G - V_{th})^2$$

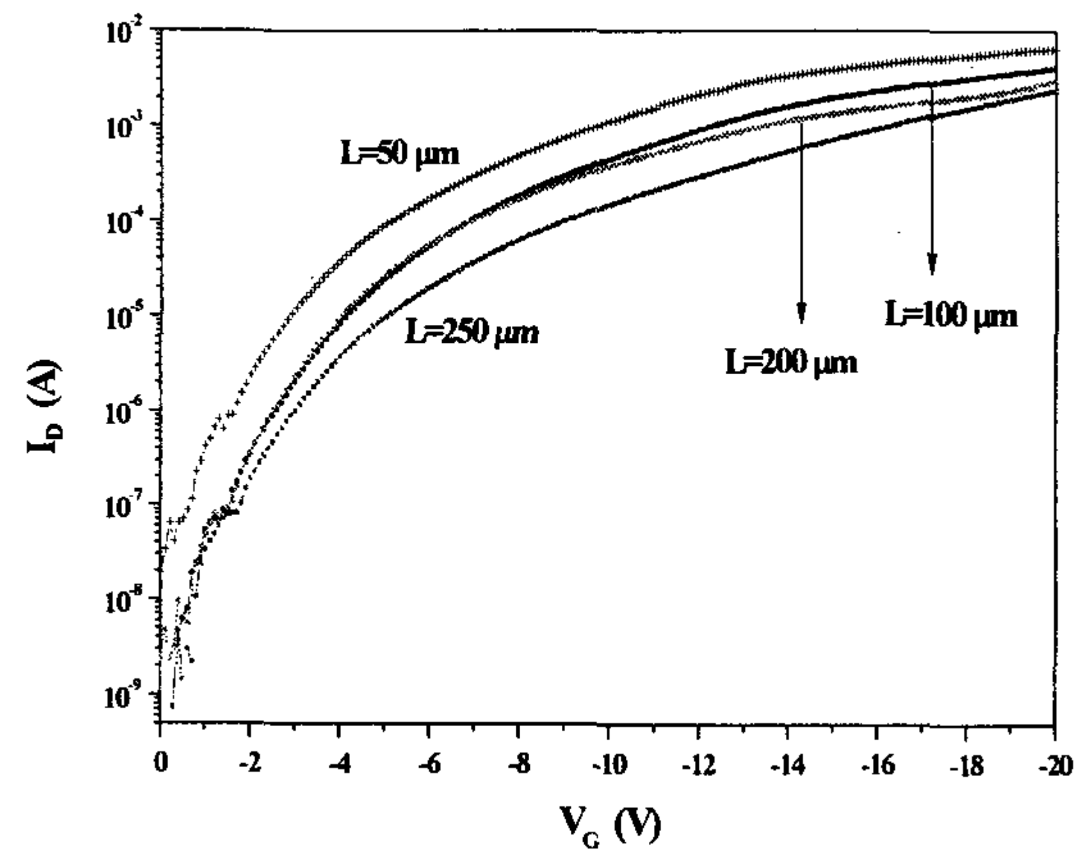

Fig. 3. Transfer characteristics of pentacene TFT with gate lengths of 50, 100, 200, 250 ㎛, width of 5 ㎜ (V_D = 2V).

where μ is the field-effect mobility, L and W are channel length and width, respectively, C_i is the gate capacitance per unit area(for 1000 Å SiO_2, C_i is 35 nF/cm^2), and V_{th} is the threshold voltage. Fig. 4 shows the procedure to extract the field-effect mobility and threshold voltage from the plot of $I_D^{1/2}$ vs. V_G. The field-effect mobility is as large as 0.07 $cm^2/V{\cdot}sec$, which is remarkably high if it is taken account of that the pentacene layer was deposited by the plain thermal evaporation under about 10^{-6} Torr pressure and the substrate was held at room temperature. Moreover, the threshold voltage is as low as –3.30 V, which is one of the lowest turn-on voltages ever reported. The high mobility and on-off current ratio, and low threshold voltage of the fabricated TFTs are thought to be attributed to the plasma treated surface of the silicon dioxide during the CF_4/O_2 plasma etching, which formed the semiconductor-insulator interface. If an effusion cell is to be used under lower pressure(10^{-9}) Torr and the substrate temperature is raised higher, the purer and better-ordered pentacene layer could be obtained to provide the much improved transistor characteristics that can be comparable to those of amorphous silicon thin film transistors. An all-organic TFT can be realized if the SiO_2 is replaced by an organic dielectric medium as a gate insulator with conducting organic electrodes.

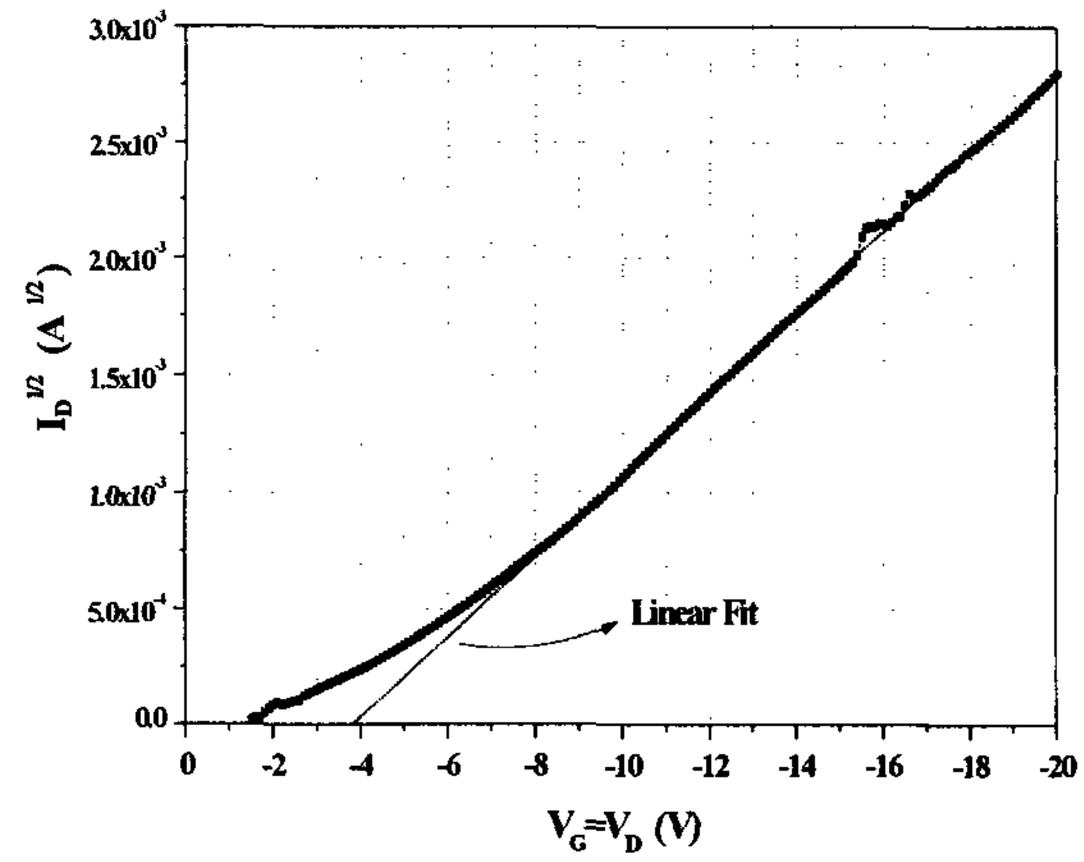

Fig. 4. Field-effect mobility and threshold voltage extraction from the measured $I_D^{1/2}$ vs. V_G in the transistor saturation region(V_D = V_G).

4. Conclusions

Pentacene TFTs was fabricated on the glass substrate. Aluminum and gold were used for the gate and source/drain electrodes. Silicon dioxide was deposited by PECVD and patterned by R.I.E. as a gate insulator. The pentacene semiconducting layer was thermally evaporated in vacuum at a pressure about 10^{-8} Torr with a deposition rate 0.3 Å/sec. Electrical characterizations of the TFTs show that the field-effect mobility is as large as 0.07 cm^2/Vs, on/off current ratio over 10^7, and threshold voltage as low as –3.30 V. The SiO_2 surface treatment of CF_4/O_2 plasma during the etching seems to be attributed to the formation of the good semiconductor-insulator interface for charge carrier transportation along it. If an effusion cell is used under lower pressure(10^{-9}) Torr and the substrate temperature is raised higher, the purer and better-ordered pentacene layer could be obtained to provide the much improved transistor characteristics that can be comparable to those of amorphous silicon thin film transistors.

Acknowledgements

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