Stability of Amorphous Silicon Thin-Film Transistor using Planarized Gate

Young Jin Choi, In Keun Woo, Byung Cheon Lim* and Jin Jang

Department of Physics, Kyung Hee University, Seoul 130-701, Korea
*LCD SBU, Hyundai Electronics Industry, Kyungki-do 467-701, Korea

Abstract

The gate bias stress effect of the hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) with a SiN_x/BCB gate insulator have been studied. The gate planarization was carried out by spin-coating of BCB (benzocyclobutene) on Cr gates. The BCB exhibits charge trappings during a high gate bias, but the stability of the TFT is the same as conventional one when it is between –25 V and +25 V. The charge trap density in the BCB increases with its thickness.

Introduction

Thin-film transistors (TFTs) including an active layer of hydrogenated amorphous silicon (a-Si:H) have been widely employed as the pixel-driving element of a liquid crystal display (LCD) [1].

When employing a-Si:H TFT array in a liquid crystal display, the main issues are to reduce RC line delay, to increase the field effect mobility of TFT and to increase the productivity in order to apply that to high resolution, large-area TFT-LCDs. RC gate line delay causes gray-scale errors due to lack of synchronization and insufficient charging to pixels because of the distortion in gate pulse [2]. To decrease RC delay, low resistive gate metal, wide and thick gate line are required. But wider gate line decreases the aperture ratio and thicker gate line yields a step-coverage problem, which can be overcome by adopting a planarized gate [3]. Therefore, a gate planarization is important for high-performance, large-area, high-definition active-matrix (AM) LCD.

On the other hand, double-layered gate insulators such as SiN_x/SiO_2 [4], SiN_x/SiON [5] and SiN_x/Al_2O_3 [6] have been adopted for a-Si:H TFTs to increase the production yield, because the pinhole density can be reduced by introducing a double-layered gate insulator. BCB (Benzocyclobutene) exhibits a low dielectric constant (2.7), a good planarization property (> 90 %) and a high optical transmittance (> 95 %) in the visible region [7]. In addition, the leakage current and the field strength of BCB were 2.1 $fA/\mu m^2$ and 4.2 MV/cm^2, respectively [7]. Therefore, the BCB can be used as a gate insulator.

In this work, we have studied the stability of the TFT under gate bias and the effect of reducing SiN_x thickness on its performance. The performance of double-layered gate insulator of SiN_x/BCB for an a-Si:H TFT have been studied. [8-9].

Device Fabrication

The inverted staggered a-Si:H thin film transistors (TFTs) were fabricated. First, Cr metal was deposited on glass substrate by sputtering and then patterned for gates. BCB was coated on the sample using a spin coater. Curing of the BCB in a convection oven at 250 °C for 1 hr results in a thickness of 700 nm. The BCB layer was etched by CF_4/O_2 plasma in order to control BCB thickness. Then, silicon nitride, undoped a-Si:H and n^+ a-Si:H were deposited on the BCB in a PECVD reactor without breaking the vacuum.

The SiN_x was deposited using a mixture of SiH_4 and NH_3 at a substrate temperature of 300 °C, and undoped a-Si:H was deposited from a gas mixture of H_2 and SiH_4 at 300 °C. The thicknesses of a-Si:H and n^+ a-Si:H layers were 150 nm and 50 nm, respectively. The n^+ a-Si:H, of resistivity ~ 100 Ωcm, was used to ensure ohmic contacts with the source/drain Ni metals. The 100 nm thick Ni layer on the n^+ a-Si:H was deposited by RF sputtering and source/drain contacts were defined using photolithography. The ratio of channel width to length of the TFT was 96 μm/12 μm.

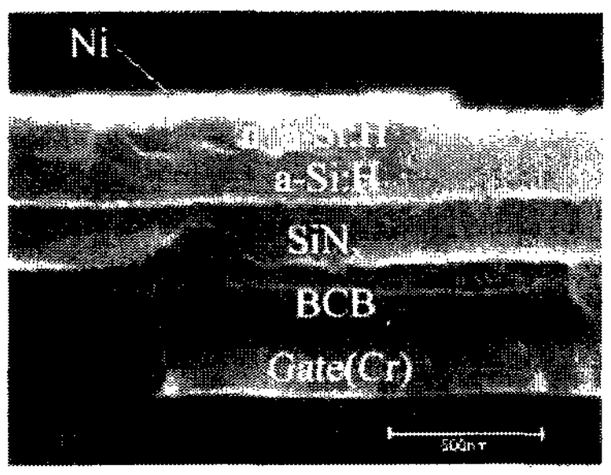

Fig. 1. A cross sectional SEM image of an a-Si:H TFT using a planarized gate insulator

Results and Discussion

Figure 1 shows a cross-sectional scanning electron microscope (SEM) image of a gate planarized a-Si:H TFT using a SiN_x/BCB. Note that there is no step between gate and source/drain, indicating a perfect planarization.

In order to check the bias stress effect of the TFT in high gate bias region, the hysteresis behavior of the transfer characteristics has been investigated. The transfer characteristics were measured during gate voltage scans from –30 V to +30 V, +30 V to –30 V, –30 V to +40 V, +40 V to –30 V, –30 V to +50 V, +50 V to –30 V, –30 V to +60 V, and +60 V to –30 V. The scan speed was 1 V/sec. The results are shown in Fig. 2. There is no shift when the gate voltage scan from –30 V to +40 V. But the transfer curve shifts to the left-hand side when the maximum gate scan voltage is +50 V because of the hole trappings into BCB.

Figure 3 shows the transfer characteristics of the a-Si:H TFT measured during gate voltage scans from +30 V to –30 V, –30 V to +30 V, +30 V to –40 V, –40 V to +30 V, +30 V to –50 V, –50 V to +30 V, +30 V to –60 V, and –60 V to +30 V after V_g scan from –30 V to +60 V. This experiment was to see the detrapping of holes from the BCB after the hole trapping into the BCB by a scan to +60 V. When the scan voltage reaches –60 V, the transfer curve become almost the same as the initial one. Note that the curve return to the initial one by annealing at 210 °C for 90 min.

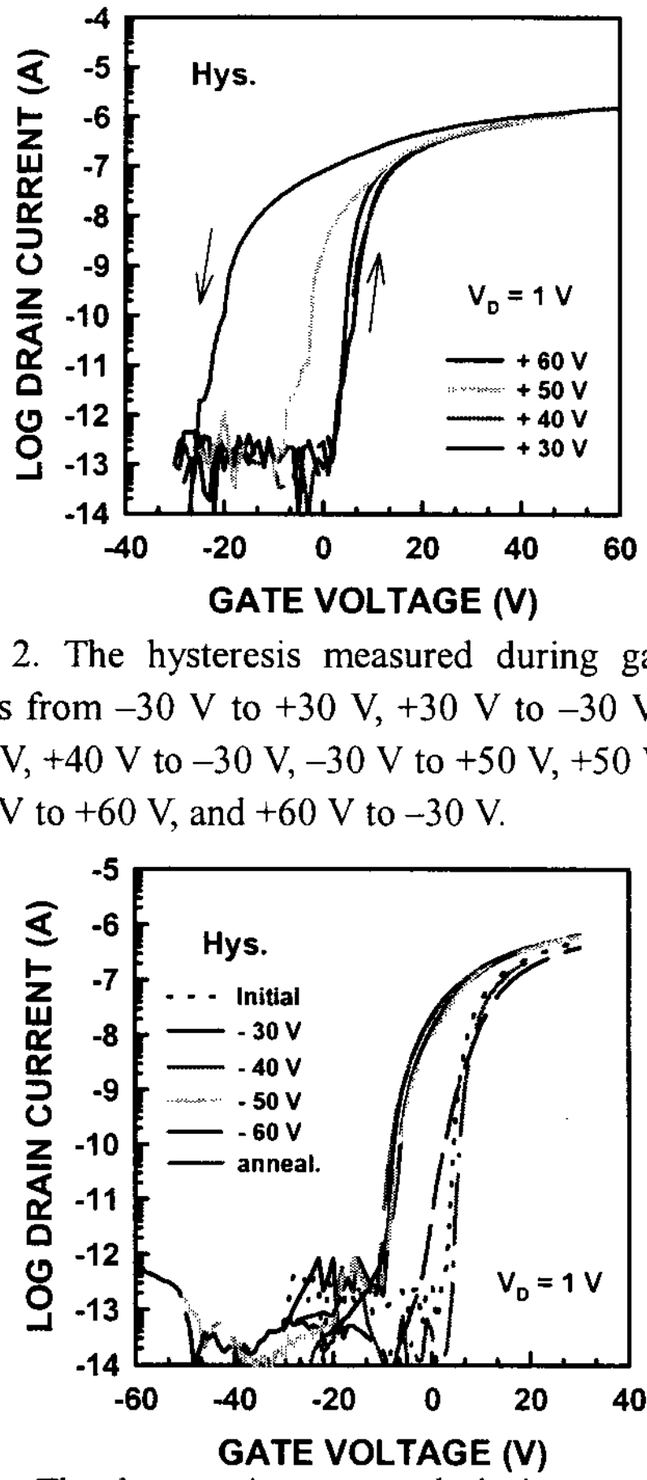

Fig. 2. The hysteresis measured during gate voltage scans from –30 V to +30 V, +30 V to –30 V, –30 V to +40 V, +40 V to –30 V, –30 V to +50 V, +50 V to –30 V, –30 V to +60 V, and +60 V to –30 V.

Fig. 3. The hysteresis measured during gate voltage scans from +30 V to –30 V, –30 V to +30 V, +30 V to –40 V, –40 V to +30 V, +30 V to –50 V, –50 V to +30 V, +30 V to –60 V, and –60 V to +30 V after V_g scan from –30 V to +60 V.

Figure 4 shows the threshold voltage shift of the gate planarized TFTs with various bias voltage. The threshold voltage does not change under gate biasing between –25 V and +25 V comparing to conventional one. But, beyond this range the threshold voltage shifts with gate bias voltage because of the carrier trappings into the BCB.

Figure 5 shows the threshold voltage shift under a gate bias stress at + 40 V with various BCB thicknesses. The threshold voltage shift increases with BCB thickness.

The carrier trappings into the BCB of an a-Si:H TFT do not appear during gate bias stress when it is between –25 V and +25 V. Therefore, the gate planarized a-Si:H TFTs can be utilized in the manufacturing of LCD.

The increase in the thickness of gate metal, which is available in planarized TFT causes a lower RC delay, and allows to use more resistive metals such as Cr, Mo, and Ta without RC delay problem. The taper etching that is necessary process for the TFT-arrays, can be avoided in the gate planarized TFT.

The production yield can be enhanced by adopting a double layered, gate insulator. Therefore, the planarized TFTs are promising for the fabrication of low cost, large-area TFT-LCDs. The SiN_x thickness can be reduced in the gate planarized TFT because of no step in the SiN_x. This is an additional advantage of BCB as a first gate insulator.

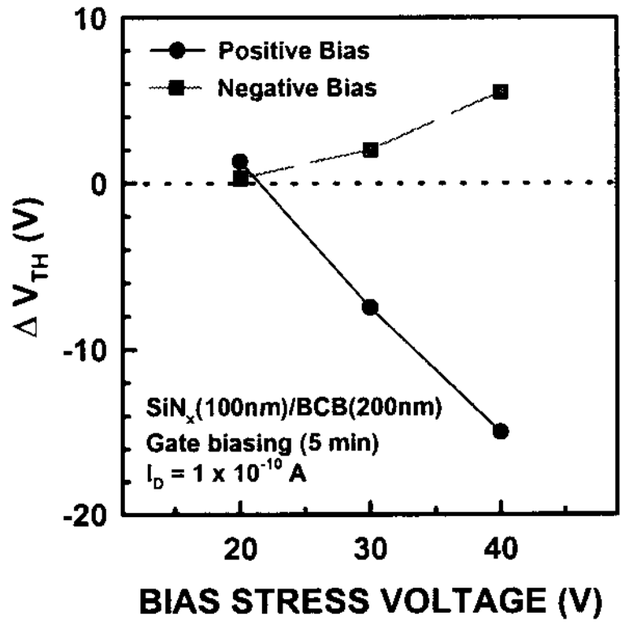

Fig. 4. The threshold voltage shift of the gate planarized TFTs with various bias stress voltage

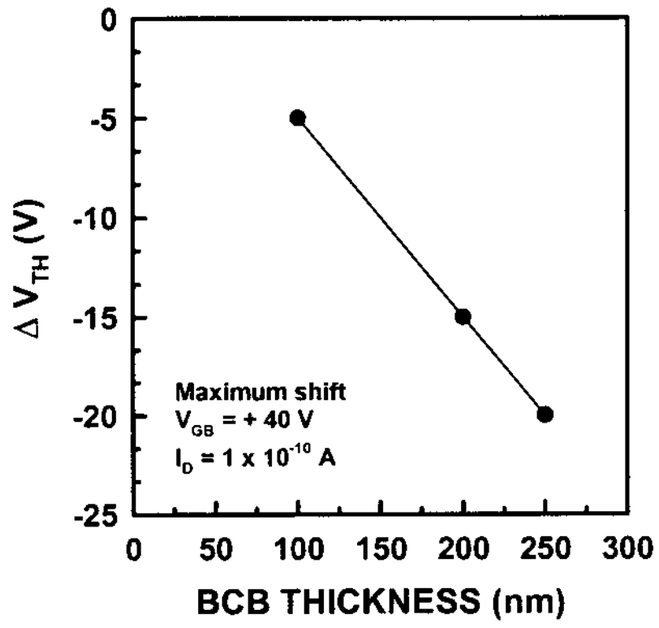

Fig. 5. The threshold voltage shift under a gate bias stress at + 40 V with various BCB thickness

Conclusion

A planarized SiN_x/BCB gate insulator has been successfully adopted for the a-Si:H TFTs. The increase in the thickness of gate metal and lower cross-over capacitance in TFT array allows lower RC delay, and to use more resistive metals like Cr or Mo without RC delay problem. The taper etching that is necessary process in conventional TFT arrays can be avoided in the planarized TFT. Therefore, the planarized a-Si:H TFTs are promising for large-area TFT-LCDs. But a higher gate bias over 25 V results in charge trappings into BCB from the gate.

References

[1] F. B. Ellis, Jr., R. G. Gordon, W. Paul, and B. G. Yacobi, *J. Appl. Phys.* 55, 4309 (1984).

[2] R. L. Wisnieff, *Proceedings of the SID* 29, 173 (1988).

[3] K. Kato, N. Kakuda, M. Okamura, N. Naito, M. Oka, K. Masuda, T. Wada, S. Kohda, and T. Kawada, *Proceedings of the SID* 32, 109 (1991).

[4] K. Fukuda and N. Ibaraki, *22nd Conference on Sol. Stat. Dev. and Mat.*, 1027 (1990).

[5] T. S. Jen, S. T. Leu, T. C. Chou, J. W. Hong, and C. Y. Chang, *Jpn. J. Appl. Phys.* 33, L977 (1994).

[6] T. Tsukada, *Mat. Res. Soc. Symp. Proc.* 284, 371 (1993).

[7] D. J. Perittie, M. J. Radler, and T. Takahashi, *Asia Display '95*, 721 (1995).

[8] B.C. Lim, C.S. Kim, J.H. Choi, M. Radler, and J. Jang, *AMLCD '98 Digest of Technical papers*, 74-76 (1998).

[9] J. Jang and B.C. Lim, *SID Int. Symp. Digest of Technical Papers 1999*, (1999)