A high frequency CMOS precision full-wave rectifier

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Abstract

In this article, the realization of a precision full-wave rectifier circuit for analog signal processing, which operates throughout in the current domain, is presented. The circuit makes use of a MOS class B/AB configuration, and provides a wide dynamic range and wide-band capability. The rectifier has a simple circuit configuration and is suitable for implementing in CMOS integrated circuit form as versatile building block. The characteristic of the circuit exhibits a low distortion in the output signal at low level input signal. PSPICE simulation results demonstrating the characteristic of the proposed circuit are included.

1. Introduction

An absolute value circuit or a precision rectifier is one of important circuit building block used in analog signal processing systems. Usually, precision rectifiers exhibit significant zero-crossing distortion. The classical approaches to realize a precision rectifier are based on the use of operational amplifiers (op-amp) and diodes [1] or bipolar transistors operating in class B [2], [3]. These approaches exhibit the output distortion evident during the zero-crossing of the low-level input signal due to the delay caused by the switching between "on" and "off" state of diodes or bipolar transistors. Alternatively, an approach based on the use of operational-amplifier supply-current sensing technique has been shown to realize a precision rectifier [4]. This approach requires the signal current much greater than the op-amp bias current to avoid nonlinearity error due to the op-amp characteristic [5]. In addition, two approaches to improve the nonideal precision rectifier performance based on current mode technique, which is demonstrated the use of current conveyors and diodes as the active elements, have been reported in literature [6], [7]. These approaches used the diodes biased to the edge of conduction to reduce the delay and improve high frequency performance. In CMOS technology, the diodes can replace by a drain-gate-connected MOS transistor [8]. However, the MOS diodes exhibit the nonideal V-I characteristic. The realization of a CMOS full-wave rectifier can be implemented by the use of op-amp and MOS transistors operating in class B [10]. The high frequency limitation of this scheme is due to the finite gain bandwidth product of the op-amp and the delay caused by switching of MOS transistors. Another approaches are based on a CMOS class AB configuration [11], [12]. These approaches require the signal current greater than four times of the bias current to avoid square law error of MOS transistors. Recently, there has been much effort to reduce the supply voltage of analog CMOS systems. This is due to the demand of portable and battery-powered equipment. The purpose of this paper is to propose a CMOS circuit technique for the realization of a low-voltage precision full-wave rectifier circuit. The resulting performances of the proposed circuit have high accuracy and wide-band capability.

2. Circuit description

The proposed high frequency CMOS precision full-wave rectifier is shown in figure 1. The transistor M_4 and the current source I_1 generate a constant voltage V_B to provide a prebias M_1 and M_2. The constant voltage V_B is approximately equal to the sum of the threshold voltage of the transistors M_1 and M_2, $V_{T1} + V_{T2}$, and brings them to the edge of conduction. The transistors M_2 - M_3 and M_5 - M_6 form as a unity gain current mirror. The transistor M_7 and the current source I_2 are used to alleviate the channel-length modulation effect of the transistor M_3. During a positive input current $i_{in} > 0$, the current i_{in} flows through the transistor M_2 that causes the gate-source voltage of the transistor M_2 to increase and the gate-source voltage of the transistor M_1 to decrease effecting M_1 to cutoff. Similarly, the flow of a negative current $i_{in} < 0$ through the transistor M_1 causes the transistor M_2 to cutoff. Therefore the currents I_{D1} and I_{D2} can be given by

$$I_{D1} = i_{in} \quad \text{and} \quad I_{D2} = 0 \quad \text{for } i_{in} \le 0 \qquad (1a)$$

and

$$I_{D2} = i_{in} \quad \text{and} \quad I_{D1} = 0 \quad \text{for } i_{in} \ge 0 \qquad (1b)$$