High - Speed BiCMOS Comparator

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Abstract

This paper introduces the design of BiCMOS latched comparator circuit for high-speed system application, which can be used in data conversion, instrumentation, communication system etc. By exploiting the advantage technology of the combination of both the bipolar transistor and the CMOS transistor devices. The comparator circuit includes an input stage that combines MOS sampling with a bipolar regenerative amplifier. The resistive load of conventional current-steering comparator is replaced by a load, which is made by a NMOS transistor. The advantage of design and PSPICE simulation of BiCMOS latched comparator are the circuit will obtain wide bandwidth with lowest power consumption at a single supply voltage. All the characteristics of the proposed BiCMOS latched comparator circuit is carried out by simulation program.

I. Introduction

The increasing interest for high-speed, low-power, low-voltage analog-to-digital conversion can be explained by growth of the market of portable, [1] – [4] which requires a reduction of supply voltage and by the shift toward higher frequencies of the boundary between analog and digital signal processing.

The classical latched comparator,[1] in silicon bipolar technology has traditionally derminated the field of monolithic high-speed data conversion circuit. However, the emergence of BiCMOS as a viable mainstream VLSI technology offers new opportunities for improving the performance of such circuits by combining the complementary advantages of each technology. Relative to MOS devices, bipolar transistors exhibit superior threshold matching, higher transconductance and lower noise levels.

This paper present novel latched comparator designed and simulation in a BiCMOS technology.[5]-[7] It achieves power consumption of the comparator is only 650 μW at a single supply voltage of 3 V, 100 MHz clock with 50 MHz input signal. The load resistance of the classical comparators are replaced by NMOS transistors.

In Section III of this paper describes the BiCMOS comparator circuit. Simulation results are presented in section IV.

II. High-Speed Latched Comparators Circuit Description

In order to quick resolve differential voltage of few millivolts, circuits with positive feed back are commonly used, like the well-known latched comparator of Fig. 1. Its

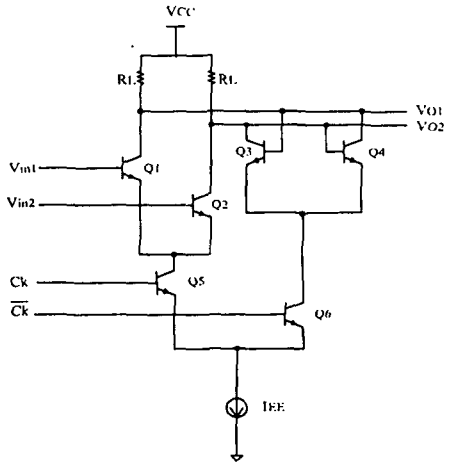

Fig. 1. Typical current-switching bipolar comparator.

performance can be improved by an input preamplifier. In order to highlight the limits of this architecture, the latched comparator circuit behavior must be considered both in the acquisition phase (ck = 1), when it behaves as differential amplifier, and in the regeneration phase (ck = 0), when it exploits positive feedback to reach valid digital levels within half a clock period with reference to previous work and the following five fundamental relationships can be easily obtained, which estimate the recovery time, bandwidth of the differential amplifier, the small-signal regeneration behavior, the low frequency output swing, and the maximum rate of charge at the outputs:

$$t_{rec} = R_L C_{total} \ln[1 + \frac{1}{\tanh(A_p V_{in} / 2V_{th})}] \quad (1)$$

$$V_O \approx V_{O1} - V_{O2} \approx A_L V_{in} \exp(t / \tau_{reg}) \quad (2)$$

with

$$\tau_{reg} = \frac{C_{Trg}}{g_m} (\frac{g_m R_L}{g_m R_L - 1}) \quad (3)$$

t = The falling and rising edge of the clock
V_{th} = The thermal voltage
V_{in} = $V_1 - V_2$
A_p = The voltage gain of the input preamplifier
C_{total} = The total capacitance affecting the acquisition phase.
R_L = The small-signal load resistance