2-bit Flash ADC Based on Current Mode Algorithmic

V. Tipsuwanporn *, S. Chuenarom **, S. Maitreechit ** ,W. Chuchotsakunleot* and V. Kongrat*

* Faculty of Engineering , King Mongkut's Institute of Technology Ladkrabang, Bangkok 10520, Thailand.

*(Tel: (66-2) 739-2406: Ext. 102, *E-mail: ktvittay@kmitl.ac.th)

**Faculty of Engineering ,South-East Asia University ,Bangkok 10160 Thailand.
**(Tel: (66-2) 807-4500: Ext. 331, **E-mail: Seri@sau.ac.th)

Abstract

This paper presents the 2-bit parallel algorithmic ADC using current mode for parallel method algorithm. It is operated by parallel conversion, 2-bit at each moment, and increase bit numbers by serial connection. The circuit operates in current mode. The comparison ratio can be controlled while working under mode operation. The circuit design used 0.8 μm CMOS technology which capable to convert 2-bit in 50 ns, power consumed 0.786 mW, with input current 0-50 mA from 3V single supply. From simulation testing, the conversion rate is much faster than other method.

1.Introduction

The analog design circuit was developed to work under current mode by using digital submicron CMOS technology [8], operating at low voltage, high speed, which used in CMOS ADCs. Such as two-step [1,7] pipelined [2] and algorithmic [3] under the high-speed requirement wish high resolution and less energy consumed. All the three principles are brought to put under consideration in order to achieve the required characterization for ADC. Since, each individual characteristic can not give the fully required property.

High speed analog to digital conversion by Flash and two-step Flash is quite popular but by Flash, can not increase the number of bit at the output. The number of comparison bit has to be 2^n-1, and n is the output bit. So it has to space the area and powers twice of the number of output bits. For Two-step Flash, it has slow speed because the DAC circuit has to be the main operating circuit. The total time operation has to be included both conversion time and operation time of DAC. In algorithmic method, the DAC in deleted, resulted in high speed and size reduction. In this paper the presentation emphasises on the increase of speed of 2 times based on algorithmic [3] by convert 2-bit at each moment.

2.Principle operation

The algorithmic analogue-to-digital conversion technique[9] has been known for many years as a conversion method that can take advantage of relative simple hardware to produce ADCs. A 2-bit parallel algorithmic conversion is performed as shown in Fig .1.

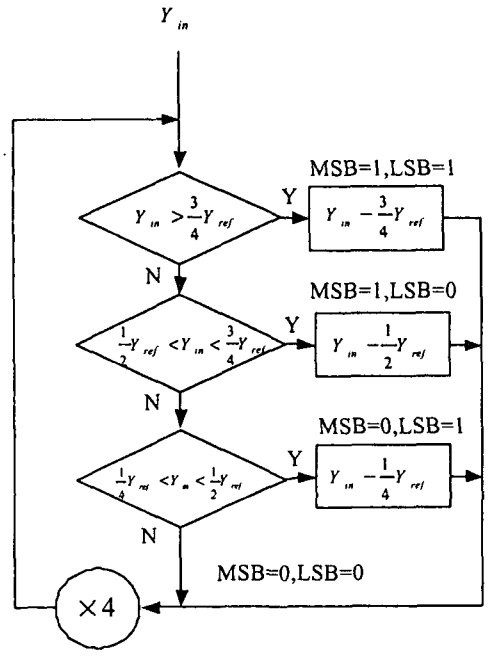

Fig. 1. Flow chart of 2-bit Parallel Algorithmic.

The input signal, Y_{in} which can take on any value between zero and the reference, Y_{ref}, is compared with the tripled reference (Y_{ref} is reference input). A condition of comparison is shown in the flowchart Fig.1. The new Y_{in} value multiplied by four to create $4Y_{in}$.can then to be fed back to the input or the following identical cell which will perform exactly the same function and generate another bit