CMOS Switch-Current Square Base on Switch Current

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Abstract

Current signal square based on switch current is presented in this article. This is the new technique that can design current signal square circuit by using switch-current memory cell, current square and sample and hold technique, which have been presented by the general switch-current. This principle which is present have the good electrical characteristics such as the low input impedance, high output impedance and high frequency response. The system can also operate in the audio frequency range to the high frequency current signal. The system application of this technique can be apply to the current signal multiplier by quarter square technique. The experimental results agree well with the theory as high accuracy and linearity.

1. Introduction

The current squarer is one of the most important circuit building blocks of the analog signal processing in the VLSI design. This circuit can be applying to the circuit that uses the square current function such as the current multiplier circuit. In this present article, the block diagram of the multiple output current square bases on switch current memory cell is shown in Fig.1.

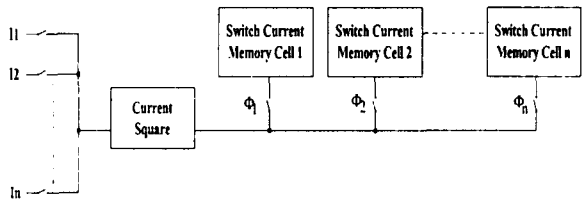

Fig 1. The circuit block diagram of the n-state current square

A switched-current [1] is a new analogue sample data processing technique and more attention. Unlike switched-capacitor circuits that require additional processing steps to fabrication precision linear capacitor. Switched-current has a number of important advantages: they are exclusively composed of MOS transistors, switches and current sources instead of operational amplifiers, and precise linear floating capacitor, making them suitable for implementation in standard CMOS processes. As capacitors in switch-current technique are only use for holding voltage, switched-current has no problems with capacitor mismatch. Furthermore, switched-current is well suited for low-voltage application and high speed operating requirement.

2. Circuit description

The MOS Memory cell

Current memory cell [1] can be formed by basic current mirror as show in Fig 1.

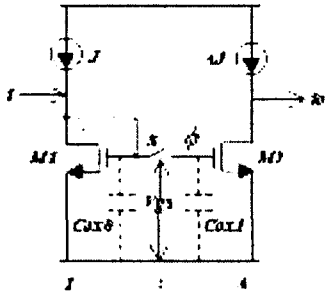

Fig 2 Switch Current Memory Cell

The circuit in Fig 1 [3] – [5] is simply memory cell formed by basic current mirror with a switch S separating its input (M_1) and output (M_2) transistor. A switched S can be control by clock phase ϕ the switch turn on when their control voltage is high. The memory cell has two modes of operations the track operation and hold operation. In the track operation the switched S is close. It is base on the current store, ideally shorting together the gate of M_1 and M_2 both oxide capacitance, C_{ox0} and C_{ox1} are to V_{gs} where

$$V_{gs} = \sqrt{\frac{2(J+i)}{k'\left(\frac{W}{L}\right)}} + V_t \qquad (1)$$

By normal current mirror [6] – [7] action $i_o = -i$ and i_o is available simultaneously with the input sample. Therefore, the output current tracks the input current. In the hold operation the switch is opened and isolates the input from the output. A voltage close to V_{gs} held on C_{ox1} the transistors gate capacitance of M_2 stores the charge