Overview of control and data processing schemes of FIMS

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The overview of control and data processing schemes of FIMS (Far-ultraviolet Imaging Spectrograph) is described in detail for developing the electrical test bed (ETB). Electrical and data interfaces are designed to meet the specifications between the spacecraft, which includes the Node Controller 4, Mass Memory System, and GPS, and FIMS. The microprocessor, DSP32C, satisfies the requirements of detector and housekeeping electronics: the MIPS analysis proves that the maximum photon input rate, which is presumed of 2800 photons per seconds, can be acquired by DSP32C and be transferred to MMS. To provide the precise time information, the time synchronization with GPS is implemented in the design. We use FPGA chip to optimize the size, mass, and power of the circuit. The initial test of ETB has been performed and verified at this moment. In according to the development schedule of KAISTSAT-4, we are preparing for the integration test with other systems.