영상의 깜박거림 현상을 최소화하기 위한 순환 루프 필터의 설계

문 오학, 이 봉근, 이 호남, 이 영호, 강 봉순, 홍 창희
동아대학교 공과대학 전기전자컴퓨터공학부

Design of IIR Loop Filter to minimize A flick Phenomenon of An image

O. Moon, B. Lee, H. Lee, Y. Lee, B. Kang, and C. Hong
School of Electrical, Electronic, and Computer Eng, Dong-A University, Busan, Korea
Email: moh9@didec.donga.ac.kr

Abstract

In this paper, we propose a method, an optimized architecture of a device with an image signal process of a field unit to minimize the flick phenomenon that happens in direction of a color temperature at a color tone change. The proposed IIR loop filter has an optimized architecture and reduced hardware compared with previous filters. In order to achieve the optimization for the hardware complexity, It is designed by time-multiplexing architecture. The proposed IIR loop filter is synthesized by using the STD90 0.35um cell library.

I. INTRODUCTION

Digital filters are being increasingly used in many diverse areas, such as signal processing, image processing, communication system as they offer a number of attractive advantages in regard of stability, accuracy, reliability, and flexibility in comparison with the more conventional analog filters[1].

In this research, we propose the IIR loop filter as a device with an image signal process of a field unit to minimize the flick phenomenon that happens in direction of a color temperature as an image signal processing application.

For example, It is used to resolve the problem that occurs in changing a color tone of an image. If a linear phase FIR filter is designed for objective to minimize a flicker that happens at a color tone change, it may require bulky hardware that is expensive to build. Thereby, we designed an optimized IIR loop filter to have a low hardware complexity in consideration of a hardware embodiment while achieving the same requirement of a magnitude response and an effect to resolve this problem[2].

II. METHODS

The proposed IIR loop filter has stable and causal characteristic as 1st order system with 16 filter coefficients. Fig. 1 shows the procedure of the proposed IIR loop filter. The role of the filter is similar to a low-pass filter for gain, while the phase response obtains a nonlinear characteristic.

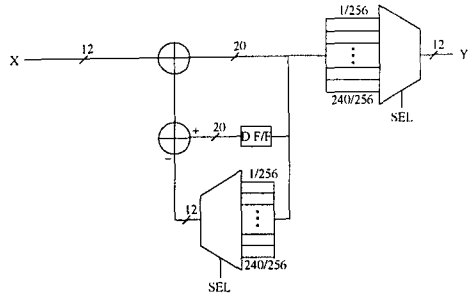

Fig. 1 The proposed IIR loop filter

The characteristics of the filter are shown in Fig. 2, Fig. 3. Fig. 2 shows the frequency responses of the loop filter.

The proposed filter is 1st system and nonlinear phase responses. The frequency responses appear in radical maximum when the poles draw near 0 point of a unit circle[3]. The 3-dB point has various frequencies in depending on the proposed loop filter coefficient. Fig. 3 shows the corresponding step responses. The limit values of step responses converge into 1.

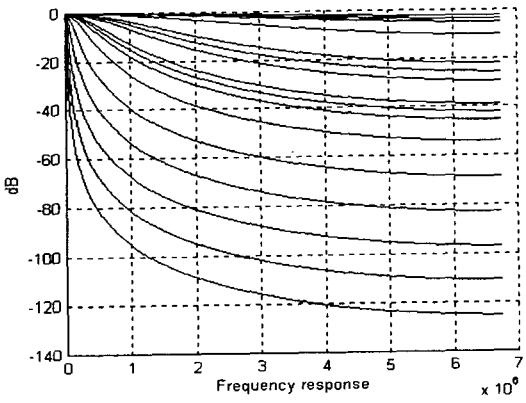

Fig. 2 Frequency responses of the proposed IIR loop filter

When one design IIR loop filters, parallel architecture is generally designed. Filters that have multi-input really exist as many as the number of input but the proposed research was designed as the time-multiplexing structure for optimized hardware complexity. It is shown in Fig. 4.

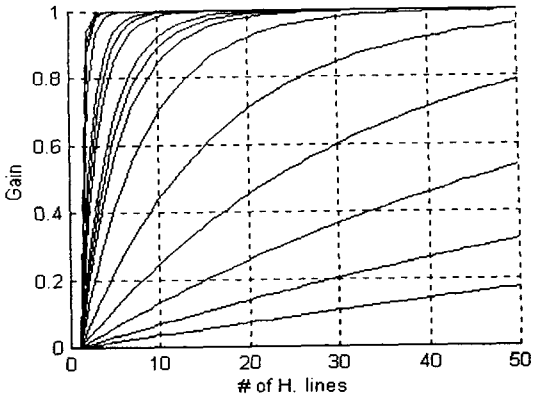

Fig. 3 Step responses of the proposed IIR loop filter

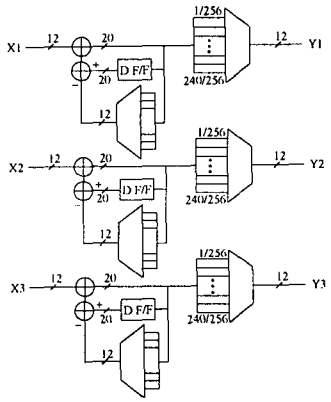

Fig. 4 Block diagram of a general parallel architecture

To optimize a hardware complexity, paper in this research proposes the time-multiplexing architecture instead of the parallel architecture. We designed two types time-multiplexing architecture. In the first, latch type was designed to reduce a hardware size in comparison with a flip-flop type scheme. But the latch type reduces a hardware size: it makes a system unstable. Therefore, in second flip-flop type design is proposed though a hardware size is increased in a few sizes.

Fig. 5 and Fig. 6 show the proposed architecture of the two types of IIR loop filter. Those consist of the following four parts: (i) input port, (ii) operation part, (iii) register area, and (iv) output

port. The input port is comprised in a counter and a multiplexer. Each input are controlled by counter. The output of each input has two clock delays. The operation part is compose of adders, a subtracter, and shifts instead of multipliers. The register area of latch type contains a demultiplexer, three registers, a clear, and a multiplexer, but flip-flop type consists of three flip-flops instead of a clear and three register. The output port was demultiplexed in accordance with two-clock delays signal. Despite both types are different, There are all the same in respect to the total delay.

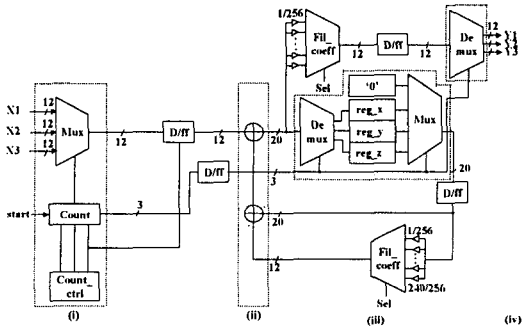

Fig. 5 Time-multiplexing architecture of the latch type

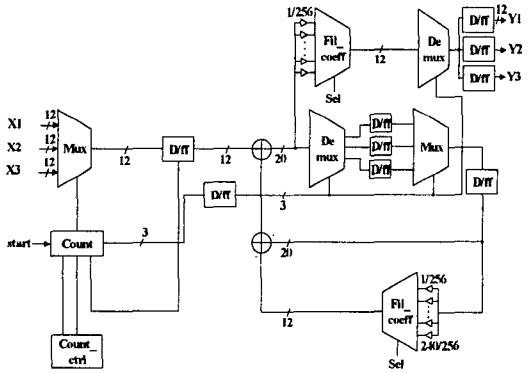

Fig. 6 Time-multiplexing architecture of the flip-flop type

III. RESULTS

The proposed IIR loop filter is modeled by using VHDL and the models are verified by using the Synopsys simulator. After the verifications are done, the models are synthesized into gate by using the STD90 0.35um cell library. The proposed IIR filter is synthesized in gates and results are, then, listed in Table I.

	12Bits(Input)	
	Gate Count	Time Delay
Single architecture	2,273	28.77ns
Parallel(3 Input)	6,823	29.68ns
Time-multiplexing (Latch)	3,146	27.84ns
Time-multiplexing (F/F)	3,525	28.51ns

Table I. Comparison of hardware complexity and delay

The first column lists a gate count of 12bits input. As one can see, the time-multiplexing latch architecture with 12bits input reduces the gate count of the proposed IIR loop filter from 6,823 to 3,146 that is 53.89% reduction in the hardware complexity. Although the above architecture reduces the hardware complexity, this architecture can cause an unstable system. Thereby, we propose the time-multiplexing flip-flop architecture because it makes a system stable though the hardware complexity is increased about 12.05% in condition of 12bits input.

Fig. 7 shows a synthesized circuit of the proposed IIR loop filter using Synopsys tool.

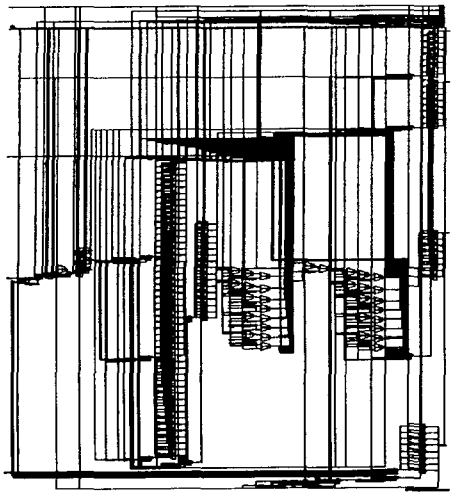

Fig. 7 A synthesized circuit of proposed IIR loop filter

IV. CONCLUSIONS

The proposed IIR loop filter really showed that it was powerful to minimize the flick phenomenon that happens in direction of a color temperature in application changing a color tone. Besides, the proposed IIR loop filter reduced the hardware complexity by using the time-multiplexing architecture. The proposed IIR loop filter was synthesized into gate by using the STD90 0.35um cell library, resulting in the gate count of 3,525 at 12bits input.

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REFERENCES

[1] 八木伸行, 井上誠喜, 合志清一, and 林正樹, The Digital Image Processing in according to C Language, Ohmsha · Seong An Dang, 1998.

[2] Michael Robin and Michael Poulin, Digital Television Fundamentals, McGraw-Hill, Inc., 1997.

[3] Higgins, Richard J., DIGITAL SIGNAL PROCESSING IN VLSI, Prentice-hall, Inc., 1990.