Effect of the size of active device and heatsink of power MOSFETs on its the junction to ambient transient thermal behavior

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ABSTRACT

To investigate the compact effects of the different area of an active layer and the different type of heatsink on the junction to ambient transient thermal impedance, we have characterized the thermal behavior of power MOSFETs that have three different areas of an active layer and two types of heatsink. To do so, the "cooling curve method" has been used in order to measure the junction-to-ambient transient thermal impedance Z_{thja} that represents the thermal behavior of the devices. The measured data depicts that the larger area of an active layer gives the better - in other words, smaller - thermal impedance, and that the larger size of a heatsink improves the thermal impedance.

INTRODUCTION

The most important parameter for keeping a power MOSFET within its safe operating area is probably its silicon temperature, often referred to as "junction temperature (Tj)". The aging of a device is proportional to the fourth power of the temperature deviation. The ON-resistance R_{on} of a MOSFET and thus the conduction losses are roughly doubled when a temperature increase from 25℃ to 150℃[1]. In order to limit these effect, a maximum junction temperature must be specified for all semiconductor devices which, when exceeded, can lead to destruction or permanent damage of the devices.

The junction-to-ambient transient thermal impedance Z_{thja} of system - they consist of silicon chips, packages and heat sinks - has been popularly used to do so, since this gives the temperature between junction to ambient. It depends largely on the area of an active layer and the type of heatsink [2]. To investigate of the compact effects of these factors on it, we have described the transient thermal behavior of DMOSFETs, which have different active devices and heatsinks, using the junction-to-ambient thermal impedance Z_{thja}.

MEASUREMENT

The "cooling curve method" has been used in order to measure the transient thermal response [4]. The cooling curve is the thermal response to a switch-off performance and differs from the process of the heating curve only by the sign and the temperature offset due to the steady-state thermal resistance.

The usual procedure, in practice, is to first heat the devices with defined power dissipation P_0 until it assumes a stationary temperature T_0. If one knows the exact temperature dependence of a parameter of the chip, the forward voltage drop of an integrated diode structure is used the cooling curve Tj(t) of the affected region of the chip can be determined after reducing the power dissipation to zero. This gives one the transient thermal impedance Z_{th} (t) as [3][4]

$$Z_{th} = \frac{T_{j1} - T_j(t)}{P_D} \quad (1)$$

This single pulse transient thermal impedance corresponds in system theory to the step response (turn-on) and therefore contains the full thermal description of the system.

In order to measure the temperature of MOSFETs at the active layer; the body diode is commonly used. This diode results from the technological structure of MOSFET transistors, as shown in the following figure.

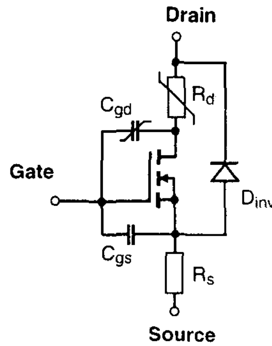

Figure 1 Circuit diagram of a DMOS model

The following equation gives the temperature dependence of the voltage of a p-n junction diode with constant current *I*.

$$V = \frac{kT_0}{q}\left(\frac{T}{T_0}\right)\cdot\left[\ln\left(\frac{I}{I_{S0}}\right) - \frac{E_{g0}}{kT_0} - 3\ln\left(\frac{T}{T_0}\right)\right] + \frac{E_{g0}}{q} \quad (2)$$

In order to link the voltage drop at the inverse diode to the junction temperature, more than two points of measured temperature are advisable. The temperature / voltage relationship does not show a perfect linearity due to the temperature dependent logarithm term in Eq. (2). It is more accurate to take up several temperature calibration points for getting the appropriate straight line. To do so, the transistor is put into a furnace. When the furnace ambient temperature is obtained after approx. 30-min, the voltage drop V_{SD1} as well as the temperature T_1 of the furnace with the current can be determined. Subsequently, the procedure is repeated for a second measurement, when the couple (V_{SD2}, T_2) is obtained. These points give a straight line as

$$T_J(t) = \left(\frac{T_{J1} - T_{J2}}{V_{SD1} - V_{SD2}}\right)\cdot V(t) + \left(\frac{V_{SD1}\cdot T_{J2} - V_{SD2}\cdot T_{J1}}{V_{SD1} - V_{SD2}}\right) \quad (3)$$

$$K = \frac{T_{J1} - T_{J2}}{V_{SD1} - V_{SD2}} \quad (4)$$

If more than two measurement are performed, the slope and the intercept of Eq. (3) can be found by means of linear regression. This procedure is called "K-factor calibration" because the gradient of Eq. (3), i.e. Eq (4) is the so-called "K-factor" [3][4]. A K-factor calibration set-up which measures V_{SD} for a specified value of I_m in an environment in which temperature is both controlled and measured is shown as Figure 2.

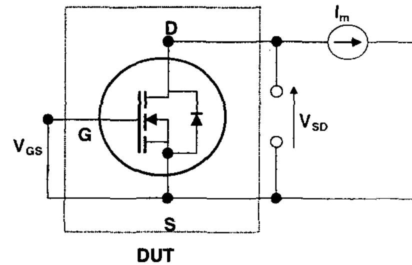

Figure 2 Circuit diagram for measurement

In Figure 2, the magnitude of I_m shall be chosen so that V_{SD} is a linearly decreasing function over the expected range of T_j during the power pulse. I_m must be large enough to ensure that the source-drain junction is turned on, but not so large as to cause any significant self-heating. I_m will normally be 10mA for small power devices and 100mA for large ones.

The following figure shows the connection diagram of the used measurement set-up. Here, the gate and drain are shorted [4].

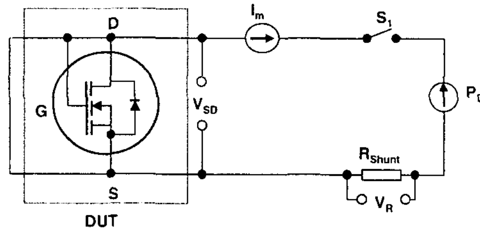

Figure 3 K-factor calibration measurement setup

RESULT & DISCUSSION

To investigate the compact effects of the area of an active layer and the type of heatsink on the junction to ambient transient thermal impedance, we have characterized the thermal behavior of DMOSFETs, which have three different areas of an active layer and two types of heatsink. Table 1 and Figure 1 show these and, in accordance with the labels used by Infineon Technologies AG, MOSFETs are addressed BSO304SN, BSO302SN and BSO615NV.

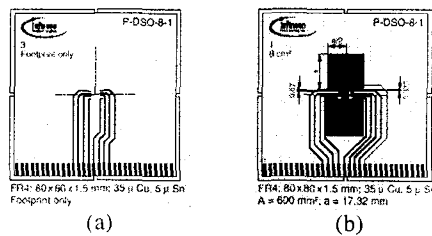

Figure 4. Footprint for SO-8 device (a) the minimal footprint (b) 600mm² footprint

Type	BSO304SN	BSO302SN	BSO615NV
Area of an active layer	4.03 mm²	6.24 mm²	9.60 mm²

Table 1. Measured MOSFETs and their active areas

The measured MOSFETs are based on the DMOS (Double diffused MOS) technologies and housed in SO (Small Outline) packages using SMD (Surface Mounted Device) technologies by Infineon Technologies AG, Munich, Germany.

In Figure 4, the forward voltage drop across the sensing diode biased at a constant current of 10mA varies linearly with the temperature with a coefficient of 2.07mV/K for the BSO302SN, 2.10mV/K for the BSO304SN and 2.10mV/K.

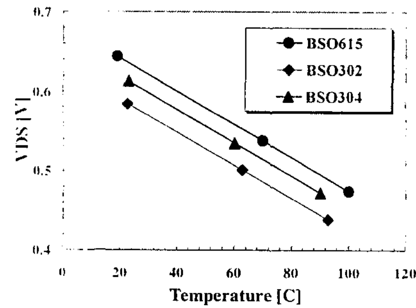

Figure 4 K-factor calibration of characterized devices

Figure 5 to Figure 7 show the measured V_{SD} vs. time of the BSO302SN, the BSO304SN and the BSO615NV for the cases of a junction-to-solder and a junction-to-ambient measurement.

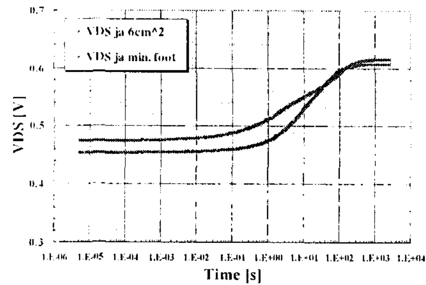

Figure 5 V_{SD} of the BSO302SN vs. time

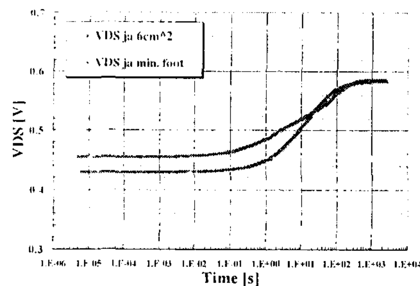

Figure 6 V_{SD} of the BSO302SN vs. time

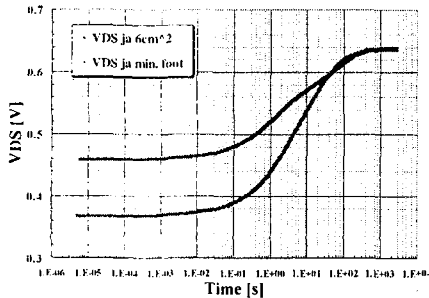

Figure 7 V_{SD} of the BSO615VN vs. time

By using Eq. (3) and Eq. (1), the transient thermal impedance of the devices with 600mm^2 heatsink is shown in Figure 8. and that of the devices with minimal footprint shown in Figure 9. Here, dissipated power was 1.02 W for the BSO615NV, 2.01 W for the BSO302SN and 2 W for the BSO304SN.

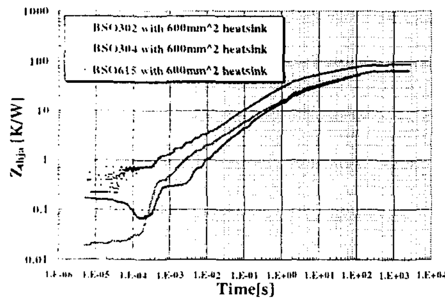

Figure 8 Z_{thja} of devices with 600mm^2 heatsink

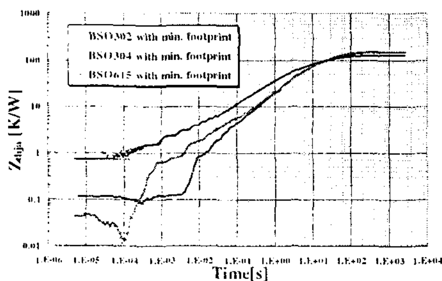

Figure 9 Z_{thja} of devices with 600mm^2 heatsink

As can be seen, the accuracy of the data is limited up to the time of about half ms while the results from the time of about half ms up to thermal equilibrium of each curve are better. Up to the time of about 0.01 ms data represents the thermal behavior of the silicon. A plateau occurs up to about 1 ms, due to the copper slug. Above about 1000 ms the steady state occurs which means the junction temperature goes up to the ambient one. The value of Z_{thja} is defined as the junction-to-ambient thermal resistance R_{thja}, when steady state occurs. This is a measure how fast the systems sink heat from inner to outer, i.e. ambient. Figure 8 and 9 depict that the larger area of an active layer gives the "better" - in other words, smaller - thermal impedance, and that the larger size of a heatsink improves the thermal impedance.

Circuit and device designer must consider these results to keep a power device within its safe operating area. If the thermal network could be generated from the transient thermal impedance, the "dynamic" operating states of a Power MOSFET, in which a relevant inherent heating occurs, can be simulated with a circuit simulation tool, e.g. PSpice® or SABER ®, etc.

ACKNOWLEDGEMENT

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