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Simulated Annealing Approach to Evaluation of Maximum Number of Simultaneous Switching Gates

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Abstract

This paper presents a new approach to evaluate the maximum number of simultaneous switching gates of a given combinational circuit. The new approach is based on an iterative method proposed by Sinogi et al. and applies a simulated annealing strategy to search for a new solution. The experimental evaluation using ISCAS'85 benchmark circuits shows that the proposed approach has attained an excellent improvement compared with other related methods including the iterative method.

1 Introduction

The increasing use of portable computing and communication systems makes the minimization of power dissipation one of the main concerns in the circuit and system design. Hence, it is strongly needed to accurately estimate power dissipation for power reduction in VLSI design. For a CMOS circuit, the dominant source of power dissipation is dynamic transition current, and other sources are much smaller and can be neglected. Therefore the maximum number of switching gates may be used to evaluate the maximum power dissipation for enhancing the worst-case reliability of combinational circuits[1, 2].

Many approaches have been proposed for evaluating the maximum number of simultaneous switching gates. Ghosh et al.[1] proposed a symbolic simulation method. However it is only applied to small circuits. Ueda and Kinoshita proposed three methods: the partial exhaustive enumeration method, branch and bound method[2] and the genetic algorithm[3]. Among them, the partial exhaustive method is simple and gives a good solution, but unfortunately it needs too much computation time.

Next, Shinogi et al. proposed an iterative improvement method[4, 5], in which input vector pair is successively updated to increase the number of switching gates. Then, we tried to solve the difficulties in [4] by introducing circuit partition based on cone structure[6]. But the improvement attained is not sufficiently large.

In this paper, we present a new approach to improve the final solution, which applies a simulated annealing strategy to search for a new solution during iterative improvement. By using the probability $exp(-\delta C/T(t))$ with the current temperature $T(t)$, we can improve the solution iteratively until the freezing temperature.

2 Preliminaries

Consider an example circuit C_1 shown in Figure 1. Suppose that input vectors $(0,1,0,0,0)$, $(1,1,1,0,0)$ are given to the primary inputs:I_1, I_2, I_3, I_4, I_5 at two distinct times consecutively. Then the output values of three gates G_1, G_3, G_4 change from 0 to 1. On the other hand, the output value of G_2 remains unchanged. In this case, we call three gates G_1, G_3, G_4 simultaneous switching gates. We say the number of simultaneous switching gates, denoted by $N(C_1, V_1)$, is three for the circuit C_1 and the input vector pair $V_1 = ((0,1,0,0,0),(1,1,1,0,0))$.

It is clear that by taking another input vector pair $V_2 = ((0,1,0,1,0),(1,1,1,1,1))$ as shown in Figure 2, the value of $N(C_1, V_2)$ becomes four. Then, the maximum number of simultaneous switching gates, denoted by $N_{max}(C)$, for a given circuit C is defined by $N_{max}(C) = max(N(C, V_i))$ where all input vector pair $V_i's$ are considered and the maximum value is chosen for all of $N(C, V_i)'s$. For Figure 2, $N_{max}(C_1) = 4$.

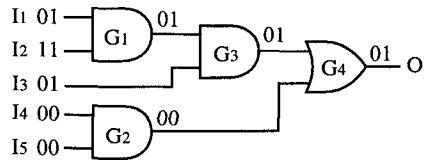

Figure 1: Circuit C_1 and input vector pair V_1

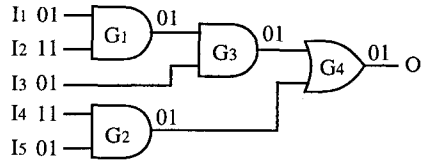

Figure 2: Circuit C_1 and input vector pair V_2

3 Simulated Annealing Approach

For combinatorial optimization problems, new heuristic approaches based on simulated annealing (shortly, SA) have been extensively applied. The simulated annealing is originally devised for the study of the behavior of complex systems consisting of a large number of interacting atoms in thermal equilibriam at a finite temperature. The analogy between a combinatorial optimization problem and the problem of determining the lowest-energy ground state of a physical system was first observed by [7].

The following shows an outline of simulated annealing approach to solve combinatorial optimization problems.

Step 1: (Initialization): Generate initial solution and set initial temperature.

Step 2: (Calculating solutions): Calculate a set of possible solutions.

Step 3: (Selecting a solution by SA): Select a new solution from the set by SA.

Step 4: (Updating temperature): Lower the temperature according to a scheduling.

Step 5: (Termination): If temperature becomes less than or equal to the freezing temperature, then terminate the procedure.

4 Heuristic Method

In this paper we devise a new method, which is defined by replacing the selecting strategy for a new input vector pair in the iterative improvement method[4] by the simulated annealing(SA) strategy. By adopting the simulated annealing strategy, we can expect a greater possibility of leaving the local optimal solution and then we may reach a better final solution.

The following shows an outline of the new method which evaluates the $N_{max}(C)$ for a given combinational circuit C. In the description, we use $T(t)$ to denote a temperature at time t, and R_{max} to denote the total number of initial vector pairs(that is, the total repetition times of the method).

Step 1: (Initialization): Set initial temperature $T(0)$ to an appropriate value. Generate initial vector pair V_0 randomly and compute $N(C, V_0)$. Assume that $t = 0$ and $j = 0$.

Step 2: (Calculating solutions) :

Substep 2.1: (Selecting an input pin): Select randomly a primary input pin i.

Substep 2.2: (Calculating all possible solutions): Generate all possible vector pairs V_α, V_β, V_γ with respect to the selected pin i and V_j. Then evaluate the maximum numbers $N(C, V_\alpha)$, $N(C, V_\beta)$, $N(C, V_\gamma)$.

Substep 2.3: (Selecting a candidate solution): Select a new vector pair V such that $N(C, V) = max(N(C, V_\alpha), N(C, V_\beta), N(C, V_\gamma))$.

Step 3: (Selecting a solution by SA): A new solution V_{j+1} is obtained by the following

$$V_{j+1} = \begin{cases} V & if \ N(C,V) > N(C,V_j) \\ V_j & \text{otherwise} \end{cases}$$

However, in the case of $N(C, V) \leq N(C, V_j)$, we select V instead of V_j with probability $exp(-\delta C/T(t))$ where $\delta C = N(C, V_j) - N(C, V) + 1$.

Step 4: (Updating temperature): Repeat Substep 2.2 to Step 3 n times in which i is changed to $i = i(mod\ n) + 1$ each time. Then update $T(t + 1) = \alpha T(t)$ and $t = t + 1$. Here α is a lowering rate of temperature and $0 < \alpha < 1$, and n is the number of primary input terminals.

Step 5: (Termination):

Substep 5.1: (Decision on stopping criterion): Go to Substep 2.1 as far as $T(t)$ is greater than the freezing temperature T_c. Otherwise, terminate the calculations.

Substep 5.2: (Output the best solution): Repeat Step 1 to Substep 5.1 R_{max} times, and output best solution $N_{max}(C)$.

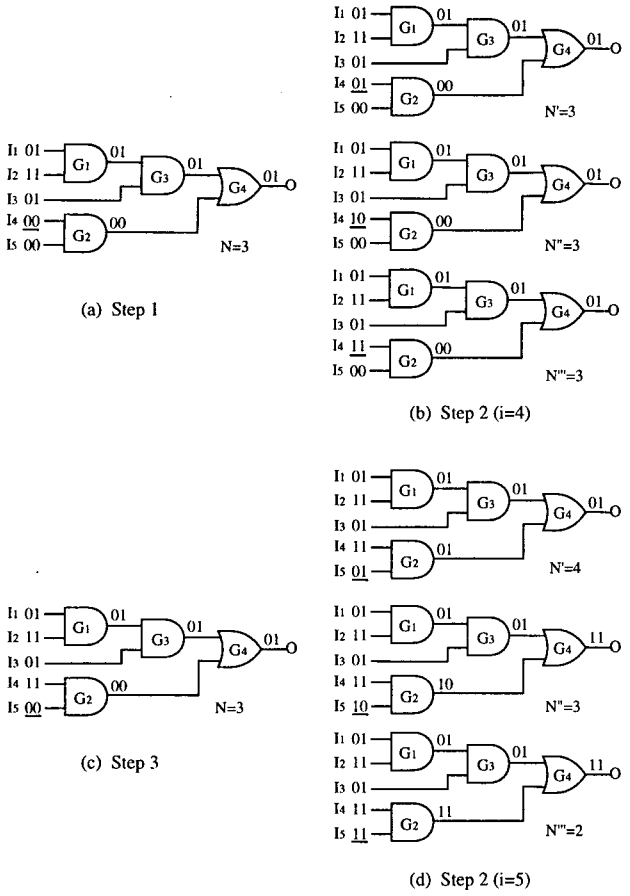

Figure 3: Explanation of proposed method

5 Example

Consider a circuit C_1 shown in Figure 3(which is the same circuit shown in Figure 1 and 2). We explain an application of the proposed method based on SA described in Section 4 to the circuit. We assume that $\alpha = 0.9$ and n=5.

As Step1, we set time t=0 and an initial temperature T(0)=10. We choose randomly an initial input vector pair $V_0 = ((0,1,0,0,0),(1,1,1,0,0))$. Then we get $N(C_1, V_0) = 3$.

Then, at Substep 2.1 we choose a primary input pin $i = 4$ randomly. At Substep 2.2, for three distinct vector pair V_α, V_β, V_γ(which are generated by assigning distinct values to fourth input pin), we get $N(C_1, V_\alpha) = (C_1, V_\beta) = N(C_1, V_\gamma) = 3$, as shown in Figure 3(b). Therefore, we select vector pair $V = V_\gamma = ((0,1,0,1,0),(1,1,1,1,0))$ as a candidate solution.

Next at Step 3 we choose one out of two vector pairs V_0 and V. In this case, since $\delta C = 3-3+1 = 1$, and T(0)=10, at the probability $exp(-1/10) = 0.9$ we select V as the new solution V_1. Hence we assume that V_1 is selected as the next solution instead of V_0.

Then we increment i and execute Substep 2.2 again. At Substep 2.2 we get a primary input pin $i = 5$. As shown in Figure 3(d), we get $N(C_1, V_\alpha) = 4$, $N(C_1, V_\beta) = 3$, $N(C_1, V_\gamma) = 2$. As the result of Substep 2.2, we select a new vector pair $V = V_\alpha = ((0,1,0,1,0),(1,1,1,1,1))$ as a candidate solution. Next, at Step 3 we choose one out of two vector pairs V_1 and V. In this case, since $N(C,V) > N(C,V_1)$, we select V as the new solution V_2.

These processes are summarized in Table 1. Table 1 shows values of parameters i, t, temperature T(t), and the resultant solution $N(C_1, V)$ with the content of V.

Table 1: Snapshots of evaluation

Parameters		Temperature	Maximum number	
i	t	T	$N(C_1,V)$	Vector pair
—	0	10	3	((0,1,0,0,0),(1,1,1,0,0))
4	0	10	3	((0,1,0,1,0),(1,1,1,1,0))
5	0	10	4	((0,1,0,1,0),(1,1,1,1,1))
1	0	10	3	((1,1,0,1,0),(0,1,1,1,1))
2	0	10	2	((1,1,0,1,0),(0,0,1,1,1))
3	0	10	3	((1,1,1,1,0),(0,0,1,1,1))
2	1	9	3	((1,1,1,1,0),(0,1,1,1,1))
3	1	9	3	((1,1,0,1,0),(0,1,1,1,1))
4	1	9	3	((1,1,0,0,0),(0,1,1,1,1))
5	1	9	3	((1,1,0,0,1),(0,1,1,1,1))
1	1	9	4	((0,1,0,0,1),(1,1,1,1,1))
5	2	8.1	4	((0,1,0,0,0),(1,1,1,1,1))
1	2	8.1	3	((1,1,0,0,0),(0,1,1,1,1))
2	2	8.1	3	((1,1,0,0,0),(0,0,1,1,1))
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6 Experimental Evaluation

We have conducted simulation studies of the proposed method using $ISCAS'85$ benchmark circuits[8] on Sun Ultra 60 Workstation(360MHz, 512Mbytes). Table 2 summarizes the values of N_{max} obtained by the proposed method and that referred from the relevant papers[2, 3, 4].

In the experiment, we set the number of initial vector pairs(that is, $R_{max} = 100$), $T(0) = 10$, $\alpha = 0.95$, $T_c = 0.1$ for the proposed method. In Table 2, Proposed SA represents the best solution obtained by the proposed method and average computation time. Iterative IMP[4] represents the best result obtained by three distinct algorithms in [4] under $R_{max} \leq 600$. Similarly Partial Ex.[2] represents the best result obtained by two algorithms in [2]. From Table 2, we can see that the proposed method gets the excellent

Table 2: Application to *ISCAS'85* benchmark

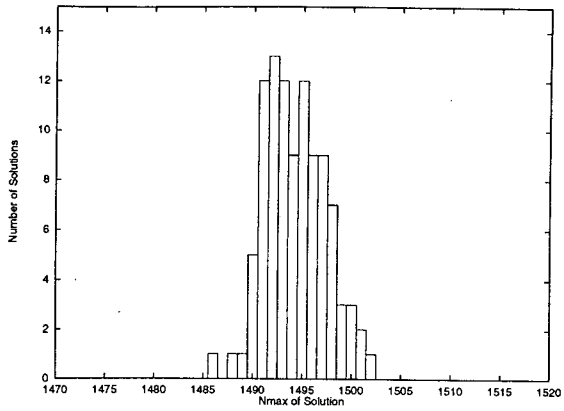
Circuit Name	Proposed SA (Rmax=100)	IMP[4]	GA[3]	Partial Ex.[2]
C880	319 (209sec)	319	318	315
C1355	308 (277sec)	295	296	305
C1908	604 (312sec)	604	588	592
C2670	823(2048sec)	813	791	806
C3540	931 (856sec)	923	919	915
C5315	1502(2948sec)	1479	1449	1434
C6288	1581(1008sec)	1564	1539	1556
C7552	2226(5278sec)	2180	2100	2133

solutions for all circuits in *ISCAS'85*.

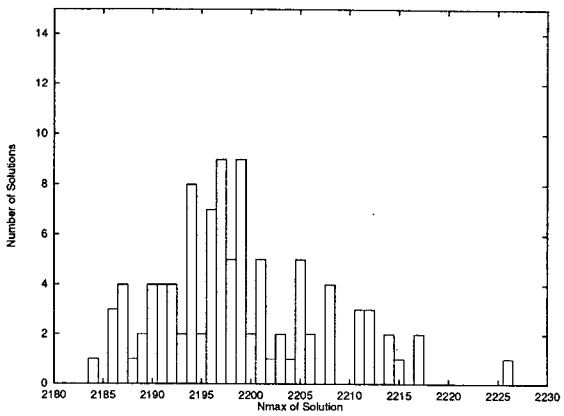
The proposed method is repeated a hundred times. Then Figure 4 shows the distribution of all these solutions. From Figure 4 we can expect that the proposed method may return good solution even if restrictive conditions are put on the execution time.

7 Conclusion

We proposed a new approach to evaluate the maximum number of simultaneous switching gates of a given combinational circuit. The new approach is based on a simulated annealing strategy to search for a new solution. The experimental evaluation using ISCAS'85 benchmark circuits shows that the proposed approach has attained an excellent improvement compared with other related methods.



(a) c5315



(b) c7552

Figure 4: Distribution of solutions

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