A Neuro-Fuzzy Based Circular Pattern Recognition Circuit Using Current-Mode Techniques

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Abstract

A neuro-fuzzy based circuit to recognize circular patterns is proposed in this paper. The simple algorithm and exemption from the use of template patterns as well as multipliers enable the proposed circuit to implement on the hardware of an economical scale. Furthermore, thanks to the circuit design by using current-mode techniques, the proposed circuit can achieve easy extendability of the circuit and efficient pattern recognition with high-speed. The validity of the proposed algorithm and the circuit design is confirmed by computer simulations. The proposed pattern recognition circuit is integrable by a standard CMOS technology.

1 Introduction

Recently, necessity for intelligent support systems is increasing in the field of the primary industry because of the decrease in the working population. For example, the intelligent support systems to harvest fruits instead of human being are required in the field of agriculture. To harvest fruits by using intelligent support systems, the design of the pattern recognition system which is a building block of the support system to calculate the coordinates of the target objects is important. For this reason, several methods have already been proposed for the realization of the pattern recognition systems [1],[2]. Among others, template matching is the most famous method in the pattern recognition problem. The disadvantages of this method are requirement of large number of the template patterns and large computational time which depends on the size of the input image. Furthermore, most of the pattern recognition systems using template matching are realized by using software systems on digital computers or voltage-mode circuit designed by using HDL since the algorithm of the template matching is very complex. Therefore, they require a higher speed microprocessor and larger capacity memories. To realize the real-time processing and the economical hardware scale for the pattern recognition systems, the simple algorithm and architecture are required.

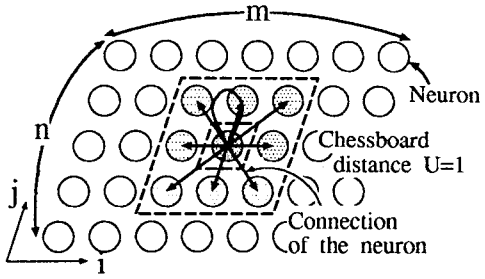


Fig.1 Architecture of the proposed circuit.

In this paper, a neuro-fuzzy based circuit to recognize circular patterns such as water melon, orange, etc. is proposed. The simple algorithm and exemption from the use of template patterns as well as multipliers enable the proposed circuit to implement on the hardware of an economical scale. Furthermore, thanks to the circuit design by using current-mode techniques, the proposed circuit can achieve easy extendability of the circuit and efficient pattern recognition with high-speed. The validity of the proposed algorithm and the circuit design is confirmed by computer simulations. Concerning 8×8-pixel binary images, the performance of the proposed circuit is analyzed by SPICE simulations.

2 Architecture

Figure 1 shows the architecture of the proposed pattern recognition circuit. In Fig.1, (i, j) denotes the coordinates of the neurons. As an input of the proposed circuit, the $m \times n$-pixel binary image is given. The pixels of the input image correspond to the coordinates of the neurons. Figure 2 shows the block diagram of the neuron for the proposed circuit. In Fig.2, the output function of the neuron is a unit-step function. The threshold value of the unit-step function is denoted by TH. In Fig.2, the neuron $f(i, j)$ is connected to the neurons which are located within a chessboard distance U (see Fig.1). The parameter U is set equal to the radius of the circular pattern. The proposed circuit is in

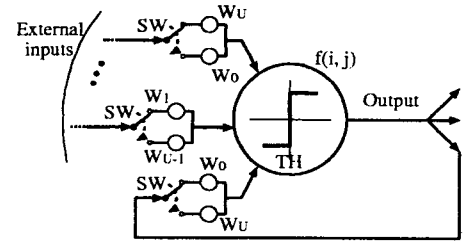


Fig.2 Block diagram of the neuron.

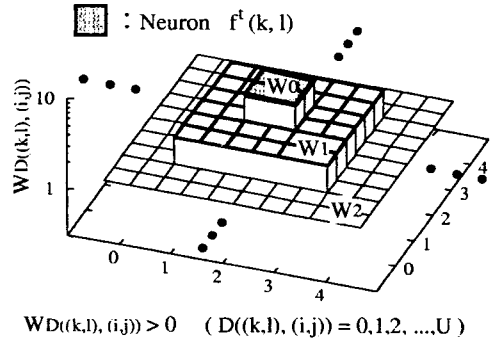


Fig.3 Fuzzification map for the noise elimination process.

the noise elimination process when the switches SW's are in the upper position. After the noise elimination finished, the positions of switches are reversed. Then, the proposed circuit calculates the center coordinates of the target pattern.

3 Algorithm

The algorithm of the proposed pattern recognition circuit is as follows.

Step1: For the input image, the initial values of the neurons, $f^0(i,j)$'s, are set to as follows:

$$f^t(i,j) \in \{0,1\} \qquad (t=0), \tag{1}$$

where 0 and 1 represent the values of the white and black pixels, respectively. In Eq.(1), $f^t(i,j)$ ($i \in \{1,\ldots,m\}$, $j \in \{1,\ldots,n\}$) denotes the value of the (i,j) neuron when the time is t.

Step2:

By connecting the switches SW's to the upper positions (see in Fig.2), the proposed circuit functions as a noise elimination circuit. For the neuron $f^t(k,l)$ ($k \in \{1,\ldots,m\}$, $l \in \{1,\ldots,n\}$) which corresponds to the black pixel, the neurons located within a chessboard distance U are weighted. The connection weights $W_{D((k,l),(i,j))}$ ($D((k,l),(i,j)) \in \{0,1,\ldots,\mathrm{U}\}$) are determined by a fuzzification map shown in Fig.3. Here, $D(\cdot)$ denotes the chessboard distance from (k,l) to (i,j). The fuzzification map shown in Fig.3 corresponds to the membership function of fuzzy systems. In the noise elimination process, the connection weights are determined to satisfy the following conditions:

$$W_q \geq \alpha^{\mathrm{U}-q} W_{\mathrm{U}} \qquad (q=0,1,2,\ldots,\mathrm{U}-1), \tag{2}$$

where α is a parameter which satisfies $\alpha > 1$. In case of the noise elimination process, the post synaptic potential for the neuron $f^t(i,j)$, $SP^t_{i,j}$, is given by

$$SP^t_{i,j} = \sum_{\{(i,j)|D((k,l),(i,j))\leq \mathrm{U}\}} f^t(k,l) W_{D((k,l),(i,j))}. \tag{3}$$

In other words, the Eq.(3) denotes the degree of overlap of the fazzification maps. Hence, $SP^t_{i,j}$ for a large cluster becomes higher than that for a small cluster.

Step3:

The noise elimination is performed as follows :

$$g^t(i,j) = \begin{cases} 0 & (SP^t_{i,j} < \mathrm{TH}^t), \\ 1 & (SP^t_{i,j} \geq \mathrm{TH}^t), \end{cases} \tag{4}$$

where TH^t is the threshold value. In Eq.(4), the threshold value TH^t is updated as follows:

$$\mathrm{TH}^{t+1} = \mathrm{TH}^t - W_{\mathrm{U}}, \tag{5}$$
$$\text{where} \qquad \mathrm{TH}^0 = \mathrm{U}W_0.$$

The noise elimination terminates when the total number of the black pixels, N^t, satisfies $N^{t+1} = N^t$ and $N^t \neq 0$.

Step4:

After the noise elimination finished, the positions of switches are reversed. Then, the proposed circuit calculates the center coordinates of the target pattern, $p^t(i,j)$. For the neuron $g^t(k,l)$ which is a part of the large cluster, the neurons located within a chessboard distance U are weighted. The post synaptic potential for the neuron $g^t(i,j)$, $SP^t_{i,j}$, is given by

$$SP^t_{i,j} = \sum_{\{(i,j)|D((k,l),(i,j))\leq \mathrm{U}\}} g^t(k,l) W_{\mathrm{U}-D((k,l),(i,j))}. \tag{6}$$

From Eq.(6), the post synaptic potential of the neuron $g^t(i,j)$ which corresponds to the center coordinates of the circular pattern becomes larger than that for other neurons since the radius of the circular pattern is equal to the parameter U.

Step5:

In the post synaptic potential obtained by Eq.(6), the neuron $g^t(i,j)$ which has the maximum value of $SP^t_{i,j}$ is extracted as a center coordinates of the target pattern. The center coordinates of the target pattern is extracted as follows :

$$p^t(i,j) = \begin{cases} 0 & (SP^t_{i,j} < \mathrm{TH}^t), \\ 1 & (SP^t_{i,j} \geq \mathrm{TH}^t). \end{cases} \tag{7}$$

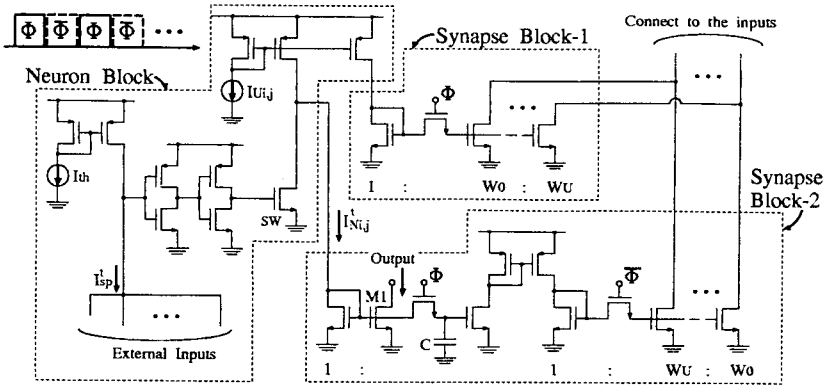


Fig.4 Neuron circuit designed by using current-mode techniques.

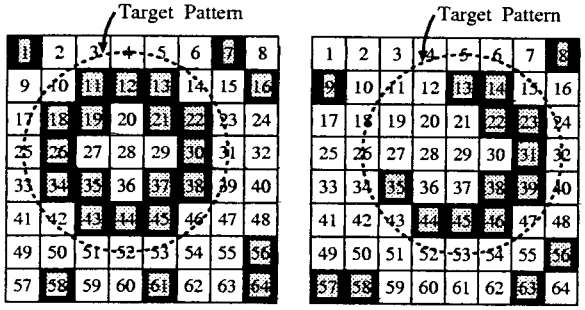


Fig.5 Input images used in SPICE simulations. (a) Image-1. (b) Image-2.

Thus, the neuron $g^t(i,j)$ is extracted as the center coordinates of the target pattern, $p^t(i,j)$, when $SP^t_{i,j} \geq \mathrm{TH}^t$. In Eq.(7), the threshold value TH^t is updated as follows:

$$\mathrm{TH}^{t+1} = \mathrm{TH}^t - W_{\mathrm{U}}, \qquad (8)$$

$$\text{where} \quad \mathrm{TH}^0 = W_0[2\pi \mathrm{U}].$$

In Eq.(8), $[\cdot]$ denotes Gauss' notation. The extraction process terminates when the total number of the black pixels, N^t, satisfies $N^t > 0$.

4 Hardware Implementation

Figure 4 shows the proposed pattern recognition circuit designed by using current-mode techniques. In Fig.4, the current sources, $\mathrm{I_{th}}$ and $\mathrm{I_{U}}_{i,j}$, correspond to the threshold value TH^t and the pixel value of the input image, $f^t(i,j)$, respectively. The external inputs $\mathrm{I_{sp}}^t$ corresponds to the post synaptic potential $SP^t_{i,j}$.

Firstly, the proposed circuit functions as a noise elimination circuit when the switches ϕ and $\bar{\phi}$ are on and off, respectively. The synapse block-1 calculates the synaptic potential $\mathrm{I}^t_{\mathrm{U}i,j} W_{D((k,l),(i,j))}$ for $f^t(i,j)$. In the synapse block-1, the connection weights are realized by the ratios of the current mirrors. The outputs of the synapse block-1 are connected to the neuron blocks which are located within a chessboard distance U. In the neuron block, the post synaptic potential $\mathrm{I_{sp}}^t$ for $f^t(i,j)$ is realized by wired-sum connection. From the output of the synapse block-1 the neuron block functions as

$$\mathrm{I}^t_{\mathrm{N}i,j} = \begin{cases} 0 & (\mathrm{I_{sp}}^t < \mathrm{I_{th}}), \\ \mathrm{I_{U}}_{i,j} & (\mathrm{I_{sp}}^t \geq \mathrm{I_{th}}), \end{cases} \qquad (9)$$

where $\mathrm{I}^t_{\mathrm{N}i,j}$ is the output of the neuron block. When the noise elimination process, the output of the neuron block, $\mathrm{I}^t_{\mathrm{N}i,j}$, which corresponds to $g^t(i,j)$ can be obtained from the NMOSFET $M1$. The output of the neuron block, $\mathrm{I}^t_{\mathrm{N}i,j}$, is stored in the capacitor C.

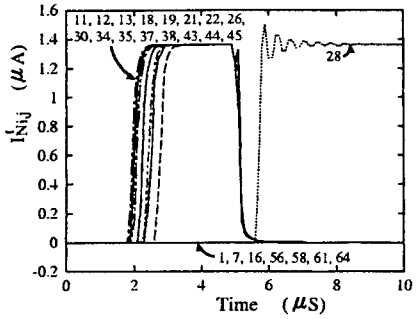
After the noise elimination finished, the switches ϕ and $\bar{\phi}$ are reversed. Then, the proposed circuit extracts the neuron which corresponds to the center coordinates of the circular pattern. The synapse block-2 calculates the synaptic potential $\mathrm{I}^t_{\mathrm{N}i,j} W_{\mathrm{U}-D((k,l),(i,j))}$ for $g^t(i,j)$, where $\mathrm{I}^t_{\mathrm{N}i,j}$ is provided from the capacitor C. The outputs of the synapse block-2 are connected to the neuron blocks which are located within a chessboard distance U. In the neuron block, the post synaptic potential $\mathrm{I_{sp}}^t$ for $g^t(i,j)$ is realized by wired-sum connection. From the output of the synapse block-2 the neuron block functions as

$$\mathrm{I}^t_{\mathrm{N}i,j} = \begin{cases} 0 & (\mathrm{I_{sp}}^t < \mathrm{I_{th}}), \\ \mathrm{I_{U}}_{i,j} & (\mathrm{I_{sp}}^t \geq \mathrm{I_{th}}), \end{cases} \qquad (10)$$

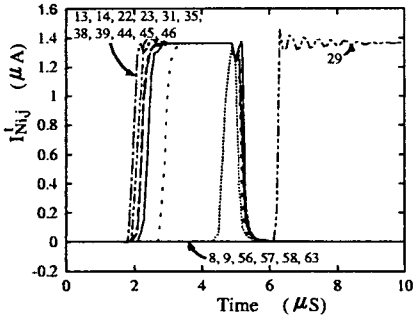
The output of the neuron block, $\mathrm{I}^t_{\mathrm{N}i,j}$, which corresponds to $p^t(i,j)$ can be obtained from $M1$.

5 Simulation

The SPICE simulations are perfomed regarding to 8 × 8-pixel input images shown in Fig.5. In Fig.5, $1 \sim 64$ are labels to specify the coordinates of the neurons. The SPICE simulations were performed under the conditions that the power supply was $\mathrm{V_{dd}} = 5\mathrm{V}$ and the bias current $\mathrm{Iu_{i,j}}$ was 1 μA. In the proposed circuit, the ratios of the current mirrors were set to



(a)



(b)

Fig.6 Transient characteristics of the proposed circuit. (a) Image-1. (b) Image-2.

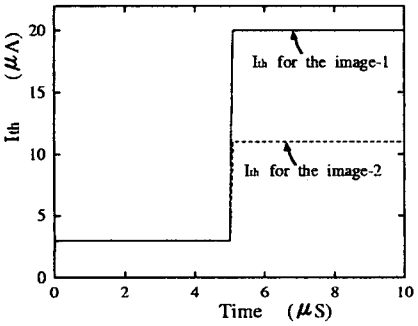
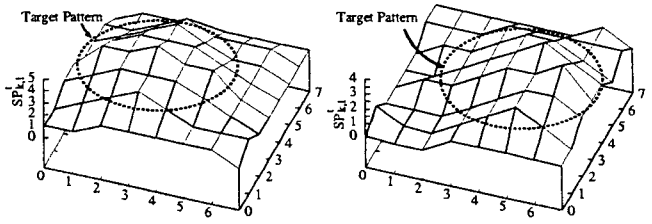


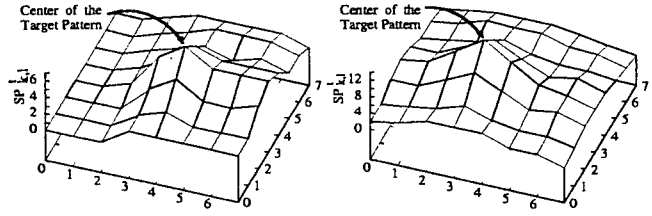
Fig.7 Threshold current I_{th}. (a) Image-1. (b) Image-2.

$W_0 = 1$, $W_1 = 0.5$, and $W_2 = 0.25$. Figure 6 shows the transient characteristics for the proposed circuit. In SPICE simulations, the threshold currents were set to the values shown in Fig.7. From 0 μs to 5 μs, the proposed circuit functions as a noise elimination circuit. And from 5 μs to 10 μs, the proposed circuit functions as an extraction circuit. Figures 8 and 9 show the post synaptic potentials for $f^t(i,j)$ and $g^t(i,j)$, respectively. Figure 10 shows the outputs of the proposed circuit. In Fig.10, the hatched images show the noise elimination results. And black pixels show the extracted neurons which are correspond to the center coordinates of the circular patterns. As one can see from Figs.6 and 10, the proposed circuit can extract the neurons which corresponds to the center coordinates of the circuilar patterns. From Figs.6, the settling time of the proposed circuit was less than 10 μs.



(a) (b)

Fig.8 Post synaptic potentials for $f^t(i,j)$. (a) Image-1. (b) Image-2.



(a) (b)

Fig.9 Post synaptic potentials for $g^t(i,j)$. (a) Image-1. (b) Image-2.

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64

(a)

1	2	3	4	5	6	7	8
9	10	11	12	13	14	15	16
17	18	19	20	21	22	23	24
25	26	27	28	29	30	31	32
33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48
49	50	51	52	53	54	55	56
57	58	59	60	61	62	63	64

(b)

Fig.10 Output images of the proposed circuit. (a) Image-1. (b) Image-2.

6 Conclusion

A neuro-fuzzy based circuit to recognize circular patterns is proposed in this paper. SPICE simulation results showed the following results: 1. The settling time of the proposed circuit was less than 10 μs. 2. Thanks to exemption from the use of template patterns as well as multipliers, the proposed circuit can be realized on the hardware of an economical scale. The proposed circuit is integrable by a standard CMOS technology.

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