Design of 1.5V-3GHz CMOS multi-chained two stage VCO

Hwa Yeal Yu, Se Hoon Oh, Yun Chol Han and Kwang Sub Yoon

*Dept. of Electronic Engineering, Inha University253
Younghyun-Dong, Nam-Gu, Inchon, 402-751, Korea
*E-mail : g1991212@inhavision.inha.ac.kr

Abstract

This paper proposes 1.5V-3GHz CMOS PLL with a new delay cell for operating in high frequency and multi chained two stage VCO to improve phase noise performance. The proposed multi-chained architecture is able to reduce a timing jitter or a transition spacing and the newly VCO is operating in high frequency. The PFD circuit designed to prevent fluctuation of charge pump circuit under the locking condition. Simulation results show that the tuning range of proposed VCO is wide at 1.8GHz~3.2Ghz and power dissipation is 0.6mW.

I. INTRODUCTION

During the last several years, there has been tremendous growth in wireless communication systems. These systems have been made possible by technological advances in the field of integrated circuits allowing a high level of integration at low cost and low power dissipation. There is also a great interest in integration of complete communication transceivers on a single chip.

Recently, a design of the high performance voltage controlled oscillator (VCO) such as LC-tank VCO and differential ring oscillator has demanded a higher operational frequency and a lower phase noise[1]. The CMOS LC-tank oscillator shows an excellent phase noise performance[2] because of a relatively high quality factor. However, its disadvantage includes a large die size due to the implementation of spiral inductor and a narrow tuning range[3][4]. In order to minimize a die size, design of CMOS differential ring oscillator has been practiced despite its inherent poor phase noise performance.

II. THE ARCHITECTURE OF PLL WITH MULTI-CHAINED TWO STAGE VCO

This paper proposes a multi-chained two stage CMOS VCO circuit, as shown in Fig. 1, based on a differential ring oscillator to improve a phase noise performance. The proposed multi-chained

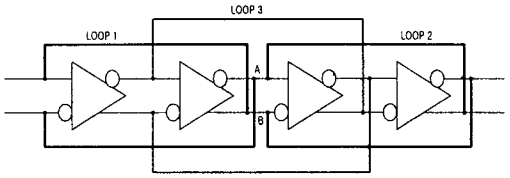

Fig. 1 Circuit diagram of the proposed multi-chained two stage VCO

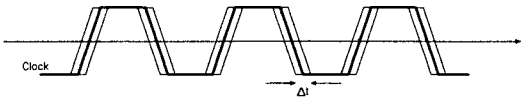

Fig. 2 General timing jitter.

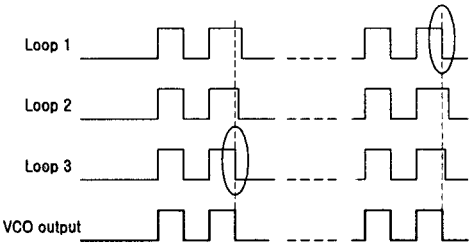

Fig. 3 The state decision diagram of output node A among three loops(#1, #2, #3).

architecture is able to reduce a timing jitter or a transition spacing illustrated in Fig. 2. The principle of the low phase noise operation of the proposed VCO is demonstrated in Fig. 3. The state of the node A is determined by the fastest timing response among three loops. In other words, the falling edge of the second clock of the VCO outputs is determined by that of the loop #3 and the falling edge of the last clock is determined by that of the loop #1. In this manner, the timing jitter can be decreased in a time domain. The height of the phase noise sidebands due to thermal noise in device is generally proportional to the normalized timing jitter variance[5]. The generated phase noise can be approximated as follows :

$$S_{\phi} = \frac{f_o}{f_{m2}}\left[\frac{\Delta t_{vco-rms}}{T_o}\right]^2 \qquad (1)$$

where f_m is the center frequency, f_o is the offset

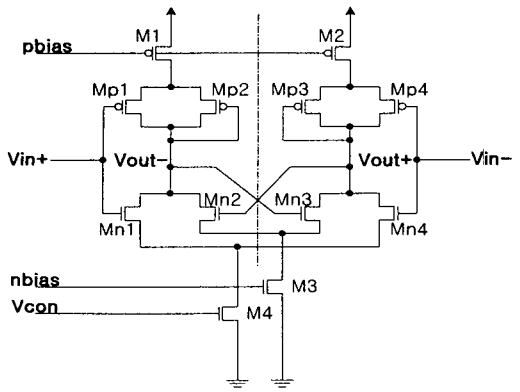

Fig. 4 Circuit schematic of the proposed delay cell.

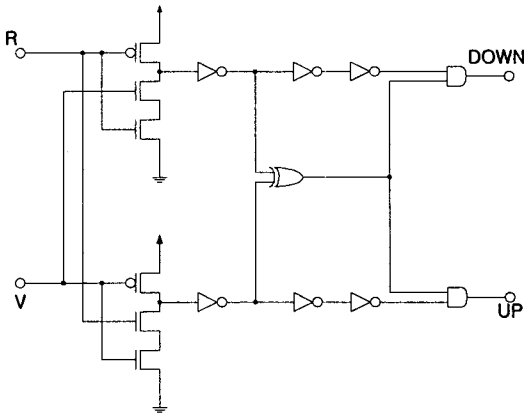

Fig. 5 The Circuit schematic of the proposed PFD.

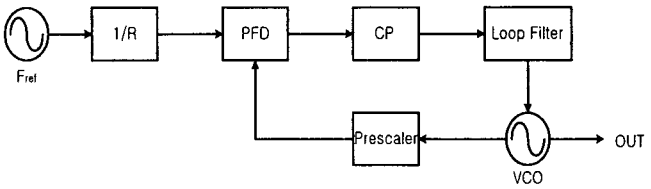

Fig. 6 The block diagram of integer N frequency synthesizer.

frequency from the carrier, T_o is the oscillation period, and $\triangle t_{vco\text{-}rms}$ is a single stage jitter variance. According to (1), the ring oscillator with a short jitter variation, $\triangle t_{vco\text{-}rms}$, is expected to exhibit a low phase noise.

The proposed multi-chained two stage VCO consists of four identical delay cells whose circuit diagram is shown in Fig. 4. The architecture of the newly designed differential delay cell is symmetrical with respect to the dotted line. Each half delay cell circuit consists of one inverter (Mp1/Mn1 and Mp4/Mn4) with a latch circuit (Mn2 and Mn3), an active load (Mp2 and Mp3), and bias circuits (M1, M2, M3, M4). The oscillation frequency of the proposed VCO can be described by :

$$f = \frac{1}{2\pi \cdot N \cdot R_o \cdot C_o} \tag{2}$$

Where N is a number of the delay cell (which is equal to 2 in this design), R_o is an output resistance of each delay cell inversely proportional to a magnitude of the current, and C_o is a total capacitance at the output node of each delay cell. The output resistance, R_o is in parallel with R_{op} and R_{on}, where R_{op} and R_{on} are the resistances looking toward PMOS devices and NMOS devices, respectively. R_o can be approximated as :

$$R_o = R_{op} // R_{on} \equiv \left(\frac{g_{mp2}}{g_{mp3}} \cdot r_{op2}\right) // \left(\frac{1}{2} g_{mn3} \cdot r_{on3}^{\,2}\right) \approx \frac{g_{mp2}}{g_{mp3}} \cdot r_{op2} = \sqrt{\frac{\left(\frac{W}{L}\right)_{p2}}{\left(\frac{W}{L}\right)_{p3}}} \cdot r_{op2} \tag{3}$$

,where g_{mp2}, g_{mp3} and g_{mn3} are transconductances of M2, Mp3 and M3, r_{op2} and r_{on3} are output resistance of M2 and M3, respectively. C_o can be described by :

$$C_o = C_{gdp4} + C_{bdp4} + C_{bdp3} + C_{gdn3} + C_{bdn3} + C_{gdn4} + C_{bdn4} \tag{4}$$

where C_{gdi} and C_{bdi} are gate-to-drain parasitic capacitance and drain-to-substrate parasitic diffusion capacitance of i^{th} MOS device, respectively. Substituting (3) and (4) into (2), it results in (5).

$$f_o = \frac{1}{2\pi \cdot N \cdot C_o \cdot \sqrt{\frac{\left(\frac{W}{L}\right)_{p2}}{\left(\frac{W}{L}\right)_{p3}}} \cdot r_{op2}} \tag{5}$$

Therefore the oscillation frequency, f_o is inversely proportional to N, C_o, and the (W/L) ratio of two PMOS devices, Mp2 and Mp3, and r_{op2}. In order to increase the oscillation frequency, a magnitude of the current flowing through bias circuits of the delay cell should be enhanced because of r_{op2} inversely proportional to the current. The latch circuit (Mn2 and Mn3) is utilized not only to provide a positive feedback path, but also to reduce the delay time. Diode-connected devices, Mp2 and Mp3 are employed to lower the output resistance of the delay cell and consequently, to increase f_o. A replica bias circuit is used to adjust the gate bias of the PMOS load device for a fixed swing output.

The proposed phase frequency detector(PFD), as

shown in Fig. 5, is designed that the part of UP signal and DOWN signal are symmetrical. Two additional AND and EX-OR gates prevent the charge pump circuit under the locked condition from fluctuation. The designed architecture of the PFD circuit prevents VCO from suffering from output jitter under the locked condition.

The block diagram of PLL based frequency synthesizer, as shown in Fig. 6, appears the structure of a conventional integer N frequency synthesizer. The dual-modulus prescaler includes a synchronous counter (divide-by-4/5) and an asynchronous counter (divide-by-32).

III. SIMUALTION RESULTS

Design of the proposed VCO circuit with a power supply of 1.5V is made by a 0.25μm standard CMOS n-well sing poly / five metal process. The overall voltage to frequency characteristic curve of the proposed VCO is plotted in Fig. 7. The Hspice simulation results are shown in Fig. 8 and Fig. 9 illustrates the oscillation frequency of the VCO to be 1.8GHz @ V_{con}=0.1V and 3.2GHz @ V_{con} =1.4V. It demonstrates that the proposed VCO is capable of operating between 1.8GHz and 3.2GHz with a nonlinear characteristic. The pull in process characteristic of PLL at 3.0GHz @ 95MHz input frequency is shown in Fig. 10. The simulated performance of the proposed VCO is summarized in Table 1.

IV. CONCLUSIONS

In conclusions, a 1.5V-3GHz multi-chained two stage VCO circuit is proposed to operate between 1.8GHz @ V_{con} =0.1V and 3.2GHz @ V_{con} =1.4V with a power dissipation of 0.6mW.

The proposed VCO which includes four newly designed delay cells will be able to exhibit a low phase noise, a low power dissipation, and a high frequency operation.

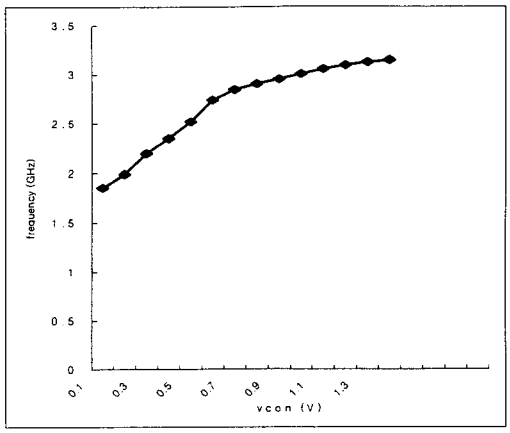

Fig. 7 The voltage to frequency characteristic curve of the proposed VCO.

Table 1. Summary of the simulated performance of the proposed VCO.

Frequency	1.8GHz ~3.2GHz
Power dissipation	0.6mW @ 3.2GHz
VCO gain	964MHz/V
Supply voltage	1.5V
Technology	0.25μm 1-poly 5-metal CMOS technology

V. ACKNOWLEDGEMENT

This research was supported by the grant of KOSEF (contact No: 1999-2-302-002-3)

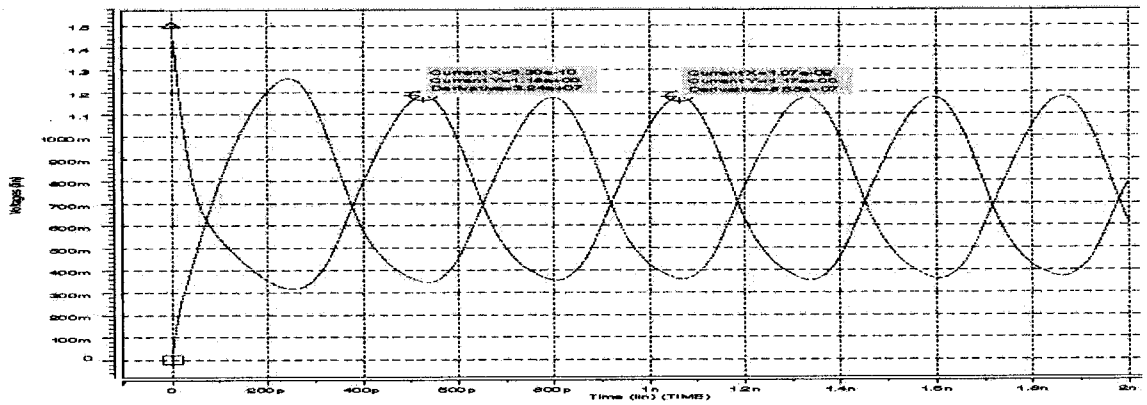

Fig. 8 The simulated plot of the oscillation wave of the proposed VCO at 1.8GHz @ Vcon=0.1V.

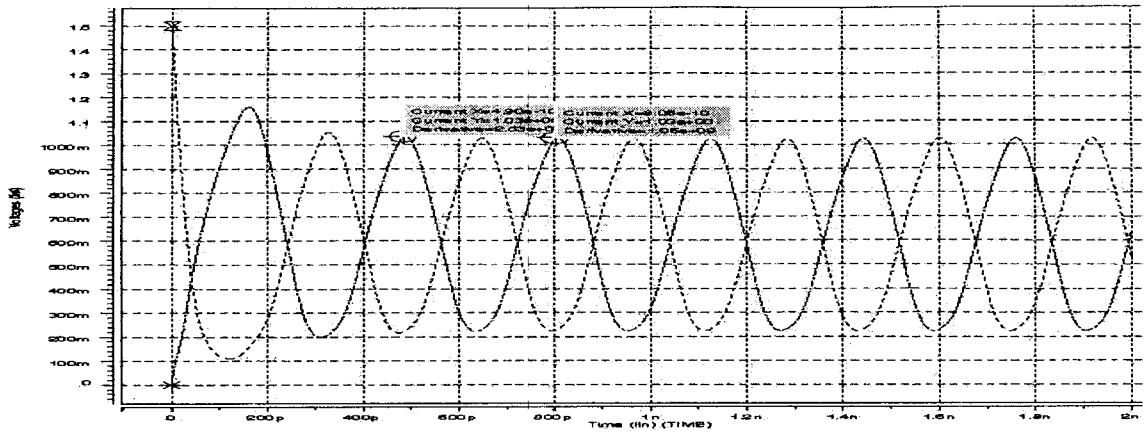

Fig. 9 The simulated plot of the oscillation wave of the proposed VCO at 3.2GHz @ Vcon=1.4V.

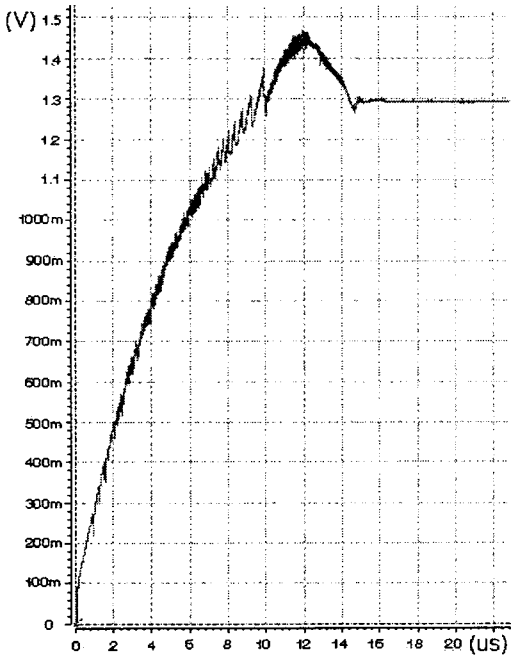

Fig. 10 Pull in process characteristic at 3.0GHz @ 95MHz input frequency

REFERENCE

[1] C. Park and B. Kim, "A Low-Noise, 900MHz VCO in 0.6μm CMOS," IEEE J.Solid-State Circuits, vol 34, pp. 586-590, May 1999.

[2] Mihai A. Margarit, Joo Leong Tham and Robert G. Meyer, "A Low-Noise, Low-Power VCO with Automatic Amplitude Control for Wireless Applications," IEEE J.Solid-State Circuits, vol 34, pp. 761-771, June 1999.

[3] A. Rofourgan, J. Rael, M. Rofourgan and A. Abidi, "A 900MHz CMOS LC-oscillator with quadrature outputs," in ISSCC Dig. Tech.Papers, San Francisco, CA, pp.392-393 Feb. 1996.

[4] J. Craninckx and M. Steyaert, "A 1.8GHz low-phase noise CMOS VCO using optimized hollow spiral inductors," IEEE J.Solid-State Circuits, vol 32, pp. 763-744, May 1997.

[5] Ali Hajimiri and Thomas H. Lee, The Design of Low Noise Oscillators, Kluwer Academic Publishers, 1999.