

A New Small Signal Modeling of RF MOSFETs including Charge Conservation Capacitances

Ickjin Kwon, Minkyu Je, Kwyro Lee, and Hyungcheol Shin
 Department of EECS, Korea Advanced Institute of Science and Technology,
 373-1 Kusong-dong Yusong-gu, Taejon, 305-701, Korea
 Tel: +82-042-869-5459, Fax: +82-042-869-8590
 E-mail: ijkwon@inca.kaist.ac.kr

Abstract: A novel extraction method of high frequency small-signal model parameters for MOSFETs is proposed. From S-parameter measurement, this technique accurately extracts the model parameters including the charge conservation capacitance parameters. To consider charge conservation, nonreciprocal capacitance is considered. The modeled parameters fit the measurements very well without any optimization.

1. Introduction

As the gate-length of MOSFET reduces, its high frequency characteristics improve [1][2]. MOSFETs are good candidate for RF IC application because of low cost, high integration, and one-chip solution possibility for analog and digital circuit. The extraction of small-signal equivalent circuit parameters is important for the development of accurate large signal model. Recently, many suggestions have been made to improve the prediction of high frequency properties by simple modification to the conventional low-to-medium frequency MOSFET equivalent circuit. A few methods of extracting small-signal equivalent circuit parameters have been reported [3]-[5]. But they are based on the MESFET model and complex curve fitting and optimization methods are required. Also, they didn't consider charge conservation capacitance parameters which are very important in intrinsic capacitance modeling.

In this paper, we have developed a new systematic parameter extraction method of MOSFET including charge conservation capacitance parameters from measured S-parameters and verified that its results match well with measured data. This work is based on physical small signal equivalent circuit of the RF MOSFET and accurate parameter extraction approach by Y-parameter analysis from measured S-parameters. The gate resistance which significantly affects the input admittance and substrate coupling effects through the drain, source junctions and the substrate resistance which affect the output admittance are also included in the proposed model. It can be used together with conventional MOSFET compact models for RF application [6]-[8].

2. Parameter Extraction Method

The common-source equivalent circuit of the MOSFET after de-embedding parasitics of on-wafer pads and interconnection lines is shown in figure 1. The

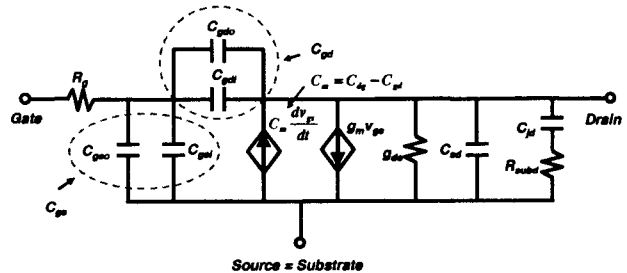


Figure 1. The proposed common-source equivalent circuit after parasitics of on-wafer pads and interconnection lines are de-embedded.

circuit elements associated with the substrate and source are excluded because the substrate is short-circuited to the source as in most high-frequency application. The resistance R_g represents the effective channel resistance which consists of the distributed channel resistance seen from the gate and the distributed gate electrode resistance. The drain junction capacitance and the bulk spreading resistance is represented by C_{jd} and R_{subd} . For simple circuit representation, the intrinsic capacitances C_{gsi} , C_{gdi} , and the extrinsic capacitances C_{gso} , C_{gdo} are merged into C_{gs} , C_{gd} . Because the source and the substrate are connected to the common, C_{gs} includes the gate-to-source capacitance and the gate-to-substrate capacitance. Also, C_{sd} includes the drain-to-source capacitance and drain-to-substrate capacitance.

C_{dg} and C_{gd} are the two non-reciprocal capacitance components [9][10]. The capacitive effect of drain on gate is represented by C_{gd} , and the capacitive effect of gate on drain is represented by C_{dg} , in terms of charging currents. $C_m = C_{dg} - C_{gd}$ is a transcapacitance taking care of the different effect of the gate and drain on each other. There is no reason to expect that the two effects are the same in general, just as there is no reason to expect that, at dc, the effect of the drain on the gate current is the same as the effect of the gate on the drain current. If C_{gd} and C_{dg} are set to be equal as in the most conventional models, large error can be introduced since charge conservation does not hold.

The new extraction procedure uses a linear regression approach for the Y-parameters which are converted from measured S-parameters. The small-signal equivalent circuit shown in figure 1 can be analyzed in terms of Y-parameters as follows,

$$Y_{11} = \frac{j\omega(C_{gs} + C_{gd})}{1 + j\omega(C_{gs} + C_{gd})R_g} \quad (1)$$

$$Y_{12} = \frac{-j\omega C_{gd}}{1 + j\omega(C_{gs} + C_{gd})R_g} \quad (2)$$

$$Y_{21} = \frac{g_m - j\omega C_{dg}}{1 + j\omega(C_{gs} + C_{gd})} \quad (3)$$

$$Y_{22} = g_{ds} + \frac{j\omega C_{jd}}{1 + j\omega C_{jd} R_{subd}} + j\omega C_{ds} + j\omega C_{gd} + \frac{\omega^2 C_{gd} C_{dg} R_g + j\omega g_m C_{gd} R_g}{1 + j\omega(C_{gs} + C_{gd}) R_g} \quad (4)$$

For operation frequency up to 10 GHz, by using the assumption that $\omega^2(C_{gs} + C_{gd})^2 R_g^2 \ll 1$, it can be approximated as following.

$$Y_{11} = \omega^2(C_{gs} + C_{gd})^2 R_g + j\omega(C_{gs} + C_{gd}) \quad (5)$$

$$Y_{12} = -\omega^2 C_{gd}(C_{gs} + C_{gd}) R_g - j\omega C_{gd} \quad (6)$$

$$Y_{21} = g_m - \omega^2 C_{dg}(C_{gs} + C_{gd}) R_g - j\omega C_{dg} - j\omega g_m R_g (C_{gs} + C_{gd}) \quad (7)$$

$$Y_{22} = g_{ds} + \frac{\omega^2 C_{jd}^2 R_{subd}}{1 + \omega^2 C_{jd}^2 R_{subd}^2} + \omega^2 C_{gd} C_{dg} R_g + \omega^2 g_m R_g^2 C_{gd} (C_{gs} + C_{gd}) + \frac{j\omega C_{jd}}{1 + \omega^2 C_{jd}^2 R_{subd}^2} + j\omega C_{ds} + j\omega C_{gd} + j\omega g_m C_{gd} R_g - j\omega^3 C_{gd} C_{dg} (C_{gs} + C_{gd}) R_g^2 \quad (8)$$

Parameter extraction is performed from real and imaginary parts of Y-parameters. C_{gs} , R_g , C_{gs} , g_m , C_{dg} , g_{ds} can be obtained by (9)-(14). g_m and g_{ds} are obtained from y-intercept of $\text{Re}[Y_{21}]$ versus ω^2 and from intercept of $\text{Re}[Y_{22}]$ versus ω^2 , respectively.

$$C_{gd} = -\text{Im}[Y_{12}] / \omega \quad (9)$$

$$R_g = \text{Re}[Y_{11}] / (\text{Im}[Y_{11}])^2 \quad (10)$$

$$C_{gs} = (\text{Im}[Y_{11}] + \text{Im}[Y_{12}]) / \omega \quad (11)$$

$$g_m = \text{Re}[Y_{21}] \Big|_{\omega^2=0} \quad (12)$$

$$C_{dg} = -\text{Im}[Y_{21}] / \omega - g_m R_g (C_{gs} + C_{gd}) \quad (13)$$

$$g_{ds} = \text{Re}[Y_{22}] \Big|_{\omega^2=0} \quad (14)$$

R_{subd} and C_{jd} are obtained from linear regression of the following relations from $\text{Re}[Y_{22}]$.

$$Y \equiv \frac{\omega^2}{\text{Re}[Y_{22}] - g_{ds} - \omega^2 C_{gd} C_{dg} R_g - \omega^2 g_m R_g^2 C_{gd} (C_{gs} + C_{gd})} \quad (15)$$

$$= \omega^2 R_{subd} + \frac{1}{C_{jd}^2 R_{subd}}$$

R_{subd} is determined from slope of Y as a function of ω^2 and C_{jd} is extracted as

$$C_{jd} = [(Y - \omega^2 R_{subd}) R_{subd}]^{-1} \quad (16)$$

Finally, C_{ds} is obtained from (4) as

$$C_{ds} = \frac{\text{Im}[Y_{22}]}{\omega} - C_{gd} - \frac{C_{jd}}{1 + \omega^2 C_{jd}^2 R_{subd}^2} - g_m R_g C_{gd} + \omega^2 C_{gd} C_{dg} (C_{gs} + C_{gd}) R_g^2 \quad (17)$$

3. Experiments and Results

The test devices are multi-fingered n-MOSFET's fabricated by 0.35 μm technology. The parameter extraction has been performed for an n-MOSFET with 100 μm width. To remove on-wafer pad parasitics, de-embedding technique was carried out by subtracting S-parameters of open pad structure from measured device S-parameters. The small signal parameters including charge conservation capacitance parameters are extracted using (9)-(17). $R_g = 8.8 \Omega$, $g_m = 21.3 \text{ mS}$ and $g_{ds} = 0.94 \text{ mS}$ were extracted and R_{subd} of 203.4 Ω was determined by (15) as shown in figure 2.

The frequency dependence of extracted small-signal parameters at $V_{gs} = 2 \text{ V}$ and $V_{ds} = 2 \text{ V}$ are shown in figure

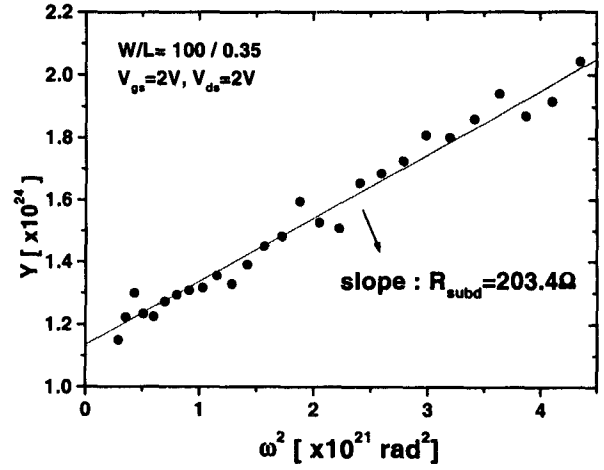


Figure 2. R_{subd} was determined from the slope of Y as a function of ω^2 by (15).

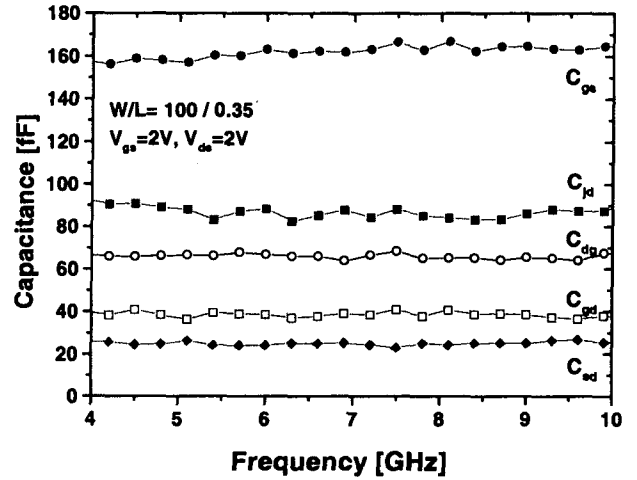


Figure 3. The frequency dependence of extracted parameters for an n-MOSFET having 100 μm width and biased at $V_{gs} = 2 \text{ V}$, $V_{ds} = 2 \text{ V}$.

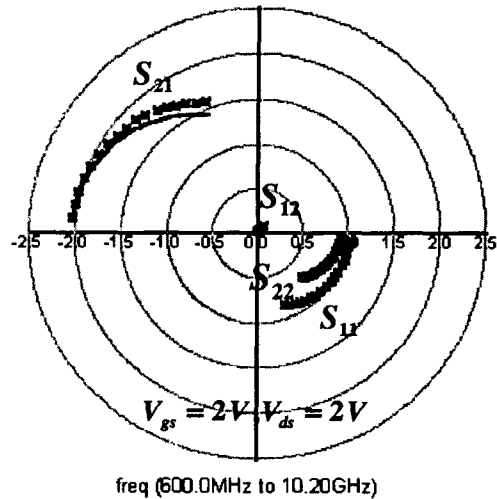


Figure 4. The measured and modeled S-parameters for the n-MOSFET biased at $V_{gs} = 2 \text{ V}$, $V_{ds} = 2 \text{ V}$. The symbols represent the measured data and the solid lines represent the modeled ones.

3. The results shows that extracted parameters remains almost constant with frequency and verifies that this extraction method is accurate and reliable. Due to the

non-reciprocity, C_{dg} is larger than C_{gd} . The total gate capacitance $C_{gg} \approx C_{gs} + C_{gd}$ in saturation region at $V_{gs} = 2$ V and $V_{ds} = 2$ V is about 187.5 fF including the overlap capacitance. This value is very close to the calculated result of total gate oxide capacitance.

Figure 4 compares the measured and modeled S-parameters. The symbols represent the measured data and the solid lines represent modeled ones. It shows that the modeled S-parameters fit the measured ones very well without any optimization. For the extracted parameter values, $\omega^2(C_{gs} + C_{gd})^2 R_g^2$ is calculated to be 0.01 at 10 GHz, which is much smaller than one. This verifies the validity of using the assumption in simplifying (1)-(4) to (5)-(8). The total error [12] between the measured and the extracted S-parameters of the proposed model is only 0.6 %.

Figure 5 and figure 6 show the gate-bias dependence of the extracted small-signal parameters for the n-MOSFET biased to $V_{ds} = 2$ V. As gate bias increases for constant V_{ds} , saturation-to-linear region transition is occurred. C_{gd} is dominated by extrinsic capacitance C_{gdo} in the saturation region and almost constant. In the linear region, C_{gd} increases due to increase of gate-to-drain intrinsic capacitance. The smooth behaviors for C_{gs} , C_{gd} and C_{dg} are observed because the region-to-region transition is very gradual due to short-channel effects. Extracted R_g has weak gate bias dependency and decreases as gate bias increase as shown in figure 6. R_{subd} is almost constant with gate bias.

In figure 7, gate-bias dependence of the g_m and g_{ds} for the n-MOSFET biased to $V_{ds} = 2$ V are shown. We have compared extracted g_m and g_{ds} to extracted values from DC current-voltage (I-V) measurements and simulated values with BSIM3v3 model [11]. Drain conductance g_{ds} increases almost proportional to gate bias in the saturation region due to short channel effects and g_{ds} rapidly increases with V_{gs} in the linear region because for higher gate bias drain current increases more rapidly with drain bias in the linear region. As shown in figure 7, extracted g_m and g_{ds} matched well with measured values from DC I-V measurements and, also, simulated values from BSIM3v3 model.

Figure 8 and figure 9 show the drain-bias dependence of the extracted small-signal parameters for the n-MOSFET biased to $V_{gs} = 2$ V. C_{gdi} and C_{gsi} are almost same when $V_{ds} = 0$ V because in linear region gate-to-drain capacitance and gate-to-source capacitance are almost same. In figure 8, the difference between C_{gd} and C_{gs} at $V_{ds} = 0$ V is due to gate-to-substrate capacitance C_{gsb} including the extrinsic capacitance. As drain bias increases for constant V_{gs} , linear-to-saturation region transition is occurred. So, C_{gs} increases and C_{gd} decreases with drain bias. In the saturation region for higher V_{ds} , intrinsic gate-to-drain capacitance C_{gdi} approached to zero and C_{gd} is almost same as C_{gdo} . C_{sd} is negative in linear region because raising the drain voltage will increase the effective reverse bias at the drain end and will cause the magnitude of the inversion layer charges to decreases.

Extracted R_g and R_{subd} is almost independent with drain bias as shown in figure 9. In figure 10, drain-bias dependence of the g_m and g_{ds} for the n-MOSFET biased

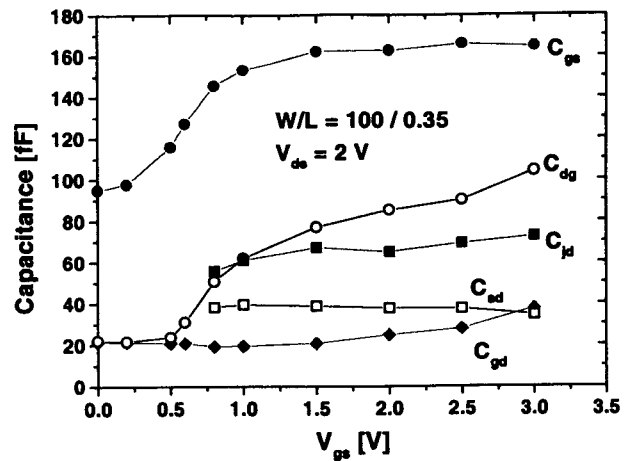


Figure 5. The gate-bias dependence of the capacitance parameters for the n-MOSFET biased at $V_{ds} = 2$ V.

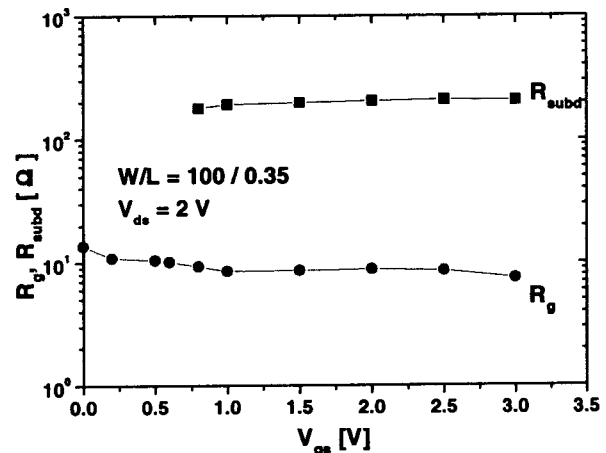


Figure 6. The gate-bias dependence of the R_g and R_{subd} for the n-MOSFET biased at $V_{ds} = 2$ V.

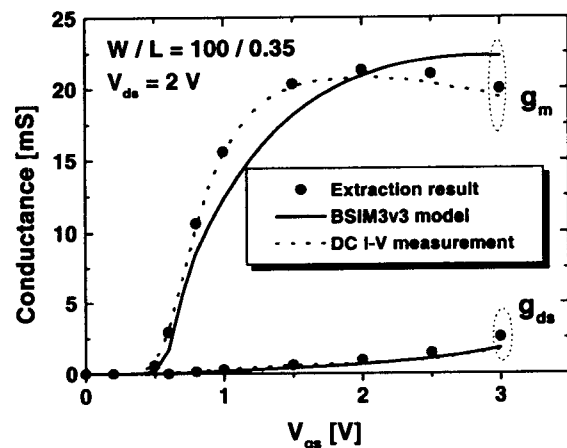


Figure 7. Conductance g_m and g_{ds} as a function of V_{gs} for the n-MOSFET biased at $V_{ds} = 2$ V.

to $V_{gs} = 2$ V are shown. g_m increases and g_{ds} decrease as drain bias increases. Also, extracted g_m and g_{ds} matched well with the values from DC I-V measurements.

Because the determination of capacitance parameters based on large C-V test structure measurement is inaccurate in the high frequency range, the proposed parameter extraction method can be applied to accurate intrinsic capacitance modeling at the gigahertz operation.

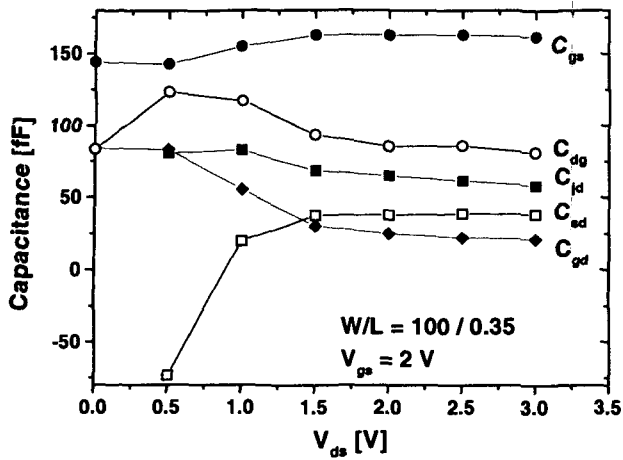


Figure 8. The drain-bias dependence of the capacitance parameters for the n-MOSFET biased at $V_{gs} = 2$ V.

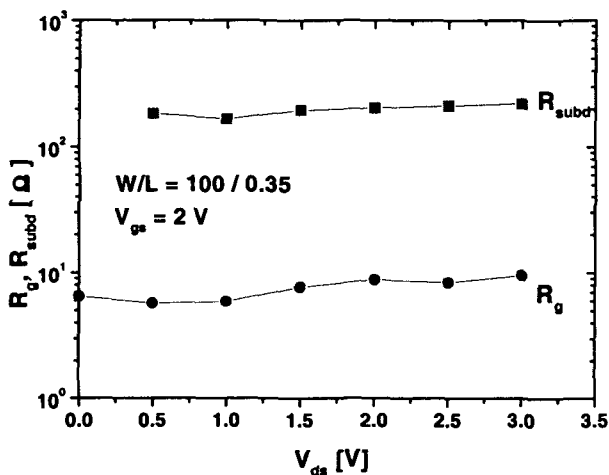


Figure 9. The drain-bias dependence of the R_g and R_{subd} for the n-MOSFET biased at $V_{gs} = 2$ V.

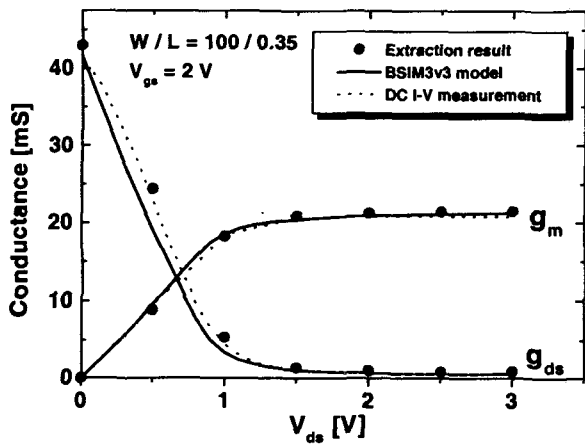


Figure 10. Conductance g_m and g_{ds} as a function of V_{ds} for the n-MOSFET biased at $V_{gs} = 2$ V.

4. Conclusions

A novel extraction method of obtaining an accurate high frequency small-signal parameters for MOSFETs has been demonstrated. This technique accurately extracted the model parameters including the charge conservation capacitance parameters. The proposed model from

parameter extraction has been evaluated with measured data and good agreement has been observed. The modeled parameters fit the measurements very well without any optimization.

5. Acknowledgement

This work was supported by the SILVACO international and the system 2010 program. And this works was supported in part by the Korea Science and Engineering foundation through the MICROS center at KAIST.

References

- [1] C. Wann, L. Su, K. Jenkins, R. Chang, D. Frank, Y. Taur, "RF Perspective of Sub-Tenth-Micron CMOS", *IEEE International Solid-State Circuits Conference*, pp. 254-255, 1998.
- [2] E. Morifuji, et al., Future perspective and scaling down roadmap for RF CMOS, Symposium on VLSI Technology Digest of Technical Papers, 1999, pp. 163-164.
- [3] D. Lovelace, J. Costa, N. Camilleri, "Extracting Small-Signal Model Parameters of Silicon MOSFET Transistors", *IEEE MTT-S Digest*, 1994, pp.865-868.
- [4] G. D. Dambrine, A. Cappy, F. Helidore, and E. Palyze, "A new method for determining the FET small-signal equivalent circuit", *IEEE Trans. Microwave Theory Tech.*, vol. 36, pp. 173-176.
- [5] S. Lee, H. K. Yu, C. S. Kim, J. G. Koo, and K. S. Nam, "A novel approach to extracting small-signal model parameters of silicon MOSFET's", *IEEE Microwave and guided wave letters*, vol. 7, pp. 75-77, 1997.
- [6] W. Liu, R. Gharpurey, M. C. Chang, U. Erdogan, R. Aggarwal, and J. P. Mattia, "RF MOSFET modeling accounting for distributed substrate and channel resistance with emphasis on the BSIM3v3 SPICE model", in *IEDM tech. Dig.*, pp.309-312, Dec. 1997.
- [7] Jia-Jiunn Ou, Xiadong Jin, Ingrid Ma, Chenming Hu, "CMOS RF modeling for GHz communication IC's", *VLSI Symp. On Tech., Dig. Of Tech. Papers*, pp. 94-95, June 1998.
- [8] D. R. Pehlke, M. Schroder, A. Burstein, M. Matloubian, M. F. Chang, "High frequency application of MOS compact model and their development for scalable RF model libraries", *Proc. of CICC*, pp. 219-222, May 1998.
- [9] Ping Yang, Berton D. Epler, Pallab K. Chatterjee, "An Investigation of the Charge Conservation Problem for MOSFET Circuit Simulation", *IEEE Journal of Solid-State Circuits*, vol. Sc-18, no. 1, Feb, 1983.
- [10] Y. Tsvividis, *The Operation and Modeling of the MOS Transistor*, McGraw-Hill, 1987.
- [11] Weidong Liu et al., *BSIM3v3.2 MOSFET model User's Manual*, University of California, Berkeley, 1998.
- [12] Charlotte E. Biber, et al., "A Nonlinear Microwave MOSFET Model for SPICE simulators", *IEEE Trans. Microwave Theory Tech.*, vol. 46, pp. 604-610, May 1998.