A 3.3V 10BIT CURRENT-MODE FOLDING AND INTERPOLATING CMOS A/ D CONVERTER USING AN ARITHMETIC FUNCTIONALITY

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Abstract

A low power 10bit current-mode folding and interpolating CMOS analog to digital converter (ADC) with arithmetic folding blocks is presented in this paper. A current-mode two-level folding amplifier with a high folding rate (FR) is designed not only to prevent ADC from increasing a FR excessively, but also to perform a high resolution at a single power supply of 3.3V The proposed ADC is implemented by a 0.6μm n-well CMOS single poly/double metal process. The simulation result shows a differential nonlinearity (DNL) of ±0.5LSB, an integral nonlinearity (INL) of ±1.0LSB

I. INTRODUCTION

High speed ADC are required to not only to interface analog signal to digital signal processing systems but also the using of digital CMOS process that allows the use of ADC in mixed analog-digital signal processing systems. due to the rapid development in digital CMOS technology, more and more functionality can be integrated onto a single chip. Single-chip solutions are becoming an attractive approach for systems with increasing complexity. since, the current-mode circuit technique is expected to handle essentially a higher speed operation and lower power dissipation than previously used for voltage-mode circuits [1]-[3].

In this work, the current-mode circuit employed in the ADC should be able to offer essentially a lower power dissipation than the voltage-mode circuit reported previously. On the other hand, the conventional folding amplifiers with a high FR can give rise to a nonlinearity error due to device mismatches, since they usually employ a large number of the reference current sources. It results in a large power dissipation of the ADC. Increasing the folding factor is only efficient when it justifies the decrease in the number of comparotors to realize a low power, small chip size . By the way of this analog preprocessing of the A/D converter is resulted into the high folding factor based on improved high resolution implementation for video-channel receiver applications in the booming market of telecommunication wireless equipment.

II. THE 10 BIT CURRENT-MODE CMOS ADC USING ARITHMETIC FUNCTIONALITY

The block diagram of the proposed 10bit current-mode folding and interpolating ADC is presented in Fig. 1.

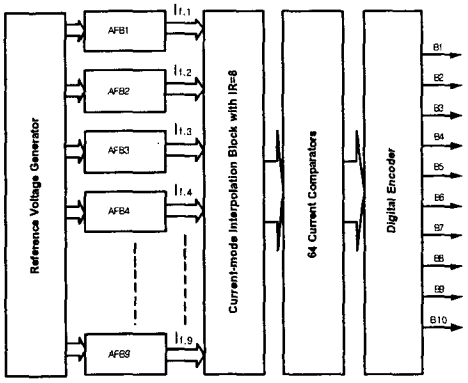

Fig. 1. Block diagram of the proposed 10bit current-mode folding and interpolating ADC.

The proposed ADC consists of 9 arithmetic folding blocks (AFB1, AFB2, AFB3, ..., AFB9) in parallel, a current-mode interpolating block, 64 current comparators, a digital encoder, and reference voltage generator. In order to implement a 10bit resolution of the proposed ADC architecture with a maximum input frequency, the folding rate (FR) and the interpolating rate(IR) are

chosen as 128 and 8, respectively. The maximum input frequency of the folding ADC, $f_{in,max}$ can be

$$f_{in,\max} = \frac{2BW}{\pi \cdot FR} \qquad (1)$$

given as:

where BW (analog bandwidth) is proportional to the voltage gain of a folding amplifier within ADC [4],[5].

The 128(=8×16) FR can be achieved by 9 arithmetic folding blocks whose FR is 16. The proposed architecture to process folding signals heavily depends on a simple arithmetic manipulation such as addition and subtraction. The block diagram of the arithmetic folding block (AFB) is shown in Fig. 2.

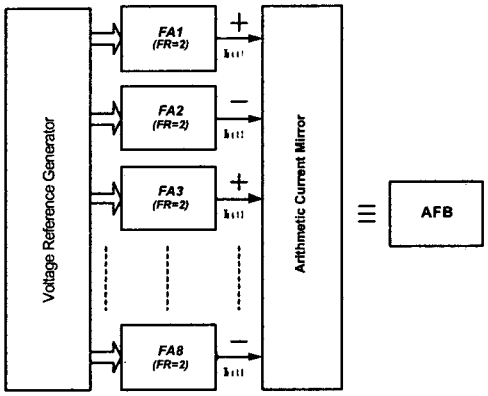

Fig. 2. Block diagram of the a rithmetic folding block (AFB) with addition and subtraction function.

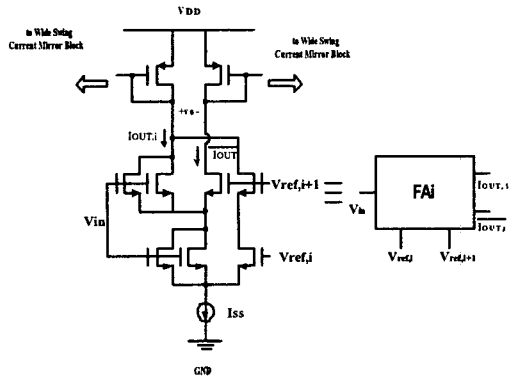

Fig. 3. Circuit schematic of two-level folding amplifier (FA).

It includes a voltage reference generator, 9 two-level folding amplifiers (FA), and an arithmetic current mirror. In order to generate fully differential current signals, $I_{out,i}$ and $I_{out,i}$ from a FA, two adjacent reference voltages, $V_{ref,i}$ and $V_{ref,i+1}$ should satisfy the following condition:

$$\Delta V_{ref} = \left| V_{ref(i+1)} - V_{ref(i)} \right| \geq 2\sqrt{\frac{2I_{ss}}{\beta_n}} \qquad (2)$$

where Iss and â are a bias current and device transconductance parameter, respectively. The two-level folding amplifier shown in Fig. 3 consists of two differential pairs serially connected, two reference voltages and one reference current source. The nine differential folding signals from FA can be successively added by an arithmetic current mirror (ACM), as shown in Fig.4.

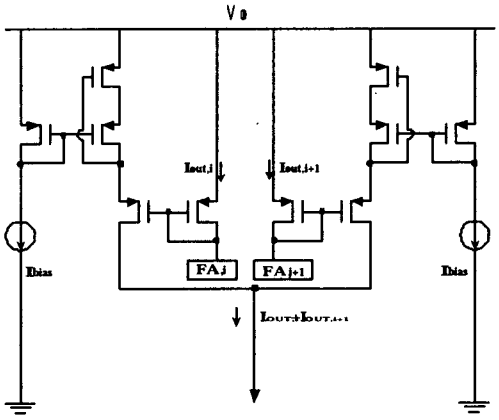

Fig. 4. Circuit diagram of the arithmetic current mirror (ACM).

It produces the resultant folding signal, $I_{f,i}$ with FR of 16. This signal processing procedure is illustrated in Fig. 5.

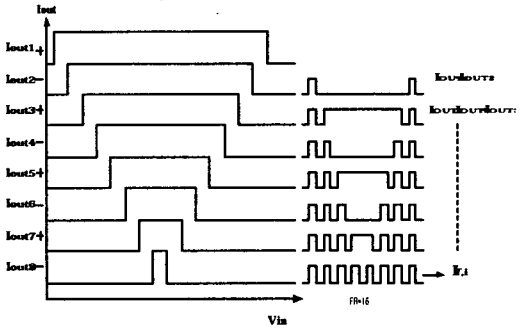

Fig. 5. Procedure to generate a folding signal, $I_{f,i}$ with FR=16.

This procedure can be also described by:

$$I_{f,i} = \sum_{K=1}^{4} I_{OUT,2K-1} + \sum_{K=1}^{4} \overline{I}_{OUT,2K} \qquad (3)$$

where $I_{OUT,2K-1}$ and $I_{OUT,2K}$ are a folding current and

a differential folding current, respectively.
The interpolating rate of 8 can be achieved by the current-mode interpolating circuit presented in Fig.6 [6] ~[8].

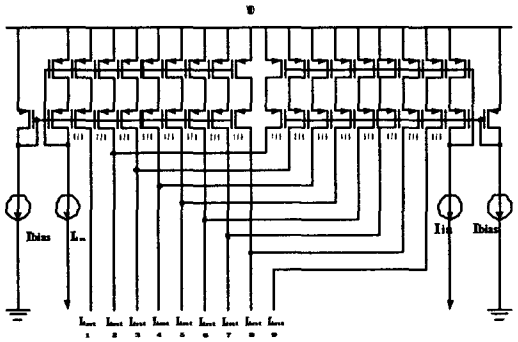

Fig. 6. Circuit diagram of the current-mode interpolating circuit.

The interpolating current signals between K^{th} and $K+1^{th}$ folding blocks can be obtained by:
The interpolating current signals are fed into the

$$I_{INTi} = \frac{\lfloor (IR-i)\cdot I_{f,k} + i \cdot I_{f,k+1} \rfloor}{IR}, i = 0,1,2,\cdots,IR \qquad (4)$$

64 current comparators to generate the 1024 circular coded voltage signals. In the current comparator circuit employed in the folding-interpolation ADC, Transmission gates are inserted in inverter chain for latching to synchronize the input of current subtraction amplifier. To decrease glitch in transmission gates and buffer to other module, NAND latch is used in the comparators. The digital encoder finally converts the 1024 circular codes into the 10 bit binary codes. The proposed ADC with a single supply of 3.3V has been simulated by HSPICE. Fig. 7 illustrates the simulated waveform of the eight folding current signals from the arithmetic current mirror. The resultant simulated folding signal with FR of 16 and folding signals from 9 AFB are demonstrated in Fig. 8 and Fig. 9, respectively. The interpolating current signals with IR=8 are simulated and presented in Fig. 10.

III. SIMULATION RESULTS

The proposed ADC designed in the 0.6μm n-well CMOS double-poly double-metal technology with single 3.3V supply has been simulated with HSPICE. The successive procedure of generating folding signal(FR=16) by ACM is illustrated in Fig. 7 and Fig. 8. The Figure 9 shows a plot of folding signals from the 9AFBs. Also shown are used in obtaining the interpolating current signals from folding blocks in Fig. 10.

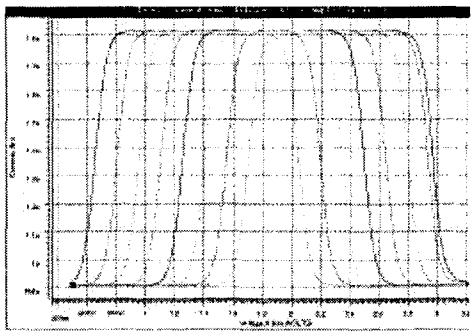

Fig. 7. Plot of the eight simulated folding signals from ACM (FR=2).

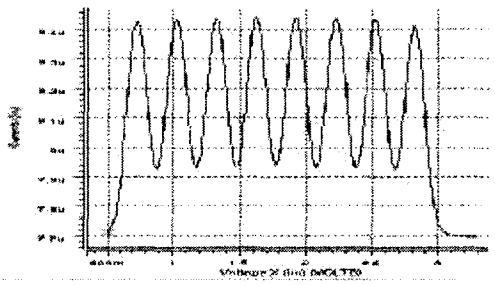

Fig. 8. Plot of the simulated folding signals, $I_{f,1}$ with FR of 16.

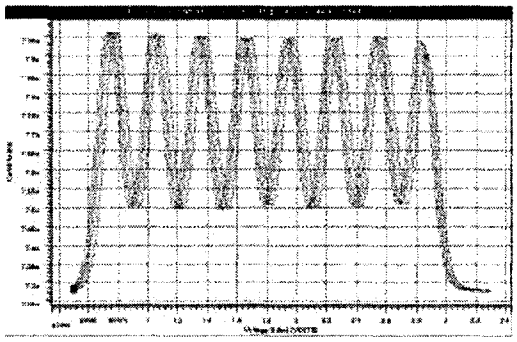

Fig. 9. Plot of the simulated folding signals from 9 AFBs.

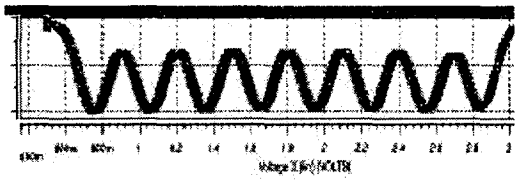

Fig. 10. Plot of the simulated 10bit folding and interpolating signals.

IV. CONCLUSION

The proposed 10-bit 3.3v Nyquist ADC is expected for a high speed and a low power

operation with using the current-mode folding interpolation, the current comparators, and the digital encoder. Furthermore, it has been focused on high folding factor and a small number of current reference sources by arithmetic approach in folding systems. Table 1 summarizes the simulated performance of the proposed 10bit ADC. The designed 10bit Nyquist current-mode ADC is expected to be suitable for an application of low power portable devices such as digital camcorderor or IF and baseband communication module in front-end block for SDR(Software Defined Radio)

Table. 1 *Summary of the simulation results*

Resolution	10 bit
Maximum Sample Rate	20 MSamples/s
DNL	≤± 0.5LSB
INL	≤± 1.0LSB
Power dissipation	150mW
Supply voltage	+ 3.3V
Technology	0.6um CMOS n-well

ACKNOWLEDGEMENT

This research was supported by the grant of KOSEF (contract No: 1999-2-302-002-3).

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