CMOS-IC Implementation of a Pulse-type Hardware Neuron Model with Bipolar Transistors

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Abstract: A number of studies have recently been made on hardware for a biological neuron for application with information processing functions of neural networks. We have been trying to produce hardware from the viewpoint that development of a new hardware neuron model is one of the important problems in the study of neural networks. In this paper, we first discuss the circuit structure of a pulse-type hardware neuron model with the enhancement-mode MOSFETs (E-MOSFETs). And we construct a pulse-type hardware neuron model using E-MOSFETs. As a result, it is shown that our proposed new model can exhibit firing phenomena even if the power supply voltage becomes less than 1.5[V]. So it is verified that our model is profitable for IC.

1.Introduction

A number of studies have recently been made on various neuron models and neural networks for application of the information processing functions of living organisms to engineering problems [1]-[3].

In physiology, the real nervous systems have transmitted the nerve impulses, which were generated by firing of excitatory nerve membrane. And the nerve membrane can be considered as a transformer of the impulse series. Therefore, it is important to know the characteristics of the impulse series in the nerve membrane, in order to clarify the information processing functions in the nervous systems. Accordingly, there are many studies for pulse-type hardware neuron models and artificial neural networks with the pulse-type hardware neuron model, which simulate the characteristics of the impulse series. We have been studying to construct hardware of the asynchronous neural network with the pulse-type hardware neuron models. When a hardware realization of the neural network is considered, the circuit structure tends to become complex. So we believe that it is necessary to design for IC of neuron models.

Recently, the pulse-type hardware neuron models, in which the circuit structure is relatively simple, have been composed of bipolar transistors [4], or have been composed of depletion-mode MOSFETs [5]. The pulse-type hardware neuron models with bipolar transistors are composed of negative resistor, equivalent inductor, membrane capacitor and membrane leak resistor. And also, one is parallel with the others.

In this paper, we first discuss the fundamental construction with the enhancement-mode MOSFETs (E-MOSFETs) of the equivalent inductance circuit and the negative resistance circuit. Next, we propose the pulse-type hardware neuron model with E-MOSFETs, which are able to use for IC, and we clarify the characteristics of the proposed model.

2. The pulse-type hardware neuron model

Figure 1 shows the fundamental circuit diagram of the pulse-type hardware neuron model with bipolar transistors. The model is composed of a negative resistance section (section A), an equivalent inductance section (section B), a membrane capacitor C_M and a membrane leak resistor R_L. The model can produce a pulse, so the model exhibits firing phenomena.

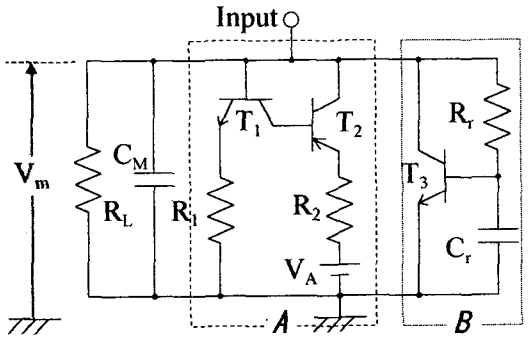


Figure 1: The pulse-type hardware neuron model with bipolar transistors.

At first, we discuss an equivalent inductance circuit. Figure 2 shows the fundamental circuit diagram of the equivalent inductance that is composed by two E-MOSFETs and C_{rL}. Figures 3 and 4 show the phase difference ϕ =arg V_{AL}/I_{AL} for the value of input frequency f_{AL}, which is changed from 0.1[MHz] to 100[MHz]. In this case, C_{rL} is 1.0[pF], and the ratio $(W/L)_n$ of n-channel E-MOSFET M_n is 10 and $(W/L)_p$ of M_p is 0.6, where W is the gate width and L is the gate length. $V_{AL}(=V_{ALD}+v_{ALA})$ is the voltage of the input A-B, V_{ALD} is input DC component of V_{AL}, v_{ALA} is input AC component of V_{AL} and input signal is sinusoidal. Figure 3 shows an example of ϕ for changing the value of f_{AL} with V_{ALD} as a parameter. v_{ALA}=0.5[V]. The marks ●,□ and ▲ are respectively the values of V_{ALD} as 1.0[V], 2.0[V] and 3.0[V]. Figure 4 shows an example of ϕ for changing f_{AL} with v_{ALA} as a parameter. V_{ALD}=2.0[V]. The marks ●,□ and ▲ are respectively the values of v_{ALA} as 0.5[V], 1.0[V] and 2.0[V]. These results show that the equivalent inductance circuit can be obtained the phase difference.

Next, we discuss the negative resistance circuit by using three E-MOSFETs (M_1, M_2 and M_3). Figure 5 shows the fundamental circuit diagram of the negative resistance circuit. This circuit added M_3 in order to bias between gate terminal and source terminal of M_2.

Figure 6 shows an example of the negative resistance characteristics for changing V_A as a parameter. This figure shows input current I_{in} for changing the value of increasing DC voltage V_{in} in case of instituting V_A from 1.5[V] to 2.5[V] at intervals of 0.5[V]. On the basis of this result, our composed negative resistance circuit can obtain the negative resistance characteristic at the power supply voltage 1.5[V], although the minimum current of the negative resistance characteristic becomes bigger and the voltage range of the negative resistance area becomes narrower. That is to say, our composed negative resistance circuit has the possibility of constructing the neuron model with the low power supply voltage.

Figure 7 shows an example of the I_{in}-V_{in} characteristics. In the figure, W/L of one of E-MOSFETs in Fig. 5 is changed with 5, 10, 20, 30 and 40 provided that W/L of the other E-MOSFETs are 10 and the value of the power supply voltage V_A=1.5[V].

Figure 7-(a) is an example of the I_{in}-V_{in} characteristics as a parameter with the ratio $(W/L)_1$ of M_1. In the figure, as $(W/L)_1$ becomes smaller, the minimum value of the negative resistance and the minimum current become bigger. And, as $(W/L)_1$ changes smaller, the voltage range of the negative resistance area becomes wider. Figure 7-(b) is an

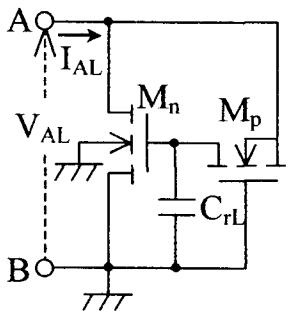


Figure 2: The equivalent inductance circuit.

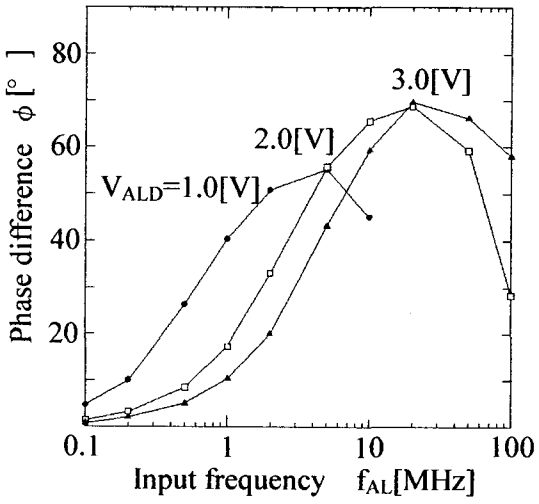


Figure 3: The ϕ -f_{AL} characteristics (V_{ALD} as a parameter).

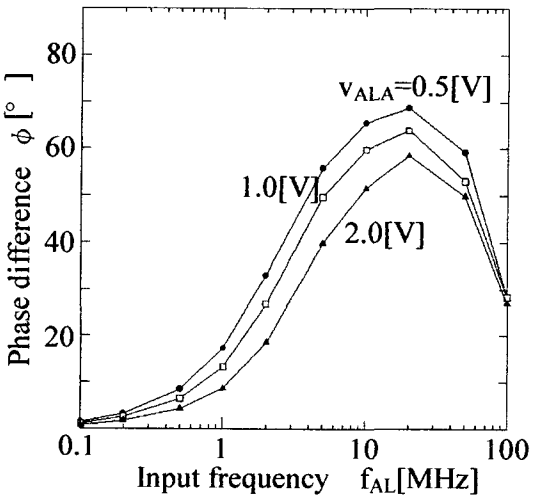


Figure 4: The ϕ -f_{AL} characteristics (v_{ALA} as a parameter).

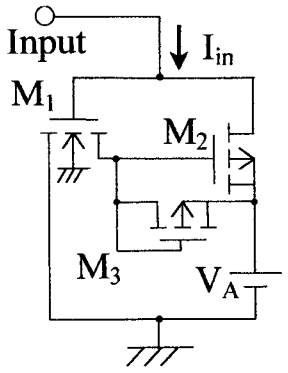


Figure 5: The negative resistance circuit.

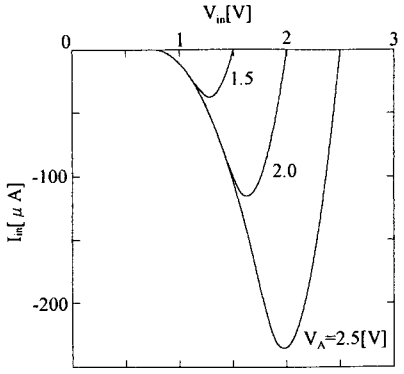
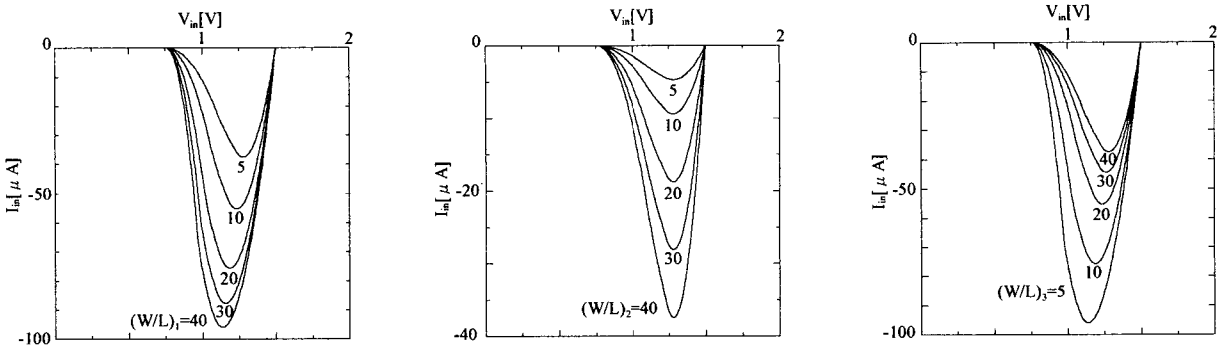


Figure 6: The negative resistance characteristics (V_A as a parameter).



(a) $(W/L)_1$ (b) $(W/L)_2$ (c) $(W/L)_3$

Figure 7: The I_{in}-V_{in} characteristics.

example of the I_{in}-V_{in} characteristics, with the ratio $(W/L)_2$ of M_2 as a parameter. In the figure, as $(W/L)_2$ changes bigger, the voltage range of the negative resistance area is not change. And as $(W/L)_2$ becomes bigger, the minimum value of the negative resistance and the minimum current become smaller. Figure 7-(c) is an example of the I_{in}-V_{in} characteristics, with the ratio $(W/L)_3$ of M_3 as a parameter. In the figure, as $(W/L)_3$ changes bigger, the minimum value of the negative resistance and the minimum current become bigger, and the voltage range of the negative resistance area becomes wider. These results mean that by choosing W/L of each E-MOSFET of the negative resistance circuit, we can decide the voltage range of the negative resistance area.

On the basis of the above results, we discuss about to implementation the new neuron model that consists of the negative resistance part and the equivalent inductance part that used E-MOSFETs. Figure 8 shows the fundamental circuit diagram of the proposed new pulse-type hardware neuron model. The model is composed of negative resistance circuit,

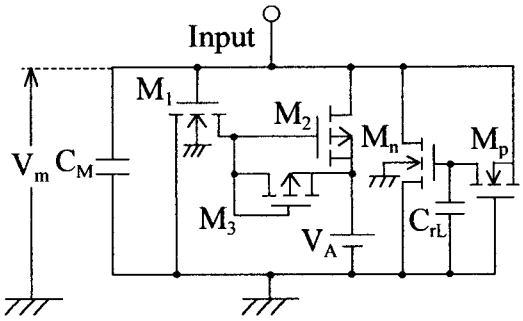


Figure 8: The proposed new pulse-type hardware neuron model.

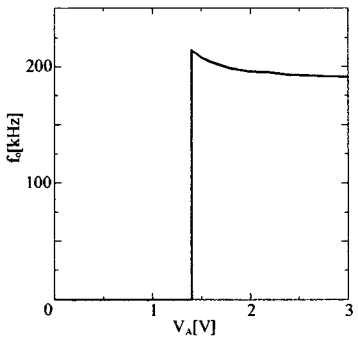


Figure 9: The f_o-V_A characteristic.

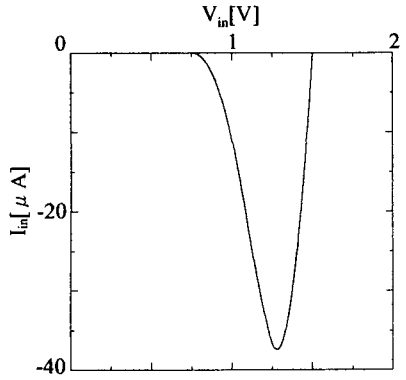


Figure 10: The I_{in}-V_{in} characteristic.

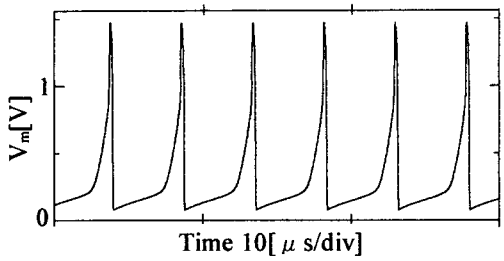


Figure 11: Firing waveform.

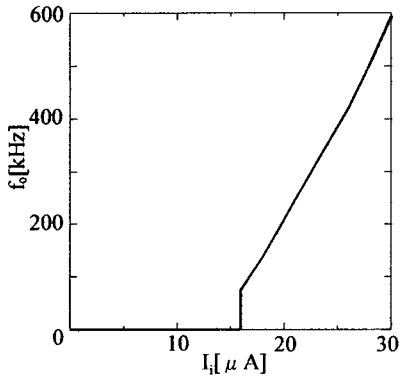


Figure 12: The f_o-I_i characteristic.

equivalent inductance circuit and membrane capacitor.

Figure 9 shows an example of the output frequency f_o when the power supply voltage V_A changes from 0[V] to 3[V]. In this investigation, on the basis of the result of Fig. 7, $(W/L)_{1\text{-}3}$ of each E-MOSFETs (M_1-M_3) are selected as the negative resistance area becomes as wide as possible. Concretely, the value of $(W/L)_1$=5, $(W/L)_2$=40, $(W/L)_3$=40, $(W/L)_4$=0.6, $(W/L)_5$=10, the capacitor of C_r=1[pF], C_M=2[pF], and the input current from the Input terminal I_i=20[μ A]. The figure shows that this model can exhibit firing phenomena when V_A is over 1.4[V].

Figures 10-12 show the simulation results, provided that V_A=1.5[V], and $(W/L)_1$-$(W/L)_5$ are same values with Fig. 9. Figure 10 is an example of the I_{in}-V_{in} characteristics of Fig. 5. The figure shows that negative resistance area can be obtained in the ranges of V_{in}=1.25[V]-0.75[V]. Figure 11 is an example of V_m provided that the input current from the input terminal I_i=20[μ A] in Fig. 8. The figure shows that the firing phenomena can be obtained by using our model. Figure 12 is an example of the firing characteristics when the input current from the input terminal changes 0-30[μ A] in Fig. 8. In the figure, f_o means the frequency of the output voltage V_m. The figure shows that the proposed model can be obtained the firing phenomena more than I_i=16[μ A].

3.Conclusions

We discussed the new pulse-type hardware neuron model with E-MOSFETs. And we clarified the characteristics of the model. As a result, it was shown that our proposed new pulse-type hardware neuron model exhibited firing phenomena even if the power supply voltage becomes less than 1.5[V]. So it is verified that our proposed neuron model is profitable for IC.

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