A Switched-Capacitor Interface for Differential Capacitance Transducers

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Abstract: For high-accuracy signal processing of differential capacitance transducers, an interface circuitry based on a switched-capacitor sample/hold circuit is developed. Driven by nonoverlapping two-phase clocks, the interface produces the output voltage which is proportional to the ratio of difference-to-sum of two capacitors of a differential transducer. Performances of a prototype chip fabricated using 0.6 μm n-well CMOS process were measured and compared with those simulated by HSPICE. The measured results indicate that 0.1% resolution is achievable with the proposed interface and the temperature-dependence of the interface is small enough for practical applications.

I. Introduction

A differential capacitance transducer consisting of two capacitors is widely used to detect such physical quantities as pressure difference, linear displacement, acceleration, and rotational angle [1]. Its electrical equivalent is shown in Fig. 1, where C_a and C_b are two capacitors which change complementarily with a measurand. In a rotational angle encorder, C_a and C_b change linearly with the angle x. In pressure transducers, on the other hand, C_a and C_b change hyperbolically with applied pressure x [2]. In either case, the measurand x can be extracted independently of the total capacitance by the following ratiometric operation:

$$x = \frac{C_a - C_b}{C_a + C_b} . \qquad (1)$$

Besides the linear extraction of a measurand x, the ratiometric operation has another distinct feature that capacitance changes due to temperature which would otherwise be a major error source are cancelled and have no effect on the accuracy if signal processing is insensitive to parasitic capacitances C_{pa}, C_{pb}, and C_{pc}.

The ratiometric operation can easily be performed by an analog-to-digital (A/D) converter with the reference being an electrical variable proportional to C_a+C_b. Such methods using a charge-balancing [3], oversampling ΔΣ modulating [4], [5], or successive-approximation [6] A/D converter provide the digital equivalent of a measurand. The other methods use the relaxation oscillator consisting of an integrator and a comparator [7], [8]. These digital methods are suited for co-integration with micromachined transducers, but are limited to low-speed applications.

For high-speed ratiometric signal processing, analog interfaces based on the current detection [9]-[12] and the charge amplifier [13] have been proposed. These interfaces allows a signal processing speed up to 10^5 sps (sample per second), but their CMOS realization is difficult.

A CMOS interface for high-speed ratiometric operation is highly requested by micromachined differential capacitance transducers for acceleration and rotary angle measurements. To respond the request, an interface is developed based on a switched-capacitor (SC) sample/hold (S/H) circuit. This paper describes its configuration and performances simulated by HSPICE and obtained in the prototype chip integrated by a 0.6 μm n-well CMOS process.

II. Interface Circuit

Fig. 2 shows the circuit diagram of the interface for ratiometric signal processing of differential capacitance transducers. It is basically a SC S/H circuit with two transducer capacitances C_a and C_b being S/H capacitors. Capacitor C_h is an additional hold capacitor to mitigate the slew rate requirement of op-amp A [14]. If the op-amp is ideal, C_a is charged to (V_{r1} - V_b) and C_b to (V_{r2} - V_b) in the ϕ phase. In the $\bar{\phi}$ phase, two capacitors are connected in parallel, to produce the output voltage $V_o(\bar{\phi})$:

$$V_o(\bar{\phi}) = V_b + \frac{C_a(V_{r1} - V_b) + C_b(V_{r2} - V_b)}{C_a + C_b}$$

$$= \frac{C_a V_{r1} + C_b V_{r2}}{C_a + C_b} . \qquad (2)$$

If V_{r1} and V_{r2} are set to

$$V_{r1} = \frac{V_{DD}}{2} + V_r , \qquad (3)$$

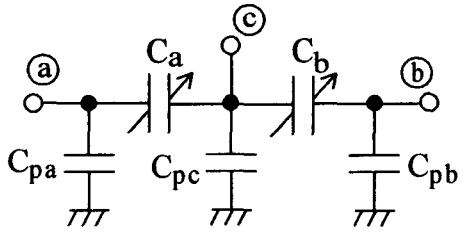


Fig. 1. An equivalent circuit of a differential capacitance transducer.

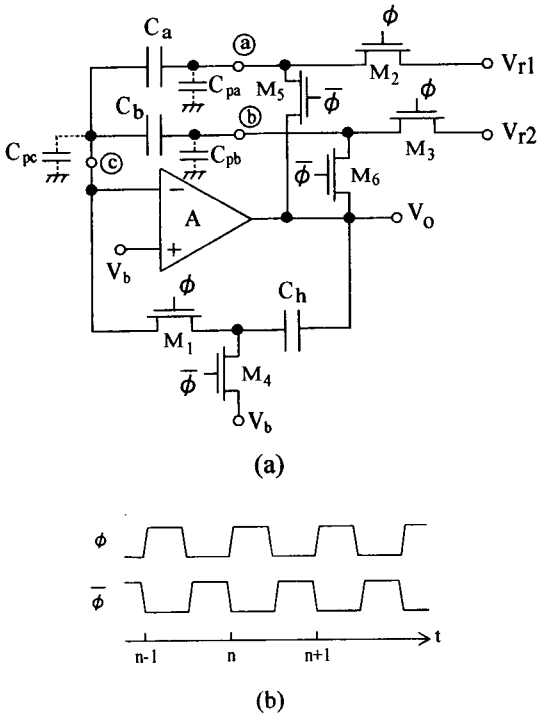


Fig. 2. (a) Circuit diagram of the interface.
(b) Timing diagram of the nonoverlapping two-phase clocks.

and

$$V_{r2} = \frac{V_{DD}}{2} - V_r, \tag{4}$$

then $V_o(\bar{\phi})$ is given by

$$V_o(\bar{\phi}) = \frac{V_{DD}}{2} + xV_r. \tag{5}$$

Parasitic capacitances have no effect on the ratiometric operation (5). This also holds true of the hold capacitor C_h because it merely provides the feedback path in the ϕ phase.

Error sources involved in the interface are the finite gain and the offset voltage of an op-amp and the charge injection from switches. It is described in [15] that the error voltage due to the finite gain of the op-amp which is stored into C_a and C_b in the ϕ phase compensates the corresponding output error in the $\bar{\phi}$ phase, thereby making the ratiometric operation insensitive to the finite gain. The offset voltage of the op-amp in the $\bar{\phi}$ phase is also compensated by that stored into C_a and C_b in the ϕ phase. Therefore, no special design strategy is required for the op-amp.

The error voltage $\delta V_o(\bar{\phi})$ due to charge injection is given by, to first order [15],

$$\delta V_o(\bar{\phi}) = \frac{q_{CH,total} + q_{CL,total}}{C_o} - \frac{2C_{OL}}{C_o^2(1-x^2)} \cdot q_{CL,total}, \tag{6}$$

where $q_{CH,total} = q_{CH1} + q_{CH2} + q_{CH3}$, (7)

and $q_{CL,total} = q_{CL1} + q_{CL2} + q_{CLH3}$, (8)

and q_{CHi} and q_{CLi} are the channel charge and the clock-feedthrough injected to C_a and C_b from switch M_i (i=1, 2, 3), respectively, and C_{OL} is the overlap capacitance. The first term in (6) represents the offset error which can be nullified by the offset adjustment. The second term is the nonlinear error that limits the ultimate accuracy. Specifically, $q_{CL,total}$ is of the order of 1 pQ and C_{OL} is typically 20 fF. Assuming C_0 = 5 pF, then the nonlinear error amounts to 2 mV. Reducing the clock-feedthrough component by the use of small-dimensioned switches with the dummy compensation is crucial for high-accuracy signal processing. Reducing the gate aspect ratio, however, increases the on resistance of a switch and thereby decreases the operational speed. Therefore, the switch should be designed based on the compromise between the accuracy and the speed.

III. Performances simulated by HSPICE

Performances expected from CMOS realization are simulated by HSPICE. A simple two-stage CMOS op-amp consisting of a differential pair followed by a rail-to-rail output stage is designed for low voltage and low power operation. Fig. 3 shows performances of the op-amp. The dc gain is typically 84 dB and the dominant pole is located at 30 Hz. Performances of the interface using this op-amp and switches with the aspect ratio W/L_{PMOS}=13.0 μm/0.9 μm, W/L_{NMOS}=4.0 μm/0.9 μm are shown in Fig. 4. These performances are quite similar to those assuming an ideal op-amp. This confirms the theoretical analysis described in the previous section that the ratiometric operation is insensitive to nonideal performances of an op-amp. Error

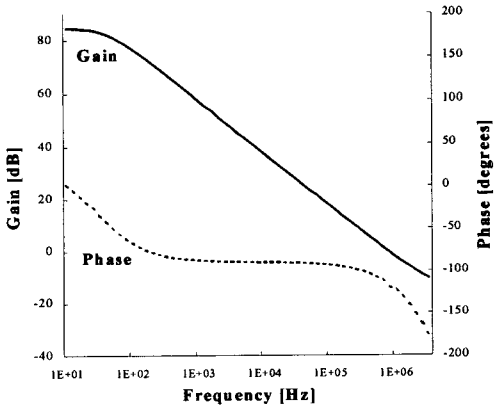
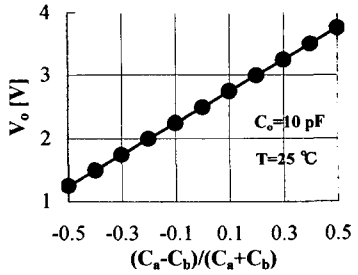
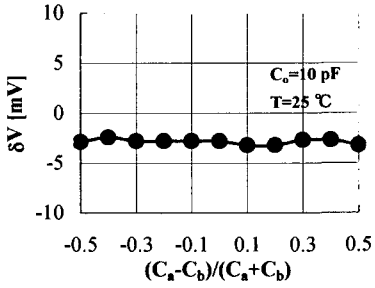


Fig. 3. Op-amp Performances.

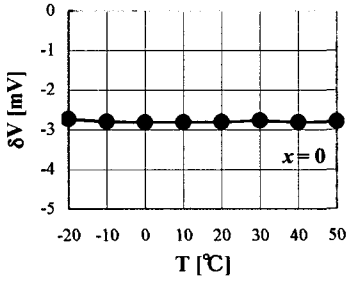


(a)

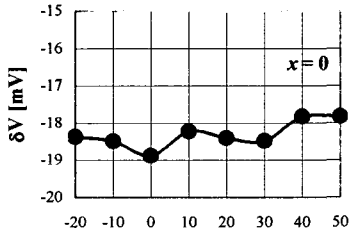


(b)

Fig. 4. Simulated performances: Output voltage (a) and the deviation from the ideal value (b) as a function of capacitance difference-to-sum ratio.
A two-stage op-amp and switches with the aspect ratio W/L_{PMOS}=13.0 μm/0.9 μm, W/L_{NMOS}=4.0 μm/0.9 μm are assumed.



(a)



(b)

Fig. 5. Error voltage as a function of temperature.
(a) W/L_{PMOS}=13.0 μm/0.9 μm, W/L_{NMOS}=4.0 μm/0.9 μm,
(b) W/L_{PMOS}=65.0 μm/1.2 μm, W/L_{NMOS}=20.0 μm/1.2 μm

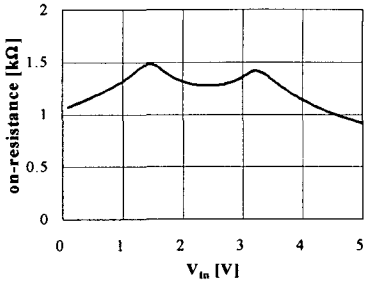


Fig. 6. The on-resistance of the switch.

voltages as a function of temperature when switch dimensions are W/L_{PMOS}=13.0 μm/0.9 μm, W/L_{NMOS}=4.0 μm/0.9 μm and W/L_{PMOS}=65.0 μm/1.2 μm, W/L_{NMOS}=20.0 μm/1.2 μm are compared in Fig. 5. The comparison demonstrates that the charge injection is dependent on temperature, and reducing the charge injection is critical to high-accuracy processing.

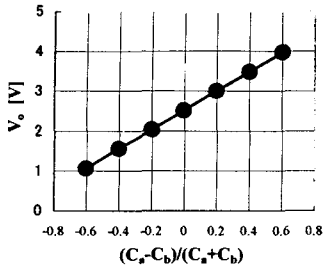
Fig. 6 shows the on-resistance of the switch as a function of the input voltage. The on-resistance of the switch is 1.5 kΩ at maximum. Assuming C_o = 50 pF, the 0.1% settling time is 520 ns. This implies that the clock signal as high as 0.96 MHz is allowed to drive switches. Inferring from the op-amp performances, however, the clock frequency will be limited to 500 kHz in practice. Much higher sampling rate is possible by increasing the power consumption of the op-amp.

IV. Performances of Prototype Chip

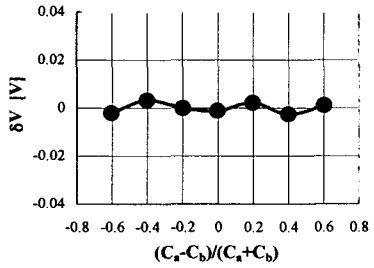
The interface of Fig. 2 was integrated using 0.6 μm n-well CMOS process. The op-amp described in the previous section and CMOS switches with the aspect ratio W/L_{PMOS} = 13.0 μm/0.9 μm, W/L_{NMOS} = 4.0 μm/0.9 μm are used for implementation of the interface. The nonoverlapping two-phase clocks are generated in the internal clock circuit. To evaluate performance of the chip, pairs of mica capacitors with the total capacitor C_o being 50 pF were used in place of a transducer. The power supply voltage V_{DD} is 5 V. The clock frequency is 100 kHz. The reference voltages V_{r1} and V_{r2} are 5 V and 0 V, respectively.

Typical measurement results are shown in Fig. 7. The output voltage plotted in Fig. 7 (a) is proportional to the difference-to-sum ratio of two capacitors, confirming the ratiometric operation given by (5). Deviations from the ideal values, plotted in Fig. 7 (b), are appreciable. The residual nonlinear error is of the order of a few mV. These results indicate that 0.1% resolution is achievable with the proposed interface.

Fig. 8 shows error voltage as a function of temperature when $x=0$. This result shows that the temperature variation is smaller than 0.002%/℃.



(a)



(b)

Fig. 7. Performances of a prototype chip:
Output voltage (a) and the deviation from the ideal value (b) as a function of capacitance difference-to-sum ratio.

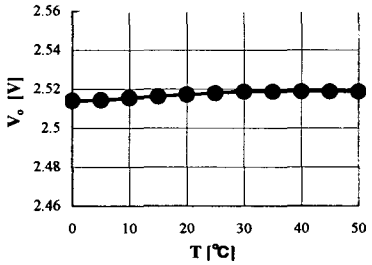


Fig. 8. Error voltage as a function of temperature of the prototype chip.

V. Conclusions

A CMOS interface of differential capacitance transducers has been described which performs the ratiometric operation with the simple configuration. Performances simulated by HSPICE and those of the prototype chip integrated by 0.6 μm n-well CMOS process were evaluated. The measurement results indicate that 0.1% resolution is achievable with the proposed interface and higher accuracy will be obtained by using the dummy-compensated switches with small gate areas.

Owing to a high resolution and the small temperature-dependence, this interface chip will find wide applicability in laser scanners and accelerometers.

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