Design of Modified Banyan Switch for High Speed Communication Network

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Abstract

In this paper, we propose and design new architecture of the modified Banyan switch for a high speed networking and the high speed parallel computer. The proposed switching network with a remodeled architecture is a newly modified Banyan network with eight input and output ports. The switch scheme is that two packets may arrive on different inputs destined for the same output.

We have analyzed the maximum throughput of the revised switch. The result of the analyses shows good agreement simulation and if we adopt such architecture of the revised model of the Banyan switch, the hardware complexity can be reduced. The FIFO discipline has increased about 11% when we compare the switching system with the input buffer system. We have designed and verified the switching system in VHDL .

1. Introduction

A complex network and a parallel computer are made up of interconnected switching units. The role of a switching unit is to set up a connection between an input port and an output port, according to the routing information.

In the Banyan switch, the switch complexity has been reduced more than in the crossbar switch. But in case of the Banyan switch, there occur internal blocking and structural blocking when a couple of packets with the same clock are being sent from the input ports to the output ports [1],[2],[3].

This paper develops an efficient buffer management scheme that makes the ATM switch be capable of supporting the delay sensitivity as well as the loss sensitivity of the packets. The proposed scheme aims at enhancing the performance of the ATM switches by modifying the Banyan switch network with an input and an output buffers.

We have proposed a switching network with a remodeled architecture. It is the modified Banyan network with eight input and output ports. The switch scheme is that two packets may arrive on different inputs destined for the same output. The switch architecture may allow one of these packets to pass through to the output, but the others must stay in the buffer for later transmission.

We have analyzed the maximum throughput of the revised switch. Our analyses have shown that under the uniform random traffic load, the FIFO discipline is limited to 58.6% in the input buffer system [2]. The switch performance increased by about 11% when we compare the switching system with the input buffer system. The switching system consists of an input control unit and a switch unit with an output control unit.

We have design the switching system by way of Max+pluse II . We have also design our test environment including microcomputers, the base station, and the proposed architecture.

The rest of the paper is as follows: In Section 2. Switch architecture and operation, In Section 3. Architecture design of switch, In Section 4. Performance, and In Section 5. Conclusions.

2. Switch Architecture and Operation

The modified Banyan switching networks consists of switch cells with 2× 2 switch elements, where each input port is the root of a tree that branches over a number of intermediate switching elements with output ports.

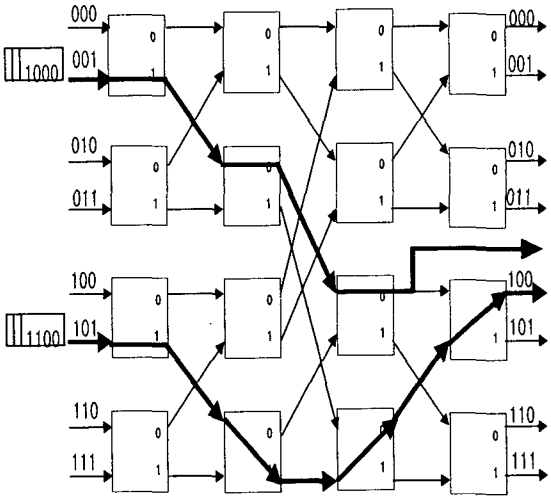


Figure 1. The modified Banyan network

An overview of the Banyan switch architecture with N=8 inputs and eight outputs is given as in Figure 1. There exist two paths connecting input ports to an output port. Furthermore, the networks are self-routing switches [3].

2.1 Packet and Switch Element

The switch network is used to route serial data streams in a packet format. Figure 2 illustrates the structure of packet and switching element. Each packet is divided into the header and the data section; the header contains the address to which the packet is routed; the address bits are ordered by most significant bit(MSB) to least significant bit (LSB).

A packet is self-routing if the header of the packet contains all the information needed to route through a switching network. This means that the switch nodes set themselves by reading the headers

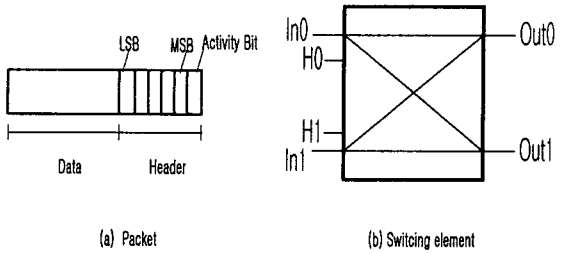


Figure 2. Packet and Switching Element

Each packet header consists of 5 bits which contain self-routing addresses. The packet is activated when the activity bit of the packet is 1, but inactivated when it is 0.

2.2 Operation of the Switching Network

A switching element is the basic unit of a switch fabric. Figure. 2 (b) gives the detail of the basic 2-input, 2-output switching element.

The packet input network performs the simultaneous insertion of up to 8 received packets from the input controller. Buffer insertion requires two steps, address generation and simultaneous access. After address generation, simultaneous access of out buffer is required and is provided pass to modified Banyan network. Each packets input to out buffer must receive a unique address in the output port. Addresses must be change self-routing header. For 8 inputs and 8 output, addressed 0 to 7, the stage of 2 × 2 switching elements. The switch element(SW) with two data inputs of In0, In1 and two control inputs of H0, H1. The control inputs select which one of the data inputs is switched to the output. A two-function switch box can assumed either the straight or cross state.

The control inputs select which one of the data inputs is switched to the output. A two function switch box can assumed either the straight or exchange state. Consider the 2 by 2 crossbar switch shown in Figure 2(b). This 2 by 2 switch the capability of connecting the input In0 to output labeled 0 or the output labeled 1, depending on the value of some control bit H0=0 of the input In0 input In0. If H0, the input is connected to the upper output, and if H0=1, the connection is made to the lower output. Terminal In1 of the switch behaves similarly with a control bit H1.

3. Architecture design of switch

In this chapter we design of the proposed switch. As shown in Figure3 , the switch network consists of a input controller(IC), a switch network with a output controller(OC).

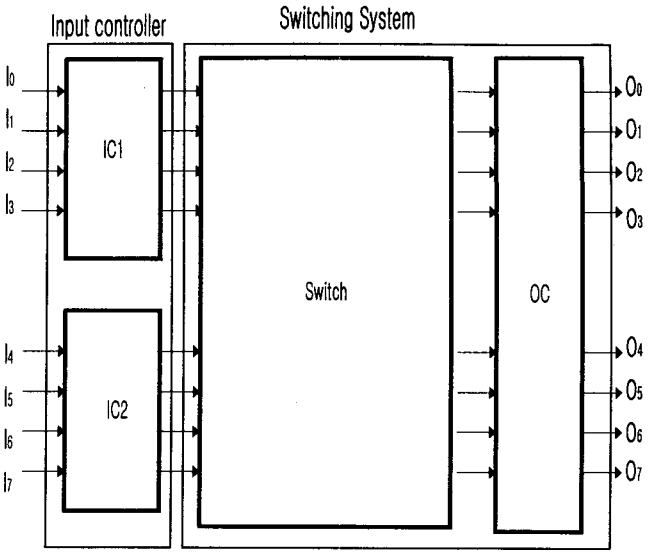


Figure 3. Block diagram of the modified Banyan switch

3.1 Input controller

Input controller are located at the input side of the switch. This part are address generation and simultaneous queue access. In this section we illustrate the design of a control circuit for input control. Figure 4 show the IC block diagram of our circuit. The circuits consist of packet register(PR) and header register(HR) which are used to hold the packet data and header data,

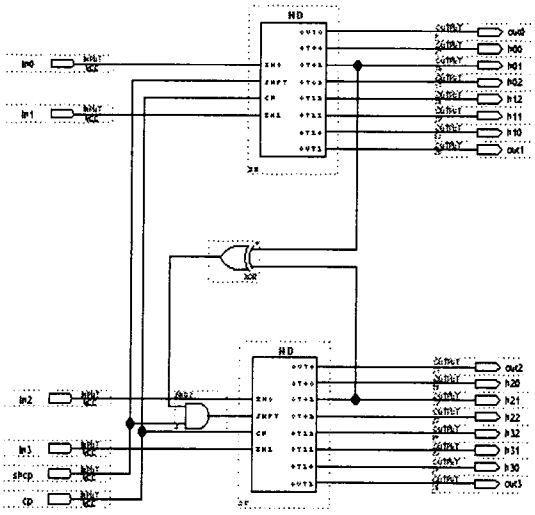


Figure 4. Input controller

respectively. The pack register serves as the FIFO. The header register is connected PR, move PR to HR for self-routing compare to MSB.

3.2 Switching system

A switching system consists of reverse Banyan switch and output controller. A switch of the architecture is reverse Banyan network with $O(\log_2 N)$ 2×2 switching elements, where N is number input/output ports, it is nonblocking switch [4]. Inside the switch, switching

nodes(SNs) are connected by internal links. A switching node in constructed with two selector. Bit clock signal is supplied to all the stages Figure 2 (b). A output controller consist of switch(switcho) and buffer(otsi10) as shown

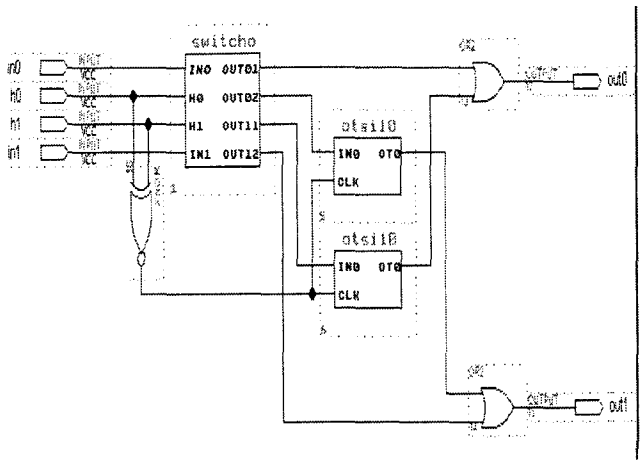


Figure 5. Out controller

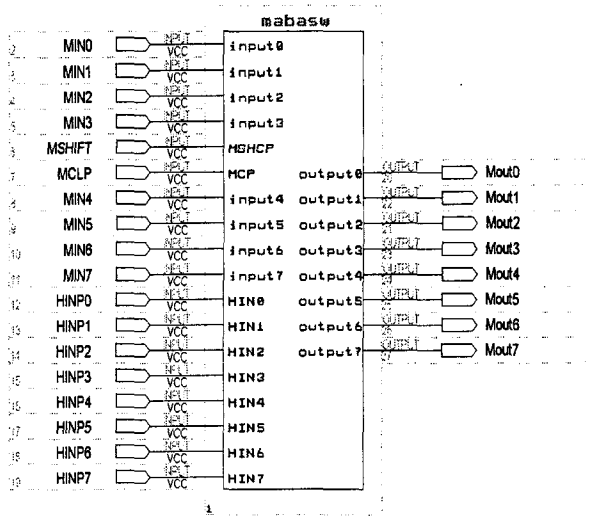
figure 5. The operation of OC is follows. A buffers are used to hold one packets when two arrived on one port.

3. 3 Simulation

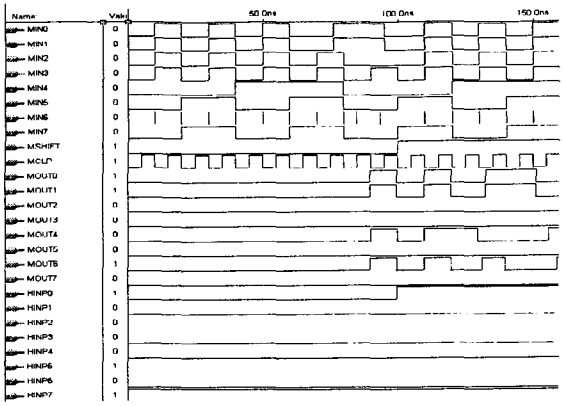
The proposed switch was designed and verified using VHDL. Figure 6 show the simulation environment for the proposed switch.

Banyan networks are described by tree character features: the switch box, the network topology, and the control structure. In this paper we design the proposed switch. As shown in Figure 6, Schematic and time diagram of Banyan switch [5].

We designed the circuit by using VHDL. First, we evaluated what and how many fundamental design resources are required, IC, Switch, OC, and how many operation cycles are needed to process each algorithm.



(a) Schematic



(b) Time diagram

Figure 6. Schematic and time diagram of the modified Banyan switch

Then, the components were coded in behavioral description way and built in a design library. Next, we decided how to connect those components for each algorithm

4. Performance

In this section we did analyses and compare of the maximum throughput of the switch. In the analyses, we made save approximations. However the results of the analyses show good agreement the simulation results.

We model the packet arrivals on the 8 input by independent. Each packet has equal probability 1/N of being addressed to any given output and successive packets are independent [6]. For small value of N, a Markov chain analysis of the system throughput can be done, yielding the results given in TableI [7].

The maximum throughput achievable with input Queueing for various switch size N and a number of packets W.

TableI. The maximum throughput achievable

N / W	2	4	8	16	32	64	128
1	0.75	0.66	0.62	0.60	0.59	0.59	0.59
2	0.84	0.76	0.72	0.71	0.70	0.70	0.70

Show the maximum throughput achievable for various switch and number of packets (N and W).

The values we obtained by simulation. Note that a increase in the achievable is possible by increasing the number of cell w from W=1 to W=2.

5. Conclusions

We designed the modified Banyan switch for BISDN networked and parallel computer. In our proposed

architecture exist two path input ports to out ports

We analyzed the maximum throughput of under the uniform random traffic load, the FIFO discipline is limited to 72% [8].

And the results of the analyses show good agreement the simulation results and reduce to the hardware complexity.

Our Proposed architecture was designed and verified in VHDL. The FIFO discipline has increased about 11% when we compare the switching system with the input buffer system.

References

[1] L. R. Goke and G. j. Lipovski, "Banyan Networks for Partitioning Multiprocessor Systems", 1st Annual Int'1. Symp. Comp. Arch., Dec. 1973. pp. 21~28

[2] L. Kleinrock, *Queueing Systems, Vol. I: Theory, Wiley, 1975*

[3] Tony T. Lee, "Non-blocking Copy Networks for Multicast Packet Switching", Int'1 Zurich Seminar on Digital Communications, Mar. 1998.

[4] Manfred N. Huber, Erwin P. Rathgeb, Thomas H. Theimer, "Self routing banyan networks in an ATM-environment", Proceedings of ICCC 1998, pp. 167~174

[5] Raif O. Onvural, *Asynchronous Transfer Mode Networks: Performance Issues*, 2nd Edition, Artech House, 1995.

[6] M.J.Karol, M.G. hluchyj, and S.P. Morgan, "Input Versus Output Queing on a Space -division packet switch, " *IEEE* Trans. commun., vol. COM.35, pp.1347-1356, Dec. 1987.

[7] Michael G.Hluchyj, Mark J.Kayol, "Queueing in High-Performance Packet Switching,"*IEEE* J,select. Areas commun., vol. 6. No,9 pp.1587-1597. Dec. 1988.

[8] J.M.Pitts and J.A.Schormans, " Introduction to ATM Design and Performance", John Wiley & Sons, p.189, 1996.