VLSI Design Innovation in the Deep-Submicron Era

Masaharu Imai, Yoshinori Takeuchi
Dept. of Informatics and Mathematical Sciences
Graduate School of Engineering Science, Osaka University
1-3 Machikane-yama, Toyonaka, Osaka 560-8531 Japan
Tel: +81-6-6850-6625, Fax: +81-6-6850-6627

Abstract: This paper describes the innovation of VLSI design methodology in the coming decade. Technology trend of VLSI fabrication is surveyed first. Then the so-called "design crisis" is analyzed. Finally, possible design methodology to overcome the design crisis is discussed.
Keywords: VSLI design, deep submicron technology, design crisis, system level design methodology, HW/SW codesign

1. Background

According to the ITRS (International Technology Roadmap for Semiconductor) 1999 report, the design rule of VLSI in the 2010's will become smaller than 100 nm and the number of transistors fabricable on a chip will exceed 1G (10^9) [1]. Taking advantage of such DSM (Deep Sub-Micron) technology, very complex electronic systems can be implemented on a single small silicon chip, as an SoC (System on a Chip). Following components are expected to fabricate on an SoC, as shown in Fig. 1:

(1) Processor Cores and DSPs
(2) Memories (RAM and ROM)
(3) Peripherals
(4) FPGAs
(5) Analog Blocks
(6) RF (Radio Frequency) Blocks

Using such SoC, embedded systems with high performance but lower power consumption can be implemented, which is suitable ICT (Information and Communication Technologies) application systems.

2. Design Crisis

There are several technical issues to be resolved for designing such SoCs effectively. These issues can be better characterized by the term "Design Crisis," which implies following difficulties.

(1) Design description management:
The more components are contained in a design, the more amount of description is required to express the model of design and its implementation. Then the amount of design description will eventually exceed the limit that designers can manage.

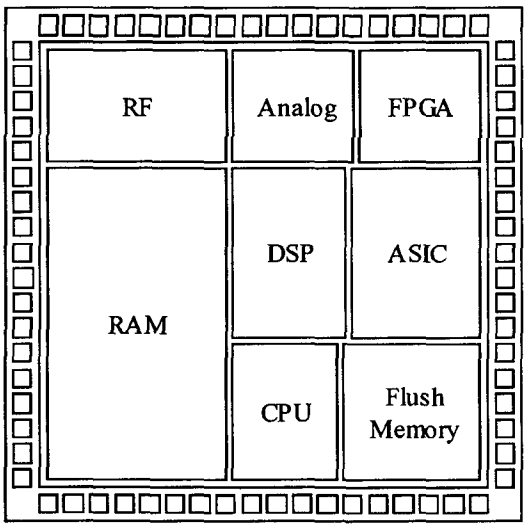

Figure 1 Possible Components in SoC

(2) Design verification/validation:
The longer and more complex the design becomes, it becomes more difficult to verify or to validate the design description. In other words, very long time and effort will be required to proof the correctness of the design.

(3) Design optimization:
The longer and more complex the design becomes, it becomes more difficult to optimize the design.

One of the reasons behind the difficulty in the design optimization is that most of the system level design optimization problems are combinational ones, and the inherent complexity of these problems is NP-hard. Another reason is that the delay and the power consumption by wire become much more complex models in the DSM technology than before. The transport delays by

wires are estimated as shown in Figure 2, which shows that the delay by a global wire will become dominant as the technology advances. Figure 3 shows a conventional and a new wire models to estimate the delay and power consumption. In the DSM, much more complex wire models than in the pre DSM technology should be used to obtain an accurate estimation results.

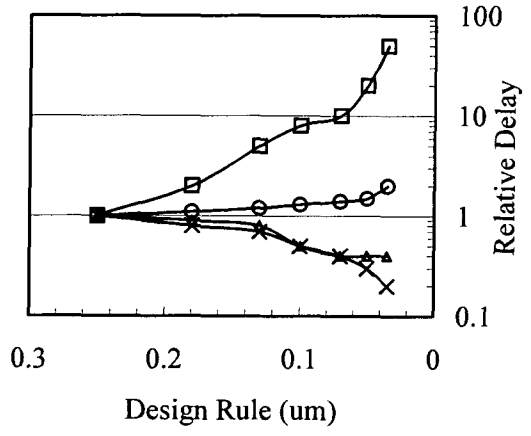

Figure 2 Relative Delay in DSM

(a) Conventional Wire Model

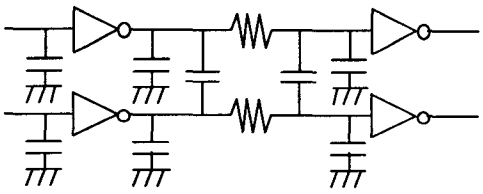

Figure 3 (b) New Wire Model for DSM

3. Requirements

In order to overcome the difficulties in the design of VLSI, we need new design methodologies that are fit for the DSM technology. The requirements to the design methodology can be summarized as follows:

(1) Complexity of design description should be reduced.
(2) Design verification can be performed easily.
(3) Design optimization can be performed in a short computation time.

4. Innovation

Following strategies will be effective to design SoCs using DSM technology.

(1) Perform system level design methodology:
To reduce the complexity of design description, the initial design description (specification of the design) should be higher enough in abstraction level.
(2) Separation and bridging of modeling and implementation descriptions:
Modeling and implementation descriptions should be separated to make it easy to verify the design. However, in order to guarantee the correctness of the implementation, these descriptions should be bridged as well.
(3) Accurate design quality estimation at a higher level of design description:
This is very important to reduce the effort to find an optimal design by avoiding unnecessary exploration of very broad design space of the design. Where design quality denotes such attributes of design as area, delay, and power consumption, of the component.

5. Conclusion

This paper outlines the future design methodology suitable to DSM technology. Proposed design methodology will reduce the design effort and will help designers to find an optimum design.

References

[1] SIA: International Technology Roadmap for Semiconductors, 1999