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A Single Transistor Type Ferroelectric Field-Effect-Transistor Cell Scheme

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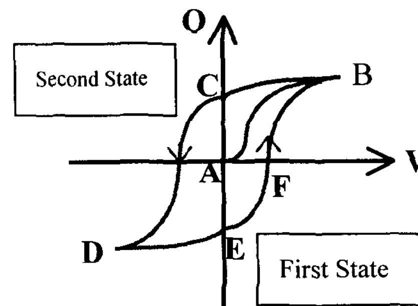
Abstract: This paper describes a single transistor type ferroelectric field effect transistor (1Tr FeFET) memory cell scheme, which select one unit memory cell and program/read it. The well voltage can be controlled by isolating the common row well lines. Through applying bias voltage to Gate and Well, respectively, we implement 1T FeFET memory cell scheme in which interference problem is not generated and the selection of each memory cell is possible. The results of HSPICE simulations showed the successful operations of the proposed cell scheme.

1. Introduction

Recently, ferroelectric devices based nonvolatile FRAMs have attracted considerable attention for nonvolatile memory devices, since they have not only nonvolatile characteristics but also low voltage operation.[1,2,3,4] There are reported two types of FRAMs which are one has DRAM-like 2T/2C or 1T/1C configurations [3,4] and the other is transistor-cell-type FRAMs[1,2]. A transistor-cell-type FRAMs can be achieved using the ferroelectric material as the gate oxide. Generally transistor-type FRAMs can be composed of Metal-Ferroelectric-Silicon (MFSFET), Metal-Ferroelectric-Insulator-Silicon(MFISFET) or Metal-Ferroelctric-Metal-Insulator-Silicon Field-Effect-Transistor (MFMISFET) structure. 1Tr FeFET stores data using hystersis characteristic between voltage and accumulated electric charge. Fig. 1 is a graph illustrating the hysteresis characteristic between voltage and electric charge of a normal ferroelectric device.



[Fig.1] Hystersis Characteristic charge .vs. Voltage

The 1Tr FeFET type memory has more merits than 1T/1C or 2T/2C. It can show non-destructive readout operations and a large remnant polarization (Pr) is not required. Also, It takes advantage of chip integrity. But, despite their many advantages in, it is very difficult to fabricate the transistor-cell-type FRAMs which could generate interference phenomena in read/write operations [1,2].

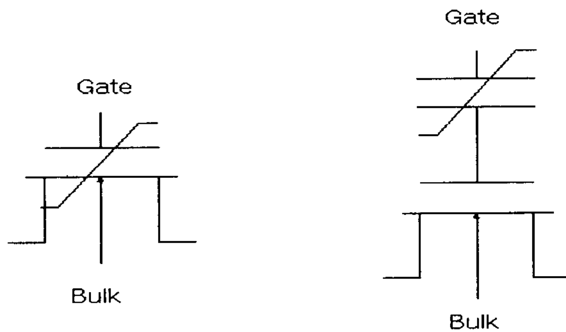
We proposed a single transistor type FeFET memory cell scheme in which interference problem is not generated and the selection of each memory cell is possible. We modeled the MFISFET using a ferroelectric capacitor and MOSFET as shown in Fig. 2. The modeled structure is same to MFMISFET [2].

2. Single transistor FeFET memory circuits

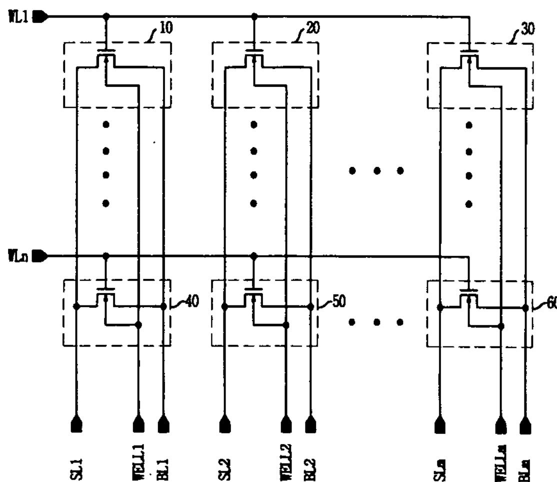
Fig. 3 is a schematic circuit diagram illustrating a memory cell array of single transistor type FeFET. A plurality of unit memory cells are organized in a matrix, by crossing multiple word lines WL_1–WL_n, multiple bit lines BL_1–BL_m , source lines SL_1-SL_m and WELL lines

$WELL_1$-$WELL_m$. A single ferroelectric transistor is arranged with connecting gates to word lines WL_1-WL_n. Here, the single ferroelectric transistor's wells arranged in row direction are connected to the row common well lines $WELL_1$-$WELL_m$. Also, single ferroelectric transistor's sources and drains arranged in row direction are commonly connected to the bit lines BL_1-BL_m or source lines SL_1-SL_m.

As the foregoing illustrations, in a memory arrangement of the ferroelectric memory device, the source lines and the drain lines are commonly used as row lines, also well lines are commonly used as row lines. So, the row lines isolate the well. Namely, since the common row well lines of adjacent different rows are electrically directly connected, voltage can be selectively applied to the well of any row through the common row well lines $WELL_1$-$WELL_m$.



[Fig.2] The Modeled MFISFET Diagram



[Fig.3] Cell Array Schematic of 1T FeFET

The followings illustrate programming for an arbitrary unit memory cell organized the N-type 1T FeFET memory cell array. The word lines hold on to the GND and the common row well lines hold on to the V_{dd} in the reset state. So, the polarization is initialized by the voltage difference of the unit ferroelectric transistor's gate to the well.

For programming the corresponding unit memory cell for "the first state", the power voltage V_{dd} is applied to the corresponding word line WL_1 connected to the unit ferroelectric transistor's gate and the grounded voltage GND is applied to the common row well line $WELL_1$.

The unselected unit memory cells which are connected commonly to the word line WL_1 of the selected unit memory cell hold on to the initial polarization state by applying the power voltage V_{dd} to the corresponding unit ferroelectric transistor's well. Also, the other unselected unit memory cells hold on to the initial polarization state by applying the power voltage V_{dd} to the corresponding unit ferroelectric transistor's well and by grounding the gate.

Next, for programming the corresponding unit memory cell for "the second state", the grounded voltage GND is applied to the corresponding word line WL_1 connected the single ferroelectric transistor's gate and the power voltage is applied to the common row well line $WELL_1$. Since, the voltage difference of the unit ferroelectric transistor's gate to the well is negative(-), then the corresponding unit memory cell is programmed for non-programmed state, namely "the second state". Table 1 showed cell condition for each state programming.

In this way, the write disturb phenomenon is not generated. And, it is possible to selective program the selected cell.

For non-destructive readout operating the corresponding unit memory cell, the read voltage is applied to the corresponding word line WL_1 and the read voltage has range between "the first state threshold voltage" and "the second state threshold voltage".

Fig. 4 is 4x4 cell array results of HSPICE simulation.

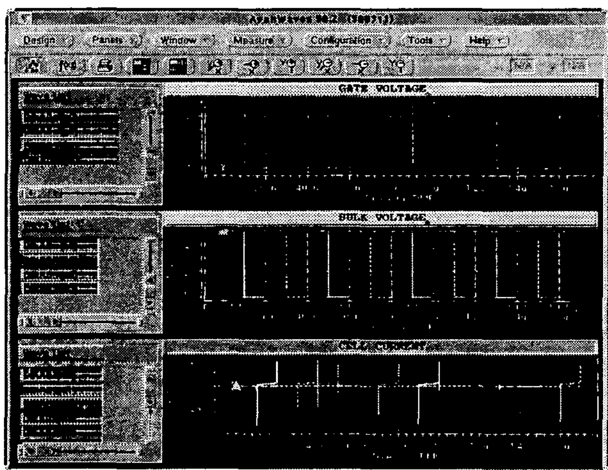
We can distinguish the selected cell current from unselected cell current, as shown in Fig.4.

3. Conclusion

We proposed a single transistor type feroelectric field effect transistor memory cell scheme without disturbance and confirmed successful bit operation.

Table1. N-Channel MF(M)ISFET Write Scheme

	RESETB	PROGRAM	
		Selection Cell	Unselection Cell
GATE	GND	VDD	GND
BULK	VDD	GND	VDD
SOURCE	VDD	GND	VDD
DRAIN	VDD	VDD	VDD



[Fig.4] Results of HSPICE simulation of 4x4 cell array

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