New Inductance Simulator Topologies Realized with DO-OTAs

Hakan KUNTMAN [1] Serdar MENEKAY[2] Oğuzhan ÇİÇEKOĞLU[3] Ayten KUNTMAN[4]

[1]İstanbul Technical University, Faculty of Electrical and Electronics Engineering, Department of Electronics and Communication Engg., 80626, Maslak, İstanbul, TURKEY
E-Mail: kuntman@ehb.itu.edu.tr

[2]Turkish Air-Force Academy, Yeşilyurt, İstanbul, TURKEY
E-Mail: s.menekay@hho.edu.tr

[3]Boğaziçi University, M.Y.O. Electronics Prog., 80815 Bebek-İstanbul, TURKEY
E-Mail:cicekogl@boun.edu.tr

[4]İstanbul University, Faculty of Engineering, Department of Electrical and Electronics Engg., 34800, Avcılar, İstanbul, TURKEY
E-Mail:akuntman@istanbul.edu.tr

Key words: analogue circuits, OTA-C based circuits, inductance simulation, dual-output OTAs

Abstract: In this paper four lossy and one lossless inductance simulator topologies employing a single DO-OTA are presented. For the topologies proposed the inductance L_{eq} and the series resistance R_{eq} are independently adjustable. The topologies employ a single capacitor and are canonic in the number of capacitors. The resistors in the topologies can easily be implemented also with DO-OTAs. In this case the topologies proposed change to DO-OTA-C inductor simulators which is important from the integration point of view. Simulation results are included to verify theory.

1. Introduction

Actively simulated grounded inductors find applications ranging from filter to oscillator design to cancellation of parasitic inductances [1-8]. Many design possibilities presented in the literature employ operational amplifiers, current conveyors, OTAs etc. as active element. The actively simulated inductors can be classified due to the type (L series ±R, L parallel ±R) or the number of active and passive elements employed, or if they simulate a grounded or floating inductance. Further comparison can be made whether they realise lossy or lossless types.

Current-mode designs are accepted owing the possibility to operate at higher frequencies compared to the circuits employing op-amps. The current-mode analogue circuits employing active elements such as OTAs, current conveyors, DO-OTAs, DO-CCIIs, FTFNs play an important role in the IC design, since these active elements exhibit greater linearity, wider bandwidth and wider dynamic range over the voltage mode counterparts [1-13].

Although several circuits for realisation of immitance and inductance simulators have been reported in the literature, little attention has been paid for realising such type simulator circuits by using DO-OTAs.

In this paper four lossy and one lossless inductor simulator topologies employing a single DO-OTA are presented. For the topologies the inductance L_{eq} and the series resistance R_{eq} are independently adjustable.

2. DO-OTA

The circuit symbol of the DO-OTA (dual-output operational transconductance amplifier) is given in Figure 1. Ideally, DO -OTA is assumed an ideal voltage-controlled current source and can be described by following equation,

$$I_0^+ = g_{m1}(V^+ - V^-) \quad , \quad I_0^- = g_{m2}(V^- - V^+) \quad (1)$$

where I_0^+, I_0^- are dual output currents, V^+ and V^- denote noninverting and inverting input voltage of the DO-OTA, respectively.

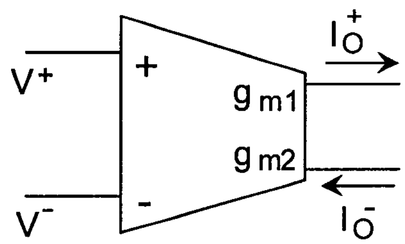
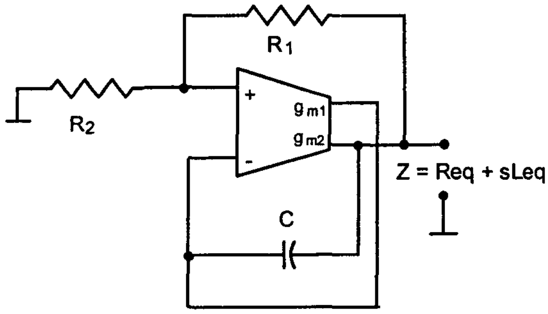
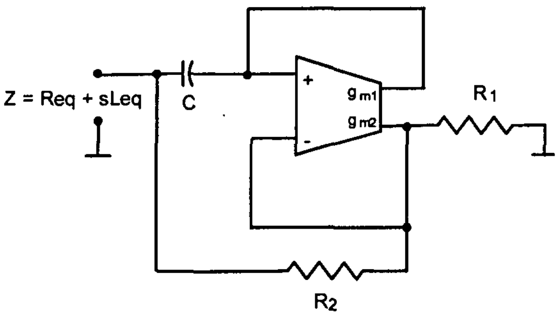


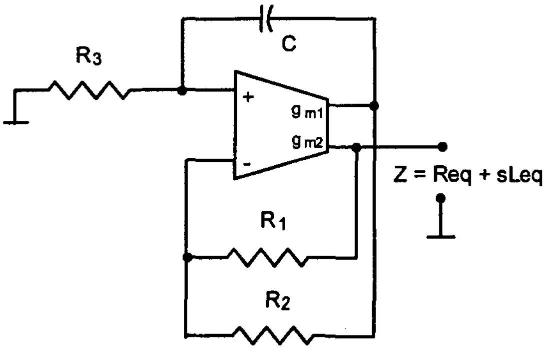
Figure 1. Circuit symbol of DO-OTA.

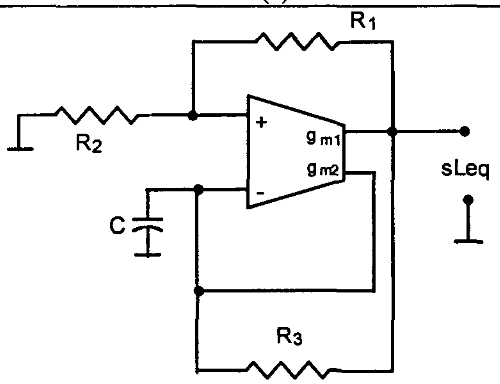
3. The proposed circuit topologies

The proposed three lossy grounded inductance simulator topologies are shown in Fig.2a,b and c. A lossless inductance simulator circuit is illustrated in Figure 2d. All of the circuits were derived by using a systematic circuit generation method [14]. The corresponding equations for equivalent inductance and equivalent resistance are also given in Fig.2.

<table>
<tr>
<td>

(a)</td>
<td>$$R_1 = \frac{1}{g_{m2} - g_{m1}}$$
$$L_{eq} = \frac{C}{g_{m1}}\left(R_1 + R_2\right),\ R_{eq} = R_1 + R_2$$
L with series R</td>
</tr>
<tr>
<td>

(b)</td>
<td>$$R_2 = \frac{1}{g_{m1}}$$
$$L_{eq} = C\ R_2\left(g_{m2}R_2.R_1 - R_2 - R_1\right),$$
$$R_{eq} = R_1 + R_2$$
L with series R</td>
</tr>
<tr>
<td>

(c)</td>
<td>$$R_2 = \frac{1}{g_{m2}} \quad R_3 = \frac{1}{g_{m1} - g_{m2}}$$
$$L_{eq} = CR_1R_3,\ R_{eq} = R_1 + R_3 + \frac{R_1R_3}{R_2}$$
L with series R</td>
</tr>
<tr>
<td>

(d)</td>
<td>$$R_3 = \frac{1}{g_{m2}}$$
$$g_{m1} = \frac{R_1 + R_2 + R_3}{R_2R_3}$$
$$L_{eq} = C\frac{R_1\left(R_1 + R_2\right)}{R_3\left(g_{m1} - 1/R_3\right)}$$
lossless L</td>
</tr>
</table>

Figure 2. Proposed DO-OTA based inductance simulator topologies

4. Simulation results, verification and discussion

All of the circuits illustrated in Fig. 2 are tested with SPICE simulations. The test circuits were constructed with the CMOS realization of cascode DO-OTA illustrated in Fig.3. The SPICE simulations were performed with the high-accurate macromodel of this CMOS cascode DO-OTA [12,13].

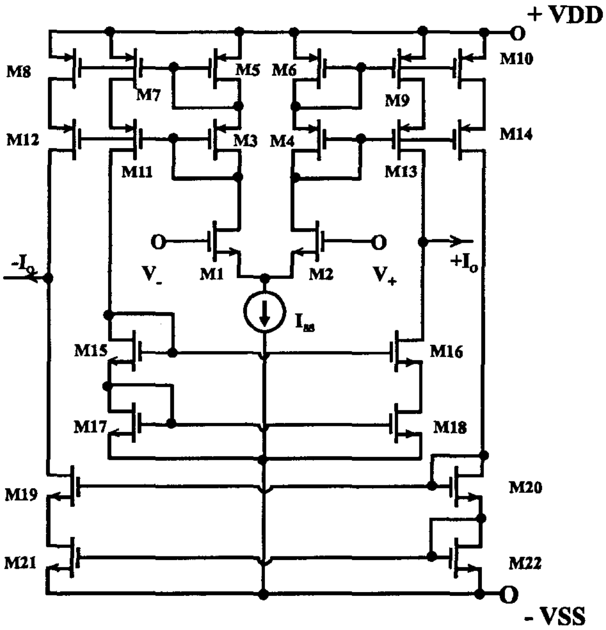


Figure 3. CMOS cascode DO-OTA structure used for SPICE simulations.

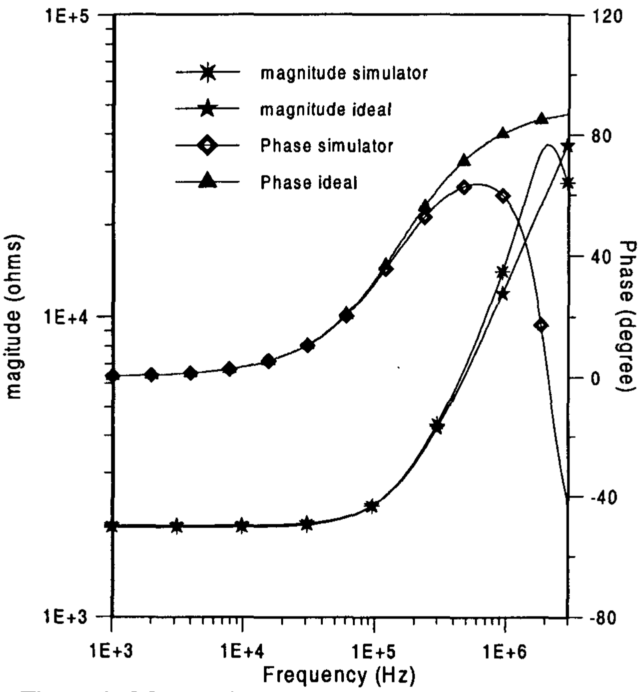


Figure 4. Magnitude-frequency and phase-frequency responses of ideal and simulated R-L circuits

To demonstrate the accuracy of topologies proposed, the lossy inductance simulation topology illustrated in Fig.2a is chosen. The simulated series R-L combination consists of an inductor L_{eq}=2mH and a resistance R_{eq} = 2k. To obtain these values, the component values R_1, R_2 and C are chosen as R_1=R_2 =1kΩ, and C=1nF. respectively. The DO-OTA transconductances are taken as g_{m1}= 1mA/V and g_{m2} = 2mA/V. The circuit was supplied with symmetrical supply voltages of ±10V. The magnitude- and phase-frequency responses of the inductance simulation circuit obtained from SPICE program is given in Fig.4 with the responses of the ideal series R-L circuit. From Fig. 4 it can be easily observed that the SPICE simulation results obtained for the realization circuit are in good agreement with the results obtained for ideal R-L circuit in a certain frequency range. The deviations in this certain range and the drastical differences observed outside of this range between the simulated and ideal magnitude- and phase-frequency resposes are caused by the non-idealities of the active element, especially caused by the limited output resistances of the DO-OTA. The influence of the limited output resistances can be kept small by using DO-OTA structures providing higher output impedances.

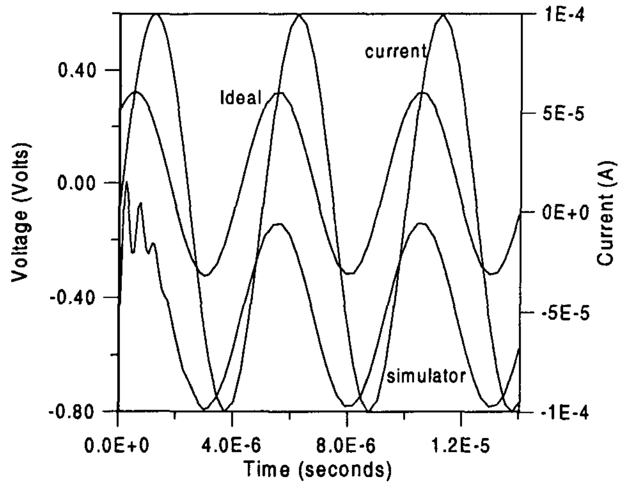


Figure 5. Transient responses of ideal and simulated R-L circuits for a 200 kHz sinusoidal current of 100μA.

Furthermore a 200 kHz and 100μA sinusoidal current is applied to the circuit and the waveform of the voltage across the circuit is observed. To compare the results with the response of the equivalent R-L circuit, the transient response of the equivalent R-L circuit is also obtained with SPICE simulations. The waveforms of the simulator and the ideal circuit are shown in Fig. 5. Comparision of the responses of simulator and ideal circuits shows that the simulator yields approximately the same waveform with the same phase-shift but with an offset voltage of -462mV. Note that this offset voltage is caused by the CMOS realization circuit and can be kept as small as possible by proper design of the DO-OTA.

5. Conclusions

In this paper four different inductor active simulating topologies employing a single DO-OTA are proposed. Each resistor in the topologies can easily be implemented with a single DO-OTA [13]. In this case the topologies employ only the same type active element which results in DO-OTA-C inductor simulators. Note that the realization with DO-OTAs and a capacitor is important from the integration point of view. This type realization provides the IC designer the possibility of obtaining adjustable inductors since the DO-OTA transconductance can be easily controlled by the biasing currents. Simulation results are included to verify theory.

References

[1] K. Pal, "Novel floating inductance using current conveyors", *Electronics Letters,* 17, no. 18, pp 638, 1981.

[2] K. Pal, "New inductance and capacitor floating schemes using current conveyors", *Electronics Letters,* 17, no. 21, pp. 807-808, 1981.

[3] V. Singh, "Active RC single-resistance-controlled lossless floating inductance simulation using single grounded capacitor", *Electronics Letters*, 17, no. 24, pp. 920-921, 1981.

[4] R. Senani, "Novel lossless synthetic floating inductor employing a grounded capacitor", *Electronics Letters,* 18, no. 10, pp. 413-414, 1982.

[5] M. Higashimura, Y. Fukui, "Novel method for realizing lossless floating immittance using current conveyors", *Electronics Letters,* 23, no. 10, pp. 498-499, 1987.

[6] A. N. Paul, D. Patranabis, "Active simulation of grounded inductors using a single current conveyor", *IEEE Transactions on Circuits and Systems*, 28, no. 2, pp. 164-165, 1981.

[7] S.I. Liu, Y. Y. Yang, "Higher-order immittance function synthesis using DO-OTAs", *Electronics Letters*, 32, no. 25, pp. 2295-2296, 1996.

[8] O. Çiçekoğlu, H. Kuntman, "Single CCII+ Based Simulation of Grounded Inductors", Proc. of *European Conference on Circuit Theory and Design, ECCTD 97,* Budapest, Hungary, pp 105-109, 30. Aug.- 2 Sept., 1997.

[9] M.T. Abuelma'atti, A.A. Al-Ghumaiz and M.H. Khan, "Novel CCII- based single-element controlled oscillators employing grounded resistors and capacitors", *International Journal of Electronics,* 78, pp 1107-1112, 1995.

[10] M.T. Abuelma'atti, A.A. Al-Ghumaiz, "Novel CCI-Based Single Element Controlled Oscillators Employing Grounded Resistors and Capacitors", *IEEE Transactions on Circuits and Systems I Fundamental Theory and Applications*, 43, Iss 2, pp 153-156, 1996.

[11] A. Sedra, K.C. Smith, "A Second-Generation Current Conveyor and Its Applications", *IEEE Transactions on Circuit Theory,* 17, pp 132-134, 1970.

[12] H. Kuntman, "Simple and accurate nonlinear OTA macromodel for simulation of CMOS OTA-C filters", International Journal of Electronics, Vol. 77, pp. 993-1006, 1994.

[13] H. Kuntman, A. Özpınar, "On the realization of DO-OTA-C oscillators", Microelectronics Journal, Vol.29, No. 12, pp.991-997, 1998.

[14] O. Çiçekoğlu, H. Kuntman, "Circuit design techniques: AD-HOC method or systematic generation methods", Proc. of the 10th International Conference on Microelectronics (ICM'98), Monastir, Tunisia, pp.187-190, December 14-16, 1998.