Practical Fault Coverage of Supply Current Testing for Open Fault in TTL Combinational Circuits

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Abstract: There are some variations in quiescent supply current of TTL SSIs. Thus, some variations in quiescent supply current of logic circuits made of TTL SSIs will be generated. The variations make it difficult to apply supply current test methods to tests of TTL circuits. In this paper, in order to examine the applicability to TTL circuits, fault coverages of a supply current test method for open faults in some ISCAS-85 benchmark circuits are evaluated, which are made of TTL LS-type SSIs. The experimental results shows that if SSIs are used for implementation having the variation of quiescent supply current within 1%, supply current test methods are applicable for the tests.

1. Introduction

Recently, quiescent supply current testing of logic circuits has been shown to be useful for realizing high reliable logic systems[1,2,3]. Especially, IDDQ testing is very effective in CMOS logic IC tests. Also, test input generation algorithms for the IDDQ testing have been proposed. In a fault-free CMOS IC, very small quiescent supply current will be generated in operation. If large quiescent supply current is generated, the circuit can be determined as faulty. The IDDQ testing can detect physical defects which can not be modeled as logical faults and is effective for realizing high reliable systems.

Besides CMOS ICs, bipolar circuits, like TTL and ECL circuits, are well used now for implementing logical systems. Especially, they are used in the electronic equipments which require a high speed operation and are used as a core in logic system. If they do not work, the generated damage will be extremely large. Thus, very high reliability is requested for bipolar circuits.

Quiescent supply current of unfaulty bipolar gates depends on the output logic values[4]. Thus, even if any defects do not occur in bipolar circuit, quiescent supply current flows from the VCC terminal to the GND terminal. Thus, IDDQ test technique is not applicable to fault detection problems of bipolar circuits.

In order to detect faults in bipolar circuits with their quiescent supply currents, a new fault detection method should be developed. Thus, in the past, we proposed a supply current test method for bipolar circuits[4]. The method is to detect faults by measuring the quiescent supply current of a circuit under test and comparing it with the unfaulty circuit. Also, a fast random test input generation method for the supply current testing and an algorithmic one are proposed in [5] and [6], respectively. Furthermore, we proposed a test method which is applicable even if there are some variations among gates[7], since there are some variations in the quiescent supply current of each gate in implemented logic circuits. However, the practical fault coverage of the supply current test method in TTL combinational circuits has not been examined fully.

Faults which occur well in logic circuits fabricated with the state-of-art technology are bridging faults and open ones. As for bridging faults, when they are sensitized, extremely large quiescent supply current will be generated. Thus, they are easy to be detected by any supply current tests. On the other hand, open fault will not generate any large quiescent supply current in the sensitization. It leads that they are difficult to be detected by supply current tests. In this paper, in order to examine the practical fault coverage of our supply current tests, open faults in TTL circuits are selected as our targeted faults.

In this paper, a supply current test method is proposed in section 2. After that, our executed experiments and the obtained results are described in section 3.

2. Supply Current Test for TTL Circuits

Quiescent supply current $I_{CCN}(T_j)$ of an unfaulty TTL circuit made of Ns gates which flows when the i-th test input vector T_j is applied to the circuit, can be defined by Eq.(1).

$$I_{CCQN}(T_j) = \sum_{i=1}^{Ns} I_{CCQNi}(T_j) \quad (1)$$

where $I_{CCQNi}(T_j)$ is the quiescent supply current of the i-th TTL gate generated when T_j is provided to the unfaulty circuit. Also, quiescent supply current $I_{CCC}(T_j)$ of a circuit under test(CUT) can be defined by Eq.(2)[5].

$$I_{CCQC}(T_j) = \sum_{i=1}^{Ns} I_{CCQCi}(T_j) \quad (2)$$

where $I_{CCQCi}(T_j)$ is the quiescent supply current of the i-th TTL gate in the CUT generated by the T_j application.

If Eq.(3) is satisfied, the CUT is determined as faulty.

$$\Delta I_{CCQ}(T_j) \geq I_{th} \quad (3)$$

where $\Delta I_{CCQ}(T_j)$ is defined by Eq.(4) and I_{th} is the threshold value to determine whether the CUT is faulty or not.

$$\Delta I_{CCQ}(T_j) = | I_{CCQC}(T_j) - I_{CCQN}(T_j) | \quad (4)$$

Quiescent supply current of unfaulty TTL gates depends on the output logic values[6]. In this paper, it is assumed that quiescent supply currents I_{iL} and I_{iH} flow in the i-th TTL gate when the output logic value is L and when it is H, respectively.

When an open fault is excited by a test input vector T_j, any large quiescent supply current change will not be generated in the gate having the open fault at the output signal line. Thus, $\Delta I_{CCQ}(T_j)$ is defined by the supply current changes of gates whose output logic values are changed by the fault propagation. A set of the gates is called Sg in this paper. and $\Delta I_{CCQ}(T_j)$ can be defined as Eq.(5) by means of Sg.

$$\Delta I_{CCQ}(T_j) = \sum_{i \in Sg} \Delta I_i(T_j) \quad (5)$$

where $\Delta I_i(T_j)$ is quiescent supply current change of the i-th gate which is generated when T_j is provided to the circuit and is defined by Eq.(6).

$$\Delta I_i(T_j) = \begin{cases} I_{iL} - I_{iH}, & \text{the output of the i-th gate} \\ & \text{is changed from H to L} \\ I_{iH} - I_{iL}, & \text{the output of the i-th gate} \\ & \text{is changed from H to L} \end{cases} \quad (6)$$

In fact, there are some variations in quiescent supply current among ICs. The generation process can as modeled as a Gaussian distribution process $N(\mu_{Ni}(T_j), \sigma(T_j)^2)$, where $\mu_{Ni}(T_j)$and $\sigma(T_j)^2$ are the mean value and the variance of quiescent supply current which flows when a test input vector (T_j) is provided to the CUT.

Supply current of logic circuits made of TTL gates can be modeled as a Gaussian distribution. Examples of the distributions for an unfaulty circuit and the fault one are shown in Fig.1. By the variation generated in IC productions, $I_{CCQN}(T_j)$ and $I_{CCQC}(T_j)$will not be defined as values and fault can not be detected by using Eq.(3). The supply currents should be defined by means of distribution functions.

If the distributions of $I_{CCQN}(T_j)$and $I_{CCQC}(T_j)$ are separated each other, the fault can be detected. Otherwise, it is not detected. However, if they are overlapped with small probability, in our test method, it is determined that the fault can be detected. In order to introduce probability into supply current tests, the statistical analysis method with level of significance(α) is used in our test method. That is a fault is detected with α, which is used for judging whether any two distributions are separated each other like in [7]. In the case of the fault in Fig.1, since the distribution of $I_{CCQC}(T_j)$ can be judged to be different from $I_{CCQN}(T_j)$, by using it the circuit is determined as faulty.

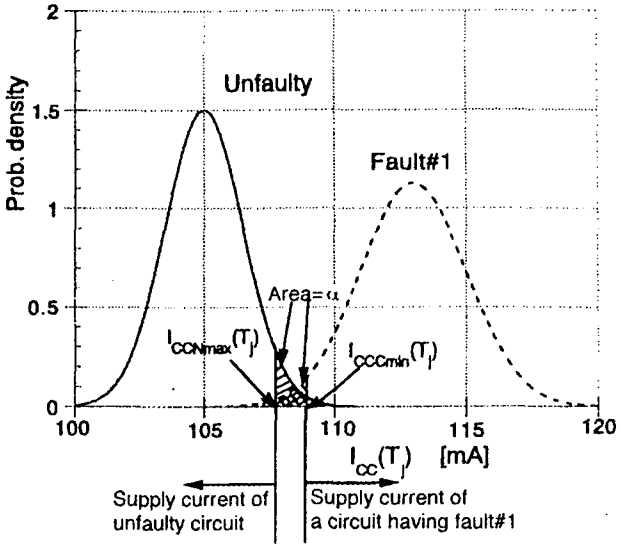

Fig.1 Fault detection with level of significance.

3. Experimental Evaluation

In order to examine fault coverage of open faults in TTL circuits, test input vectors are generated for ISCAS-85 benchmark circuits made of TTL LS-type SSIs. In our experiments, the vectors are derived by a random test input generation method which is almost the same as in [5]. At first, an input vector is generated by using random numbers and the output logic value of each gate is determined by logical fault simulation. From the output logic value of each gate, the supply current of the circuit is calculated by the method in [8]. From the current and specified variation, a Gaussian distribution can be derived, whose example is as shown in Fig.1. As shown in Fig.1, if the distribution of quiescent supply current of faulty circuit can be separated to the unfaulty one by specifying α, the vector is employed as a test input vector for detecting the fault.

Supply current of a CUT is measured at the supply voltage terminal. Usually, current is measured as voltage by means of an I-V transformer. Thus, we assume that supply current of CUT can be measured as shown in Fig.2(a), where R_{MES} is an equivalent resistor of the transformer.

As the circuit size of a CUT becomes large, the voltage drop across the resistor R_{MES} will become large. It leads that the supply voltage may be out of the recommended power supply voltage range of ICs. Thus, R_{MES} is determined so that the supply voltage for the IC can be in the range even if the maximum supply current flows. By using it and the circuit in Fig.2(a), fault coverages for the CUTs are examined.

If supply current is measured according to Fig.2(a) fautly effects on supply current may not be observed, especially for large size of circuits. Thus, in our experiments, the CUTs are divided into circuit blocks and the supply current of each block is measured with R_{MES} =1Ω as shown in Fig.2(b). It is determined as faulty if abnormal quiescent supply current flows in any circuit block.

In our experiments, the variance of supply current in each IC is specified by the percentage to the one of each unfaulty IC. As CUTs, C432 and C5315 are used, whose specifications are shown in Table 1. The numbers of SSIs in C432 and C5315 are 472 and 5553, respectively. Usually, circuits having such large number of SSIs will not be fabricated on printed boards. However, since they can be used for evaluating the applicability of supply current testing to TTL circuits, they are selected as CUTs in our experiments.

Before testing, a technology mapping is performed, that is, it is determined which gate in ICs is used for each gate in the benchmark circuits. The recommended supply voltage range of TTL LS-type ICs is from 4.75[V] to 5.25[V]. In order to satisfy the specification, benchmark circuits are divided into circuit blocks so that the implemented circuits can work within the voltage range, as shown in Fig.2. The number of obtained circuit blocks of each circuit is shown in Table1.

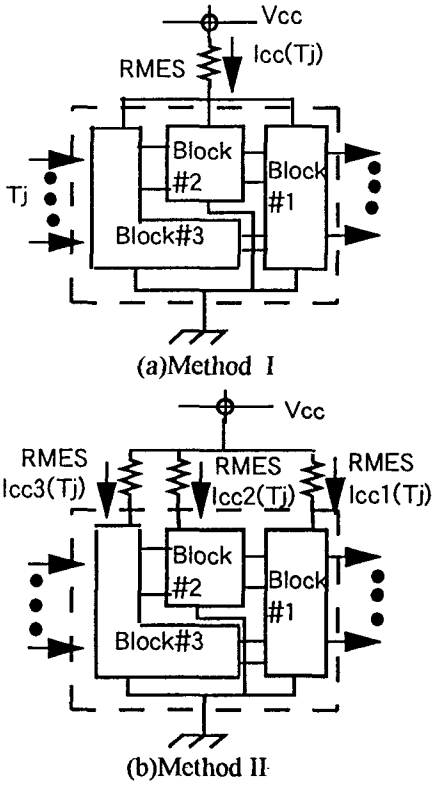

Fig.2 Supply current measurement methods.

Table 1 Circuit under test.

CUT	PIs	POs	ICs	Sig. Lines	Circuit blocks
C432	36	7	472	58	2
C5315	178	128	5553	651	15

Obtained fault coverages for C432 are shown in Fig.3 and Fig.4. As the varience becomes large, the fault coverage will be reduced as shown in Fig.3 and Fig.4. By using smaller value as α, tests can be realized with high reliability. It leads by comparing Fig.3 with Fig.4 that when high reliablity is requested in the tests, fault coverage of supply current testing will be affected by the variation of supply current more strongly. The fault coverage of logic testing for C432 is 98.4%. As shown in Fig.3(a) and Fig.4(a), larger fault coverage can be obtained by our supply current method than logic test one, if the variance of supply current I_{CCi} of each IC can be smaller than 1.0[%].

In the case of C5315, almost the same results can be obtained as C432. The fault coverage of the circuit for logic testing is 98.5%. In the circuit, if the variance is smaller than 1.0[%], higher fault coverage can be obtained by supply current testing like in C432.

In the figures from Fig.3 to Fig.6, fault coverages of supply current tests based on Method II are greater than Method I. Thus, it can be concluded that supply current should be measured by means of Method II if higher fault coverages are requested.

In this paper, only tests for open faults are discussed. Most of the faults in the circuits fabricated with the state-of-art technologies are open faults and shorts. Most of bridging faults can be detected by supply current testing. Thus, it is expected that supply current testing is practically applicable for TTL circuit tests.

4. Conclusion

In this paper, fault coverages of open faults in ISCAS benchmark circuits made of TTL LS-type SSIs are evaluated in order to examine the applicability of supply current testing to TTL circuit tests. There are some variations in quiescent supply currents of each ICs. In the evaluation, it is assumed that the variation of supply current in SSIs can be modeled as a Gaussian distribution. Furthermore, a statistical technique with level of significance is used in our supply current test method. The experimental results promise us the feasibility of supply current tests for TTL circuits.

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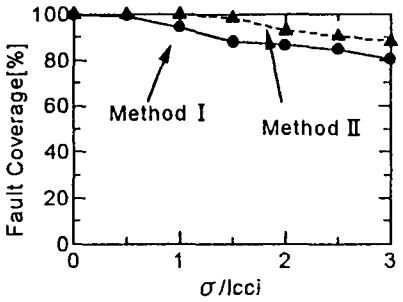
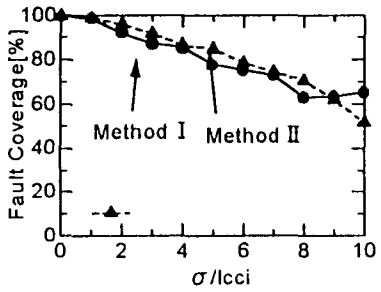
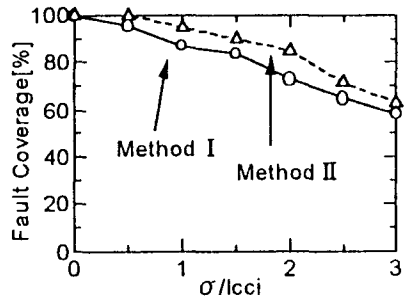


(a)fault coverage for σ/I_{cci} from 0 to 3%

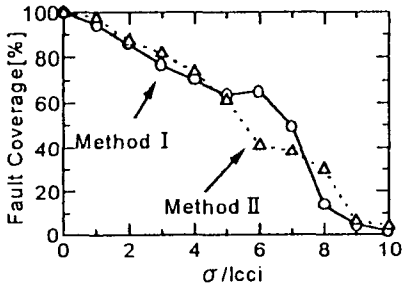


(b)fault coverage for σ/I_{cci} from 0 to 10%

Fig.3 Obtained fault coverages for C432 with α=0.1.

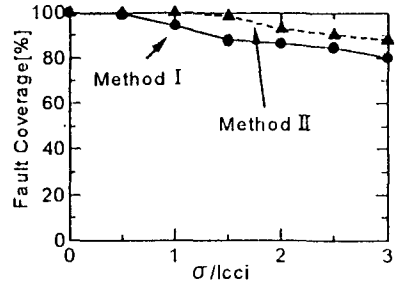


(a)fault coverage for σ/I_{cci} from 0 to 3%

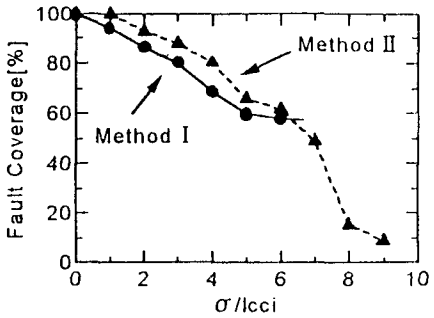


(b)fault coverage for σ/I_{cci} from 0 to 10%

Fig.4 Obtained fault coverages for C432 with α=0.01.

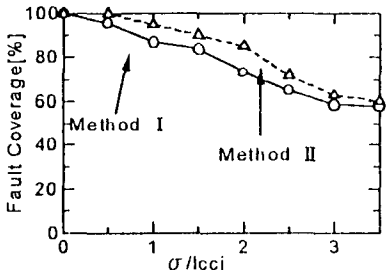


(a)fault coverage for $\sigma/I_{cci}\sigma$from 0 to 3%



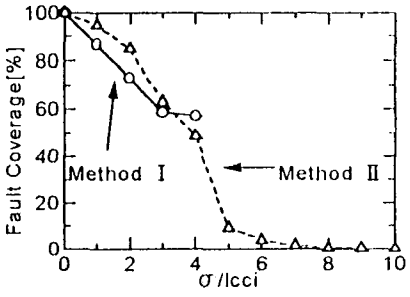
(b)fault coverage for σ/I_{cci} from 0 to 10%

Fig.5 Obtained fault coverages for C5315 with α=0.1.



(a) fault coverage for σ/I_{cci} from 0 to 3.5%

(b)



(b)fault coverage for σ/I_{cci} from 0 to 10%

Fig.6 Obtained fault coverages for C5315 with α=0.01