A Test Input Sequence for Test Time Reduction of I_{DDQ} Testing

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Abstract: It is shown that I_{DDQ} testing is very useful for shipping fault-free CMOS ICs. However, test time of I_{DDQ} testing is extremely larger than one of logic testing. In this paper, a new test input sequence generation methodology is proposed to reduce the test time of I_{DDQ} testing. At first, it is shown that I_{DDQ} test time will be denominated by charge supply current for load capacitance of gates whose output logic values are changed by test input vector application and the charge current depends on input sequence of test vectors. After that, a test input sequence generation methodology is proposed. The feasibility is checked by some experiments.

1. Introduction

It is well-known that most of defects in CMOS ICs fabricated with the state-of-the-art technology are shorts. The shorts can be modeled at the circuit level as shorts between adjacent signal lines and are called "bridging faults". Bridging faults in CMOS ICs are very difficult to be detected by using logic testing. On the other hand, they can be detected by measuring supply current easier than by measuring output logic values.

Recently, I_{DDQ} testing of CMOS logic ICs has been shown to be useful for realizing high reliable logic systems[1]. In a fault-free CMOS IC, very small quiescent supply current, which is called "I_{DDQ}", will be generated in operation. If large quiescent supply current is generated, the IC can be determined as faulty by observing I_{DDQ}, i.e. I_{DDQ} testing. Since the I_{DDQ} testing can detect physical defects which can not be modeled as logical faults, it is effective for shipping high reliable ICs.

On the other hand, extremely large test time will be required to detect them by I_{DDQ} testing. When an input vector is provided to the IC to be tested, switching current will appear. After the switching current disappears, charge current will flow to charge load capacitances of gates whose logic values change L to H levels. When the load capacitances are charged by the supply voltage, the charge current will disappear and only I_{DDQ} will be generated. In I_{DDQ} tests, ICs can be determined as faulty if elevated I_{DDQ} is measured. Since dynamic current consisting of switching and charge currents cannot disappear in a short time, I_{DDQ} tests require a large test time.

In [2,3], test input sequence is discussed for reducing test time of I_{DDQ} tests. Also, test input sequence for I_{DDQ} tests is proposed so that output signal lines of only a limited number of CMOS gates can be changed simultaneously in order to shorten the test time. However, in [2,3], only switching current which is generated whenever output logic value of each gate changes is discussed for the test time reduction. Nowadays, it has been requested to test ICs with high resolution by I_{DDQ} testing. In the case, switching current does not determine the test speed but charge current denominates it. Thus, the methodology in [2,3] cannot be used for the tests.

In this paper, we show that I_{DDQ} test time does not depend on only the switching current but also the charge current for the gates whose output logic values change L to H levels. Also, we reveal that I_{DDQ} test time can be shortened by using the test input vectors and the applied sequence which is obtained so that charge current can disappear as soon as possible. We examined the feasibility by some experiments. In this paper, we show one of the experimental results.

The supply current generation mechanism in CMOS circuits is described in Section 2. After that, test input sequence generation methodology for test time reduction of I_{DDQ} testing is proposed in Section 3. The simulation result obtained by using our approach to generate test input sequence is shown in Section 4.

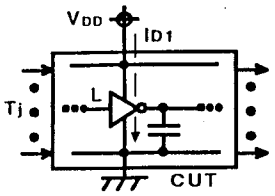
2. Supply Current Waveform in Operation of CMOS Circuit

Whenever the output logic value of any logic gate in a CMOS IC changes, some switching current will be generated. Thus, large dynamic supply current, which is generated by the switching current of each gate, will flow into the IC.

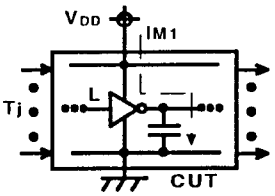
In Fig.1, supply current paths in a CMOS gate are shown which are generated when a test input vector T_j is provided to the circuit. At first, switching current I_{DI} will flow. After that, charge current I_{MI} will flows [4]. Examples of supply current waveforms of I_{DI} and I_{MI} are shown in Fig.2. As shown in Fig.2, the switching current will disappear quickly, while charge the current will not disappear.

I_{DDQ} will appear after charge current disappears. Thus, in order to test an IC with I_{DDQ} measurements, we must wait to measure supply current until the charge current disappears. Generally, in I_{DDQ} testing, test input vectors are provided per 100 μsec, since it takes 100 μsec for charge current to disappear in many commercial ICs. It means that it takes an extremely large test time for I_{DDQ} testing.

Supply current waveform of an invertor gate is shown in Fig.3. As shown in Fig.3(c), larger supply current flows when the output changes from L to H than when it changes from H to L. It stems from charge current for parasitic capacitance of the gate output.

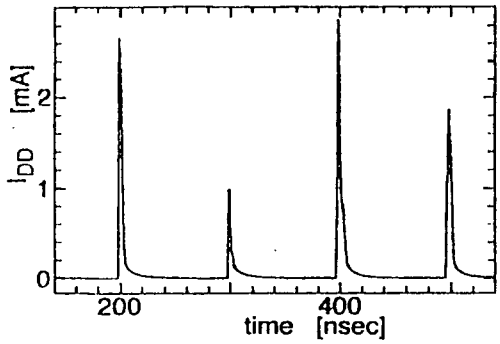


(a) When test input vector Tj is provided

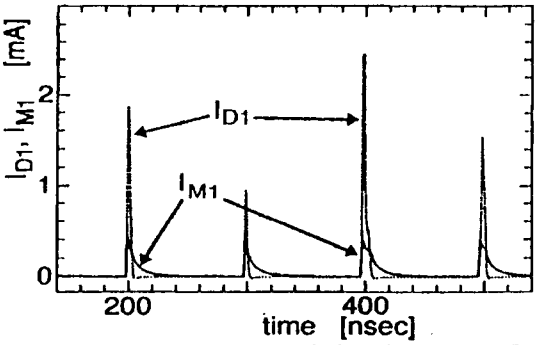


(b) After switching current disappears

Fig.1 Supply current paths in CMOS circuits.



(a) Supply current I_{DD}



(b) Switching current I_{D1} and charging current I_{M1}

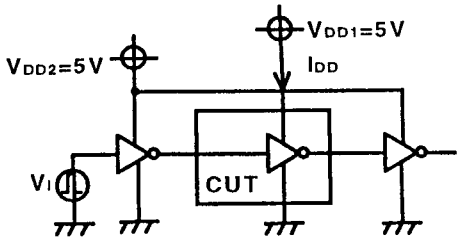
Fig.2 Examples of supply current waveforms in unfaulty circuit.

Supply current of CMOS circuits can be defined as the sum of supply current of each gate. Thus, after switching supply current disappears, only charge supply current flows as shown in Fig.4(b).

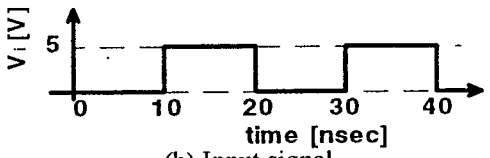
After a specified time T_M from each test input vector application, the supply current of a CUT is measured as I_{DDQC}. If Eq.(1) is satisfied, the CUT is determined as faulty.

$$I_{DDQC} \geq I_{th} \qquad (1)$$

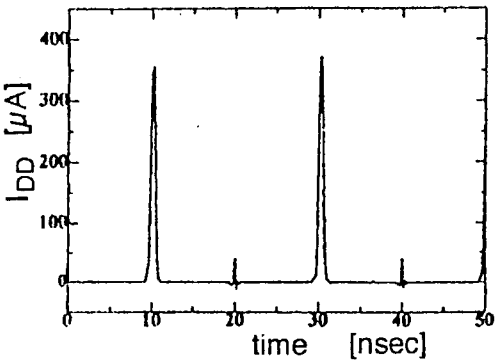
where I_{th} is the threshold value for determining whether the CUT is faulty or not and is determined by considering process variation of the ICs.



(a) Experimental circuit

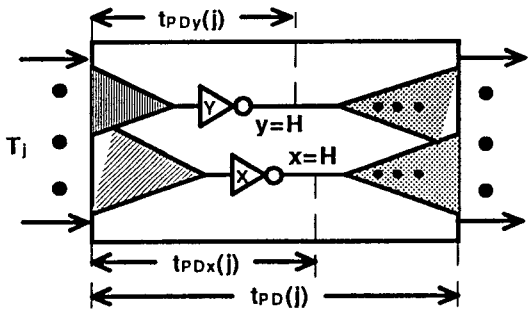


(b) Input signal

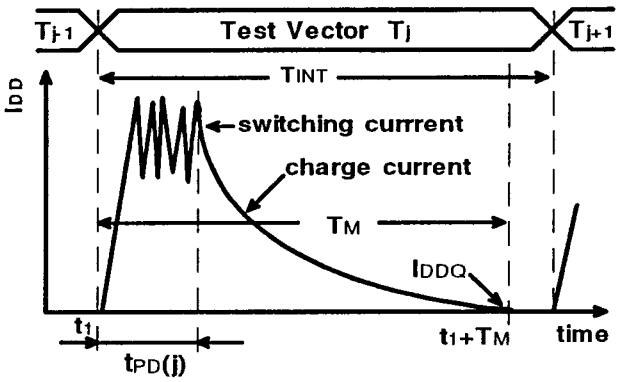


(c) Supply current waveform of I_{DD}

Fig.3 Supply current waveform of invertor gate



(a) Example circuit



(b) Supply current waveform

Fig.4 Supply current waveform in unfaulty CMOS circuit

Charge current depends on how many gates change the output from L to H by input vector application. Unless the charge current disappears, I_{DDQ} cannot be measured. Thus, test time of I_{DDQ} testing is determined by the charge current besides the switching current. It means that the time depends on the applied sequence of test input vectors.

Until now, only one test input sequence generation method to realize test time reduction of I_{DDQ} tests has been proposed [2,3]. In [2,3], only switching current is considered in the test input sequence generation. However, as shown in Fig.4(b), charge current denominates the test time of I_{DDQ} testing. Thus, we attempted to develop a new strategy to generate the test input sequence for reducing test time in I_{DDQ} tests. In our approach, test input sequences are derived so that charge current can disappear more quickly.

3. Test Input Sequence Generation for I_{DDQ} Tests

Our test input sequence generation methodology consists of two kinds of steps. The first one is to generate exciting test input vectors, with which as many bridging faults can be detected as possible. The other one is to modify some of the input vectors so that charge current can disappear quickly.

Charge current depends on how many gates change the output logic values by applying a test vector. If many gates change the output logic values from L to H levels, charge current cannot disappear quickly. Also, switching current is affected by propagation delay in the circuit. If the propagation delay time is large, it will be generated after a while from providing the test input vector. It leads that charge current cannot disappear quickly. Thus, in our test input sequence generation, the longest propagation path is derived and it is attempted that the propagation delay time can be shortened as much as possible by modifying some exciting test input vectors.

Exciting test input vectors can be generated easily, since many bridging faults between any two signal lines can be excited by a test input vector, which can generate complementary logic values to the lines in the unfaulty circuit. Thus, if some faults cannot be excited after the test vector modification, other vectors are modified so that the faults can be excited.

After generating excited input vectors, test input sequence will be determined so that charge current of unfaulty circuit can disappear quickly. That is the reason why if large supply current flows in a faulty circuit after a specified time T_M defined in Fig.4(b), supply current change will be observed and the circuit can be determined as faulty.

In unfaulty circuits, test input vectors having large propagation delay time are modified so that charge current can disappear quickly. At first, the critical path is selected in the test input vector applications, which is defined as the path having the largest propagation delay time. It is attempted to reduce the propagation delay time by modifying logic values in some primary input terminals. If any bridging faults cannot be excited by the modification, other test vectors are attempted to be modified. These modifications are continued to be executed until any propagation delay times cannot be improved.

4. Simulation Results

The feasibility of our test input sequence generation methodology is checked by some experiments. In our experiments, the circuit in Fig.5 is used as a circuit to be tested.

At first, I_{DDQ} test vectors are derived for bridging faults in the circuit by random test generation algorithm and they are arranged randomly. The input sequence is shown in Table 1(a). From the sequence, a critical path having the largest propagation time is selected, which is T6 in Table 1(a). On the path, a gate is selected with some heuristic and the test input vector is modified so that logical change from H to L can not be propagated to the output terminal. The obtained input vector is T6' in Table 1(b). By employing T6' instead of T6, some bridging faults cannot be detected. Thus, in order to detect them, T5 and T7 are modified as shown in Table 1(b).

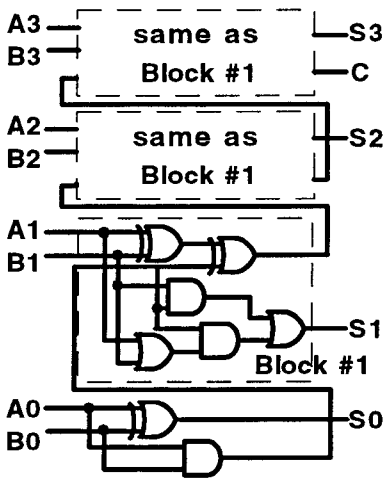


Fig.5 Circuit under test

Table 1 Test input sequence for circuit in Fig.5

(a) Original test input sequence

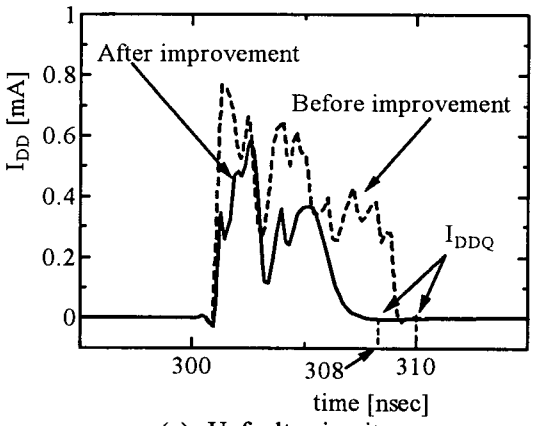
Sig. name	Original test input sequence										
	T0	T1	T2	T3	T4	T5	T6	T7	T8	T9	T10
A0	L	L	L	H	H	H	L	H	L	L	H
B0	L	H	L	H	L	H	L	H	H	L	L
A1	L	H	L	H	L	H	L	L	L	L	L
B1	L	L	L	H	H	H	H	H	L	L	L
A2	L	L	L	L	H	L	H	H	L	H	H
B2	L	H	L	H	H	L	L	L	L	H	L
A3	L	L	H	L	H	H	L	H	L	L	L
B3	L	H	H	H	H	L	H	L	H	L	H

(b) Our improved test input sequence

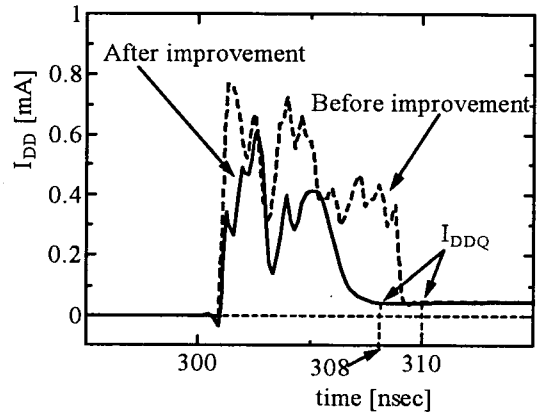
Sig. name	Our improved test input sequence										
	T0	T1	T2	T3	T4	T5'	T6'	T7'	T8	T9	T10
A0	L	L	L	H	H	H	L	L	L	L	H
B0	L	H	L	H	L	H	L	L	H	L	L
A1	L	H	L	H	L	H	L	L	L	L	L
B1	L	L	L	H	H	H	H	L	L	L	L
A2	L	L	L	L	H	L	H	H	L	H	H
B2	L	H	L	H	H	H	H	L	L	H	L
A3	L	L	H	L	H	H	L	L	L	L	L
B3	L	H	H	H	H	L	H	L	H	L	H

It is examined how much test time reduction can be obtained by using a SPICE simulator. The examples of the supply current waveforms generated when the 7-th test vector is provided to the circuit are shown in Fig.6. In Fig.6, test input vectors are applied to the circuit per 50 nsec. It is found out from Fig.6(a) that the charge current in the unfaulty circuit can disappear after 8 nsec if the modified input vector is used. In Fig.6(b), the charge current of the modified test input vector may not disappear at 308 nsec. However, the difference between the unfaulty circuit and the faulty one in the supply current can be observed as shown in Fig.6(b) and the fault can be detected by I_{DDQ} testing. It leads that a test input sequence should be generated so that load capacitors in only unfaulty circuits can be charged more quickly.

Our simulation results show that by measuring supply current after 8 nsec of each test input vector application, all of the bridging faults in Fig.5 can be detected by I_{DDQ} testing. Also, the test time is reduced by 20%. Thus, it is expected that by using our approach to generate test input sequence, test time of I_{DDQ} tests can be reduced.



(a) Unfaulty circuit



(b) Faulty circuit

Fig.6 Test time reduction by our improved test input sequence.

5. Conclusion

In this paper, a test input sequence generation methodology for test time reduction of I_{DDQ} testing is proposed. Since I_{DDQ} appears after charge current disappears, some test input vectors are modified so that charge current can disappear quickly. The feasibility of the methodology is evaluated by some experiments. In the experiments, a 4-bit adder circuit is used as a CUT and fault coverage for bridging faults are examined. The empirical results show that test time of I_{DDQ} testing can be reduced by our approach for test input sequence generation. Also, they show that there are many kinds of heuristics to find such a test input sequence which can affect the test time. It is one of the future works to develop how to generate the most effective test input vector sequence.

References

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