IDDQ Testable Design of Static CMOS PLAs with Low Power Consumption

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Abstract: *In the past, we proposed an IDDQ testable design method for static CMOS PLA circuits. All bridging faults can be detected in NOR planes of our testable designed PLA circuits by IDDQ testing with 4 kinds of test input vectors which are independent of the logical functions to be realized. However, the testable designed PLA circuits consume large power in the normal operation. In this paper, a new IDDQ testable design method is proposed and evaluated by some experiments. The experimental results show that the PLA circuit designed with our method can work with low power consumption than the previous one.*

1.Introduction

In these years, it has been incident that bridging faults are generated in CMOS ICs fabricated with state-of-the-art technology. Bridging faults in CMOS ICs are very difficult to be detected by using logic testing, but they can be detected by measured supply current easier than by logic testing.

Programmable Logic Arrays(PLAs) are suitable for implementing logic functions in ICs since they have regular structure and many powerful CAD tools can be used for their optimization and synthesis. PLA ICs have been used for developing custom ICs, since they can be programmed by the IC users. Recently, PLA circuits have been used for embedding complicated logic functions in some ASICs.

Since PLA circuits are difficult to be tested, many kinds of testable design methods have been proposed for logic testing[1-3]. However, if a PLA circuits is fabricated by means of MOS technology, bridging faults in the circuits are very difficult to be detected by logic testing[4]. Since bridging faults can be more easily by IDDQ testing, some IDDQ testable circuits have been proposed[5].

PLA circuits can be classified into static PLA circuits and dynamic ones. Until now, IDDQ testable design methods for only dynamic PLA circuits have been proposed, since dynamic PLA circuits are more suitable than static ones for embedding logic functions in ICs. However, static PLA circuits have been often used. Thus, in the past, we proposed a testable static PLA design method[6]. We can test PLA circuits designed by using the method in [6] easily before and after programming.

However, the testable design method will generate PLA circuits, in which a large supply current will flow in the normal operation. As the result, the PLA circuits will consume large power in the normal operation. Also large noise, for example, the ground bound, will be generated and the circuit may generate some malfunction by the noise. Thus, we attempted to develop a new testable design method for static PLA circuits. In the method, additional MOS transistors are added to the ones in [6].

By the new testable design method, a testable designed PLA circuit can be designed, where quiescent supply current in the normal operation is smaller than the ones in [6]. In this paper, our new testable design method is described in section 3.

2. Targeted Faults

There are 4 types of static PLA circuits: NOR-NOR type, NAND-NAND type, NAND-NOR type and AND-OR type. PLA circuits of NOR-NOR type have been often used. In this paper, only PLA circuits of NOR-NOR type are discussed.

An example of static PLA circuits of NOR-NOR type is shown in Fig.1. PLA circuits of NOR-NOR type consist of 2 kinds of NOR planes. We call them "NOR_i" and "NOR_o" as shown in Fig.1.

Our targeted faults are bridging faults between neighboring signal lines in the NOR planes, since their planes occupy larger area than the others. Possible bridging faults in the planes can be classified into 8 categories, which are indicated in Fig.1 as F1, F2, F3, F4, F5, F6, F7 and F8. Faults of types F1, F2, F3 and F4 are bridging faults in the NOR_i plane. Other faults are bridging faults in the NOR_o plane.

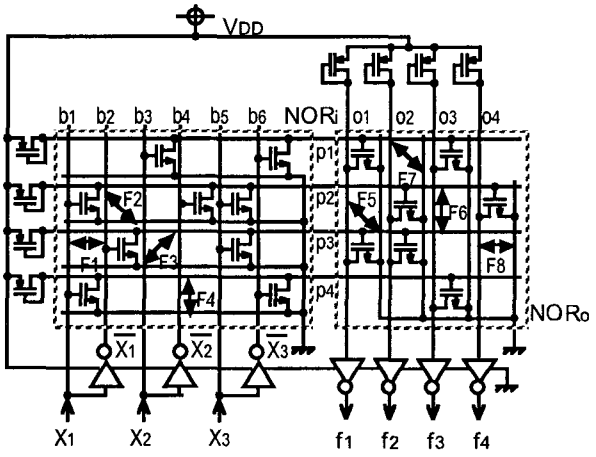


Fig.1 Bridging faults in NOR-NOR PLAs.

Faults of type F1 are bridging faults between a bit line(b_i) and the neighboring bit line(b_{i-1} or b_{i+1}). Faults of type F2 are bridging faults between a bit line and a GND line. Faults of type F3 are bridging faults between a bit

line and a neighboring product line. Faults of type F4 are bridging faults between a product line and a V_{DD} line. Faults of type F5 are bridging faults between an output line(o_i) and a neighboring product line. Faults of type F6 are bridging faults between a product line(p_i) and a neighboring one(p_{i-1} or p_{i+1}). Faults of type F7 are bridging faults between a product line and a GND line. Faults of type F8 are bridging faults between an output line(o_i) and a GND line.

In this paper, it is assumed that at most one bridging fault occurs in a PLA circuit. In logic tests of PLA circuits, the assumption is not adequate[5]. However, in IDDQ tests, the assumption can be validated. That is the reason why if more than one bridging fault occurs in a PLA circuit and are sensitized, larger quiescent supply current in the faulty circuit will be generated than in unfaulty ones and the faults can be detected by the test vectors generated under the assumption.

3. Testable Design

Many kinds of supply current test methods have been proposed. In this paper, a testable design is discussed for a conventional IDDQ test method. In the conventional IDDQ test, if Eq.(1) is satisfied in any test input vector application, the circuit to be tested is determined as faulty.

$$I_{DDQC} - I_{DDQN} \geqq I_{th} \quad (1)$$

where I_{DDQC} and I_{DDQN} are the measured quiescent supply current of the circuit and the quiescent supply current of unfaulty circuits, respectively. I_{th} is the threshold value, which is determined from the variation of quiescent supply current of unfaulty circuits. Since I_{DDQN} is nearly zero in CMOS circuits, Eq.(2) is used in IDDQ tests.

$$I_{DDQC} \geqq I_{th} \quad (2)$$

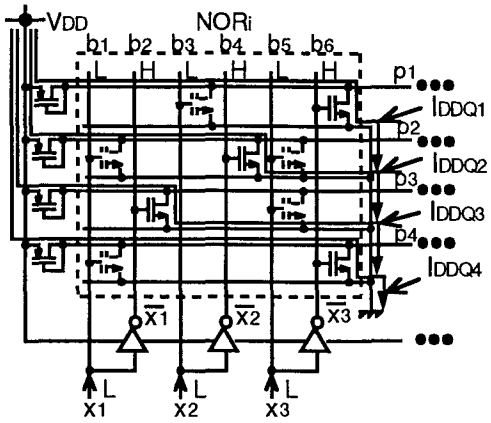
In conventional static PLAs, large quiescent supply current flows in operation. For example, when low(L) level signal is provided to x_1, x_2 and x_3 of the PLA circuit in Fig.1, 4 kinds of supply current paths will appear as shown in Fig.2(a). If the circuit has a bridging fault of type F1 as shown in Fig.2(b), the fault is sensitized by the input vector and logic level of b2 will change from high(H) level to L. By the logic level change, the current path of I_{DDQ3} will disappear and the one of I_{DDQ5} will appear as shown in Fig.2(b). If the difference between supply current in Fig.2(a) and the one in Fig.2(b) can be generated, the bridging fault can be detected by using Eq.(1).

In order to detect bridging faults by IDDQ testing, they must be sensitized. In order to sensitize a bridging fault, contrary logic values should be provided to the bridged signal lines. In Fig.2(b), H and L levels are provided to the bridged signal lines. Thus large quiescent supply current will be generated when x_1=L is provided.

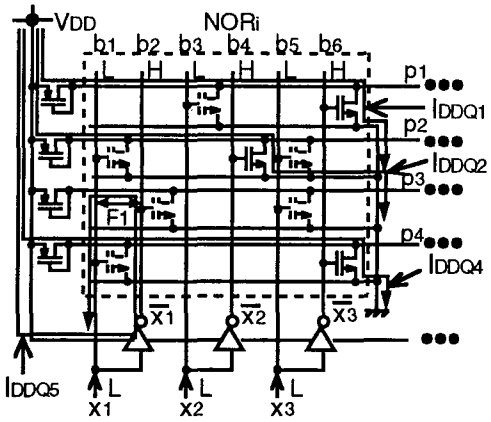
However, the fault may not be detected by IDDQ testing. The fault can be detected if and only if Eq.(3) is satisfied.

$$I_{DDQ5} - I_{DDQ3} \geqq I_{th} \quad (3)$$

It means that a bridging fault can not be always detected by IDDQ testing even if it is excited. In order to detect it only by the excitation, the circuit should be designed so that any IDDQ can not flow when unfaulty circuits are tested. Thus, we attempted to develop how to design a PLA circuit so that IDDQ can not flow whenever the unfaulty PLA circuit is tested.



(a)Unfaulty circuit



(b)Circuit having fault of type F1

Fig.2 Supply current paths in PLAs.

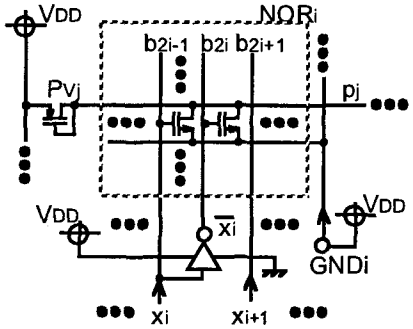
Also, IDDQ testing requires larger test time than logic testing, since it must be postponed to measure supply current until dynamic current disappears. Thus, a large number of test input vectors are not practical for IDDQ testing. On the other hand, since logic functions implemented in PLA circuits are very complicated, a large number of test input vectors are needed generally to test them. Therefore, we attempted to develop a design method of PLA circuits which can be tested with a small number of test input vectors.

In our testable design, two kinds of methodologies are used, which are shown in Fig.3, so as for IDDQ not to flow in the tests of unfaulty circuits. A GND terminal is added for the NOR_i plane, which is referred to as GND_i. By applying power supply voltage V_{DD} to GND_i in the test as shown in Fig.3(a), any quiescent supply current can not flow, since the potential of the source terminal is equal to the one of the drain terminal in each nMOS transistor even if H level voltage is provided to the gate terminal.

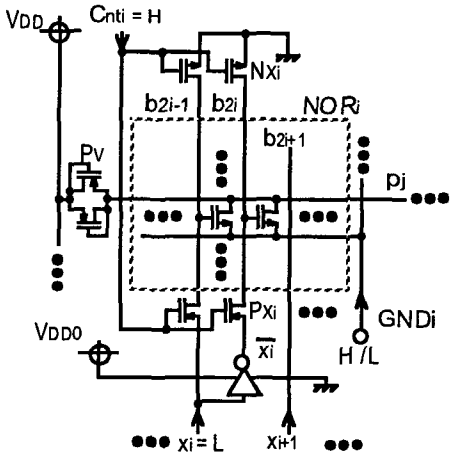
Another circuitry used in our testable design is shown in Fig.3(b). As shown in Fig.3(b), a complementary switch is inserted into each complementary input bit line(b_i), which consists of Nbi and Pbi and is controlled by Cnt_i. When Cnt_i is L level, specified outputs can be obtained from the PLA circuit. When Cnt_i is H level, the bit line connecting to a

complementary switch can be set to GND(L) level. By providing Cnt_i=H for all input signals, all of the nMOS transistors can be in the cutoff state. It means that any quiescent supply paths in NOR_i plane can not be generated by the application and the logic values of product lines can be controlled by the signal applied to the V_{DD} terminal.

By these modifications, quiescent supply current can not flow if any bridging faults do not occur in the NOR_i plane. Besides these modifications, pull-up transistor P_{Vi}'s are modified so that current can flow from the NOR_i plane to the V_{DD} terminal and vice versa as shown in Fig.3(b).



(a)V_{DD} application to GND_i terminal



(b)Insertion of complementary switch

Fig.3 Testable design of NOR_i plane.

Our IDDQ testable PLA, whose logical function is the same as the one in Fig.1, is shown in Fig.4. The circuit in Fig.4 is designed so that if and only if any faults do not occur in the circuit, quiescent supply current of the circuit can be zero when it is tested.

4. IDDQ Test for Our Testable Designed PLAs

When our testable PLA circuit is tested, 4 kinds of test input vectors shown in Table 1 are applied to the circuit and the quiescent supply current supplied from a V_{DD} voltage source is measured as I_{DDQC}. If Eq.(2) is satisfied, the circuit is determined as faulty.

When the PLA circuit is not tested, L level signal is provided to Cnt_i, Cnt_o and GND_i, and H level signal is provided to V_{DD1}, V_{DD2} and V_{DD3}. By providing them to the terminals, outputs of the programmed Boolean functions can be obtained from the output terminals.

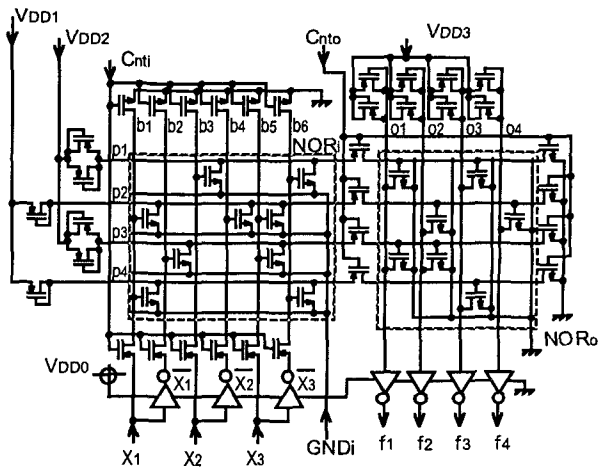


Fig.4 IDDQ testable PLA.

Table 1 Test vector and excited faults.

test vector	V_{DD1}	V_{DD2}	GND_i	Cnt_i	V_{DD3}	GND_o	Cnt_o	X_1,X_2,X_3	detectable faults
#1	H	H	H	L	L	L	L	L	F1,F2,F3,
#2								H	F5,F7
#3	H	H	L	H	H	L	H	L	F2,F3,F4, F5,F8
#4	H	L	H	H	L	L	L	L	F2,F6

An example of voltage supply circuits for our testable PLA circuits is shown in Fig.5. Our testable PLA circuits can be tested by providing the test vectors shown in Table 2 to this voltage supply control circuit. IDDQ is measured as quiescent supply current from a V_{DD} voltage source to the voltage supply control circuit. The required Boolean functions of our testable PLA circuits can be obtained by providing H level to both Test1 and Test2.

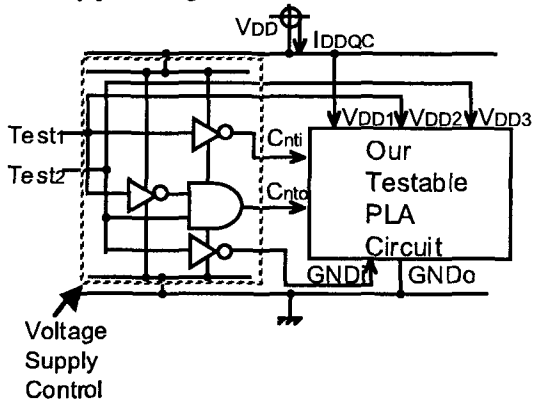


Fig.5 Voltage supply control circuit.

Table 2 Primary input vector for voltage supply control circuit.

oreration mode	Test1	Test2
test for vector #1,#2	H	L
test for vector #3	L	H
test for vector #4	L	L
without testing	H	H

5. Evaluation by Experiments

In order to evaluate our testable design method, we insert single bridging faults in the SPICE file of the unfaulty circuit in Fig.4. Quiescent supply currents of the circuit

in Fig.5, which consists of the voltage supply control circuit and the PLA circuit in Fig.4, are obtained by circuit simulation. The IDDQ of the unfaulty PLA circuit for each test input is 0.000mA. The number of inserted bridging faults is 102.

The minimum value and the maximum one in the obtained IDDQs of faulty circuits for each fault type are denoted in Table 3. As shown in Table 3, the minimum values are greater than the IDDQ of the unfaulty circuit. i.e. 0mA. Thus, it is found out from Table 3 that all faults can be detected by the IDDQ test based on Eq.(2) with 4 kinds of test input vectors in Table 1. The test input vectors are independent of implemented Boolean functions.

There may be some degradation of operation speed in the normal operation, since MOS transistors are added to the paths from input terminals of the PLA circuit in Fig.1. However, any degradation could not be observed in our experiments.

Table 3 IDDQ in fault excitation

Fault type	# of faults	IDDQ [mA]	
		minimum	maximum
F1	5	1.292	1.343
F2	24	0.414	0.549
F3	24	2.366	2.366
F4	7	1.418	0.553
F5	16	0.414	0.500
F6	3	0.168	0.168
F7	16	0.414	0.500
F8	7	0.568	0.568

Our testable design requires to add only complementary switches for all bit lines to conventional PLA circuits. Thus, area overhead for our testable design of PLA circuits will be generated. Furthermore, our testable designed PLA circuit requires a voltage supply control circuit. The control circuit occupies some additional area. Since conventional PLA circuits do not require the circuit, the area overhead will be generated in our testable PLA design, like the previous method in [6].

We examined the power consumption of our previous designed PLA circuit in [6], besides the ones in Fig.1 and Fig.4. The results are shown in Table 4. It is expected from Table 4 that the quiescent supply current in the normal operation can be reduced in our new testable designed PLA circuits.

Table 4 IDDQ in the normal operation

Input vector (X1,X2,X3)	IDDQ [mA]		
	Conv.PLAs	PLAs in [6]	ThisPLAs
(L,L,L)	0.926	1.955	1.109
(L,L,H)	0.996	1.129	1.101
(L,H,L)	1.553	1.522	1.263
(L,H,H)	0.941	1.319	1.093
(H,L,L)	1.187	1.465	1.251
(H,L,H)	1.165	1.454	1.233
(H,H,L)	1.187	1.459	1.249
(H,H,H)	0.958	1.728	1.134

6. Conclusions

In this paper, an IDDQ testable design method is proposed for static CMOS PLA circuits. The design method enables us to test designed circuits with 4 test vectors, which are independent of the logic functions implemented in PLA circuits. Since any IDDQ does not flow when the unfaulty circuits designed by our method are tested, bridging faults can be detected by IDDQ testing with high resolution.

In order to evaluate the method, a PLA circuit of NOR-NOR type has been designed. Fault coverage of bridging faults in the circuit is examined by circuit simulation. As the result, it is shown that all bridging faults can be detected by IDDQ testing with 4 test vectors. Also, it is shown that the power consumption of our testable designed PLA circuits is smaller than one of the previous method in [6]. The result promises us that our testable design method can be used in practical IC design.

It has not been examined how much area overhead is generated in our testable designed PLA circuits. It is the future works to examine the area overhead.

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