CMOS-Based Fuzzy Operation Circuit Using Binary-Coded Redundantly-Represented Positive-Digit Numbers

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Abstract : It is possible to perform the digital, fuzzy logical high-speed and high-precision computation by the use of redundantly-represented binary positive-digit number arithmetic operation. In this paper, as basic operation circuits in the fuzzy logic, new voltage-mode 4-valued binary parallel processing operation circuits using positive redundantly-expressed binary-coded numbers is discussed.

1. Introduction

In fuzzy logical operation, undefined fuzzy information are dealt with, these are numerized by fuzzy grades of membership function made up with all real numbers between 0 and 1, inclusive.

Therefore, latest fuzzy arithmetic does not execute using a conventional software approach by binary digital computer, but many analog circuits are frequently often used for a real-time and high-speed fuzzy logical operation [1-2].

However, in compact analog fuzzy circuits, the error due to analog signal processing may arise immediately, for this reason, this leads to a problem of poor precision computation.

On the other hand, the redundant binary number addition method can be effective to perform operations at a very high speed for large massive binary data [3-4]. Because the carry transfer is limited to only one process between present digit and higher order digit which enables us to obtain a constant operation time regardless of various digit-lengths.

To solve the problem of the complex addition algorithm, we have realized a current-mode CMOS-based 5-valued 4-radix adder circuit with the positive, minimum redundant code representation [5]. Moreover, we have realized a current-mode fuzzy logical operation circuits for logical computation between two redundantly-represented 5-valued 4-radix positive digit (PD) numbers which express fuzzy grades of membership functions for avoiding errors arising from analog calculation in the conventional analog fuzzy hardware systems [6].

However, these available current-mode fuzzy circuits have originally shortcomings; current-mode circuits need highly skilled circuit designing techniques and analog processing error still may be produced.

Based on these facts, in this paper concerning a high-speed fuzzy operation method, we propose to express fuzzy grades in the form of new voltage-mode binary-coded redundant 4-valued binary PD numbers [7].

We construct new operation circuits for logical product, logical sum, bounded sum, bounded difference, and bounded product based on CMOS logical combinational switches, which can also be achieved the faster operation time than conventional current-mode fuzzy operation circuits. It can be expected to improve the precision computation remarkably and also to give a guarantee on the high execution speed by using the parallel processing of fuzzy logical operations.

2. The discrimination of inequality for redundantly-represented PD numbers

The fuzzy grades $\mu_A(x)$, $\mu_B(x)$ of two membership functions which correspond to same member variable x are constituted the disconnected set of many singletons.

All logical digit values of redundant 4-valued 2-radix PD numbers are represented by non-redundant binary-coded 2-bits numbers, logical digit values of digit $a_i = [a_{i1}\ a_{i0}]$, digit $b_i = [b_{i1}\ b_{i0}]$, and both singletons are expressed by the form of Equations (1) and (2).

$$\mu_A(x) = [\,0.\ a_{-1}\,a_{-2}\cdots a_{-n+1}\,a_{-n}\,]_2^{PD} = \sum_{i=1}^{n} (a_{-i}\,2^{-i}) \qquad (1)$$

$$\mu_B(x) = [\,0.\ b_{-1}\,b_{-2}\cdots b_{-n+1}\,b_{-n}\,]_2^{PD} = \sum_{i=1}^{n} (b_{-i}\,2^{-i}) \qquad (2)$$

Each digit a_i and b_i of two numbers contains two redundant logical values "2" and "3" express as follows;

$$a_i,\ b_i \in \{\ 0,\ 1,\ 2,\ 3\ \} \qquad (3)$$

The logical values of linear deference $a_i - b_i$ in each digit is contained by

$$a_i - b_i \in \{\ -3, -2, -1, 0, 1, 2, 3\ \} \qquad (4)$$

In the complement addition between two redundantly-represented PD numbers, we try to convert the result of complement addition $\mu_A(x) + 1 - \mu_B(x)$.

In case of 4-valued binary PD numbers, each digit value of linear summation between minuend a_i and 2's complement of subtrahend $1 - b_i$ contain logical values as follows.

$$a_i + 1 - b_i \in \{\ -2,\ -1,\ 0,\ 1,\ 2,\ 3,\ 4\ \} \qquad (5)$$

From half addition of augend a_i and complement $1 - b_i$, redundant carry c_i and intermediate sum w_i are obtained in

Equation (6).

$$a_i + 1 - b_i = 2c_i + w_i \quad (6)$$

Here, intermediate sum w_i has to take digit value "2" or "3" to obtain positive digit values of final result u_i. The new algorithm rules for complement addition are shown in equation forms below.

When $a_i + 1 - b_i = 4$, then $c_i = 1, w_i = a_i - b_i - 1$ (7-1)

When $3 \geq a_i + 1 - b_i \geq 2$, then $c_i = 0, w_i = a_i - b_i + 1$ (7-2)

When $1 \geq a_i + 1 - b_i \geq 0$, then $c_i = -1, w_i = a_i - b_i + 3$ (7-3)

When $-1 \geq a_i + 1 - b_i \geq -2$, then $c_i = -2, w_i = a_i - b_i + 5$ (7-4)

Then intermediate sum w_i and redundant carry c_i contain these logical values as follows.

$$w_i \in \{ 2, 3 \}, \quad c_{i-1} \in \{ -2, -1, 0, 1 \} \quad (8)$$

However, the relation among linear complement sum $a_i + 1 - b_i$, redundant carry $c_i = [\ c_{i1}\ c_{i0}\ ]$ and non-redundant intermediate sum $w_i = [\ w_{i1}\ w_{i0}\ ]$ in half complement addition are actually obtained in Equation (9).

$$a_i + 1 - b_i = 2(2c_{i1} + c_{i0}) + w_{i0} + 2 \quad (9)$$

Then, from the full complement addition of intermediate sum w_i and carry $c_{(i-1)0}$, $c_{(i-2)1}$ from lower digits, the logical digit values of final complement sum $u_i = [\ u_{i1}\ u_{i0}\ ]$ is expressed by the form of Equation (10).

$$u_i = w_{i0} + 1 + c_{(i-1)0} + c_{(i-2)1} \quad (10)$$

Then, final sum u_i represented by positive redundant sign does not produce any output carry.

$$u_i = [\ u_{i1}\ u_{i0}\ ] \in \{ 0, 1, 2, 3 \} \quad (11)$$

minuend: a_i		1	1	3	3	1	0	1	(2)
2's complement :	+	1	1	1	1	1	1	1	(2)
subtrahend: b_i	−	2	0	3	2	1	2	1	(3)
halfway sum: w_{i0}		0	1	1	0	1	1	1	1
carry: c_{i0}	1	0	1	0	1	0	1	1	
$w_{i0}+c_{i1}$	0	1	0	1	0	0	0	0	
final sum: u_{i0}		0	0	1	1	1	1	0	0	1
final sum: u_{i1}	1	0	1	0	0	0	1	1	0	

Fig. 1 An example of PD complement addition process.

The simplified Boolean expression for logical operation is obtained as shown in Equations. (12) -(14).

$$w_{i0} = a_{i0}\overline{b_{i0}} + \overline{a_{i0}}b_{i0} \quad (12)$$

$$c_{i0} = a_{i1}\overline{b_{i1}}b_{i0} + a_{i1}\overline{a_{i0}}b_{i1} + \overline{a_{i1}}a_{i0}\overline{b_{i1}} + \overline{a_{i1}}\,\overline{b_{i1}}b_{i0} + \overline{a_{i1}}a_{i0}b_{i1}\overline{b_{i0}} + a_{i1}a_{i0}\overline{b_{i1}}\,\overline{b_{i0}} \quad (13\text{-}1)$$

$$c_{i1} = a_{i1}b_{i1} + a_{i0}\overline{b_{i1}}\,\overline{b_{i0}} + a_{i1}a_{i0}b_{i1} \quad (13\text{-}2)$$

Similarly, the Boolean expression for logical operation is obtained by following equations.

$$u_{i0} = c_{(i-2)1}c_{(i-1)0} + w_{i0}c_{(i-1)0} + w_{i0}c_{(i-2)1} \quad (14\text{-}1)$$

$$u_{i1} = w_{i0}\overline{c_{(i-2)1}}\,\overline{c_{(i-1)0}} + \overline{w_{i0}}\,c_{(i-2)1}c_{(i-1)0} + w_{i0}\overline{c_{(i-2)1}}c_{(i-1)0} + \overline{w_{i0}}\,\overline{c_{(i-2)1}}\,\overline{c_{(i-1)0}} \quad (14\text{-}2)$$

In the redundantly-expressed binary PD number system different from the normal binary notation, it is difficult to discern the inequality of two numbers by checking the value in the most significant digit of the linear deference of numbers.

To compare the size of fuzzy grades of two membership functions, all digits have to be checked the logical values which are among in three groups. The logical values are divided into three groups, values of 0, value of 1, and values of above 2.

When the end-around carry is existing or the most significant digit u_{-1} takes redundant logical values; 2 or 3, the fuzzy grade $\mu_A(x)$ is larger than the fuzzy grade $\mu_B(x)$. When the end-around carry does not exist and the most significant digit u_{-1} takes logical value of 0 , the fuzzy grade $\mu_A(x)$ is smaller than the fuzzy grade $\mu_B(x)$.

However, the end-around carry does not exist and if the most significant digit u_{-1} takes logical values of 1, the inequality of the two fuzzy grades between $\mu_A(x)$ and $\mu_B(x)$ is determined by consecutively lower digit values.

If the consecutively one or more lower digits take negative redundant value 2 or 3, , the fuzzy grade $\mu_A(x)$ is larger than the fuzzy grade $\mu_B(x)$.

If $3 \geq u_{-1} \geq 2$, $(\mu_A(x) > \mu_B(x)$

then $\max(\mu_A(x), \mu_B(x)) = \mu_A(x)$ (15-1)

If $u_{-1} = 0$, $(\mu_A(x) < \mu_B(x)$

then $\max(\mu_A(x), \mu_B(x)) = \mu_B(x)$ (15-2)

If $u_{-1} = 1$, then $a_{-1} = b_{-1}$ therefore

$\max(\mu_A(x), \mu_B(x))$ is depended on u_{-2} (15-3)

3. The logical product and logical sum for fuzzy grades of membership functions

3. 1 The complement addition circuit for PD numbers

Figure 2 shows the block diagram of binary-coded 4- valued 2-radix PD number algebraical operation.

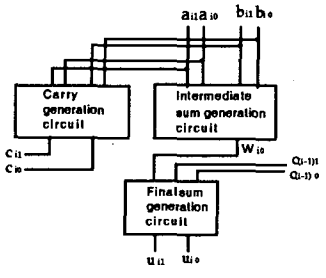

Fig. 2 Block diagram of algebraical operation part.

Figure 3 shows a circuit diagram of a new voltage-mode CMOS-based complement addition circuit for 4-valued binary PD numbers, which has comprised by logical combinational circuit, which is composed of NOT circuits and NAND circuits. The output result are obtained 4-valued binary numbers which are contained only two positive redundant logical values according to the simplified Boolean expressions (12)-(14) in the algorithm process of the complement addition.

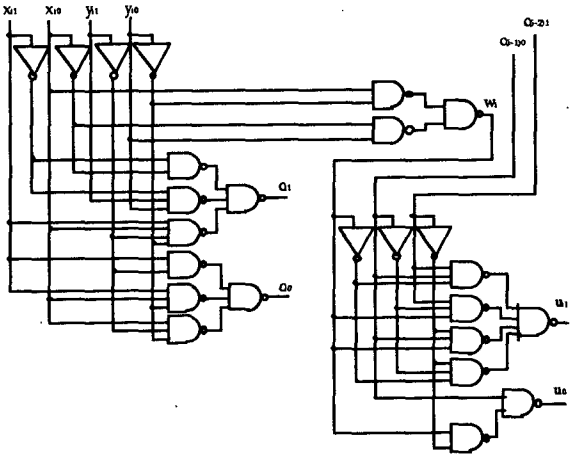

Fig. 3 The complement addition circuit structure for PD numbers.

3. 2 The MAX / MIN discrimination circuit for PD numbers

Figure 4 shows the block diagram of logical operation for two redundant binary PD numbers.

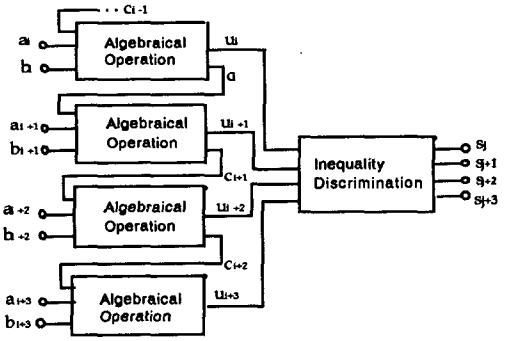

Fig. 4 Block diagram of fuzzy operation for PD numbers.

As shown in Figure 5, we constructed a new CMOS-based maximum discrimination circuit to comparing the size of fuzzy grades represented by 4-valued binary PD numbers, which has comprised by voltage-mode logical combinational circuits.

In the complement addition circuit, when the logical value of final sum u_i is more than 2, that is, u_{i1} takes value of 1 input voltages v_x and v_y of the maximum discrimination circuit becomes low and when the value of u_i is smaller than 2, input voltages v_x and v_y becomes high. When the input z_i is larger than respectively 0 or 2, the output values of individual threshold detectors become 1.

On the other hand, a minimum discrimination circuit can be easily constructed by exchanging the types of a voltage-controlled switch transistors.

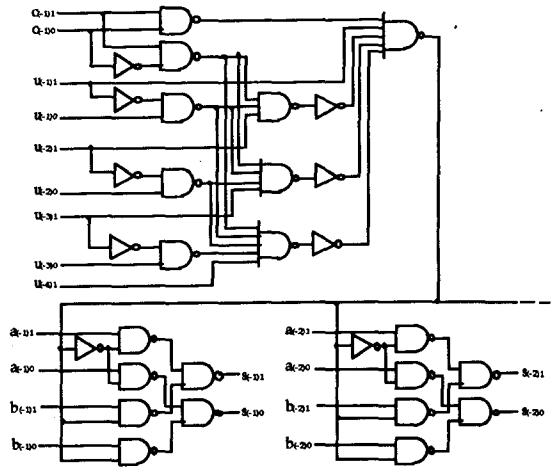

Fig. 5 The maximum discrimination circuit structure for 4-figures redundant binary PD numbers.

4. The fuzzy bounded sum, bounded difference, and bounded product

As the typical fuzzy logical operations, there are bounded sum $A \oplus B$, bounded difference $A \ominus B$, bounded product $A \odot B$ which are expanded from algebraical sum $A+B$, algebraical difference $A-B$, algebraical complement difference $A+B-1$ defined by following equation forms respectively.

$$\mu_{A \oplus B}(x) = \min(1, \mu_A(x)+\mu_B(x)) \quad (16\text{-}1)$$

$$\mu_{A \ominus B}(x) = \max(0, \mu_A(x)-\mu_B(x)) \quad (16\text{-}2)$$

$$\mu_{A \odot B}(x) = \max(0, \mu_A(x)+\mu_B(x)-1) \quad (16\text{-}3)$$

These results, which is expressing fuzzy grades, are limited to 4-valued binary PD numbers between 0 and 1.

4. 1 The bounded sum for redundant PD numbers

Addend a_i and augend b_i in each digit of two redundant PD numbers which express fuzzy grades $\mu_A(x)$, $\mu_B(x)$ contain two redundant logical values 2 and 3. Therefore, the linear summation $a_i + b_i$ in each digit include the following logical values.

$$a_i + b_i \in \{0, 1, 2, 3, 4, 5, 6\} \quad (17)$$

The algorithm processes of half addition are shown in equation forms below.

$$a_i + b_i = c_i + w_i = 2(2c_{i1} + c_{i0}) + w_{i0} \quad (18)$$

$$w_i \in \{0, 1\},\ c_{i-1} = [c_{(i-1)1}\ c_{(i-1)0}] \in \{0, 1, 2, 3\} \quad (19)$$

Then, from the full addition of intermediate sum and carry from the lower digit, final sum represented by 4-valued binary PD numbers does not produce any output carry.

$$u_i = w_i + c_{(i-1)0} + c_{(i-2)1} \quad (20)$$

$$u_i = [\, u_{i1}\ u_{i0} \,] \in \{ 0, 1, 2, 3 \} \quad (21)$$

When number of $\mu_A(x)+\mu_B(x)$ exceeds 1, bounded sum is limited to 1 by utilizing the minimum discrimination circuit which is comparing the size between $\mu_A(x)+\mu_B(x)$ and 1.

4. 2 The bounded difference for redundant PD numbers

The summation between minuend a_i and 2's complement of subtrahend 1-b_i in each digit is executed accoding to the complement addition process expressed by Equations (9) and (10).

4. 3 The bounded product for redundant PD numbers

The subtraction between addend a_i and 2's complement of augend 1-b_i in each digit is executed. Similarly, whether the bounded product $\mu_A(x)+\mu_B(x)$ -1 is larger than 1 or not can be determined by the same way in case of the bounded difference.

5. Ability evaluation

The characteristics of the fuzzy operation circuits are simulated by using general circuit simulation software, SPICE. The SPICE model parameters of the enhancement type PMOS and NMOS transistors are based on 0.5 μm MOSIS CMOS technology. The logical value 1 in the adder is standardized by the voltage value 3 [V]. We confirm the performances of the circuits .

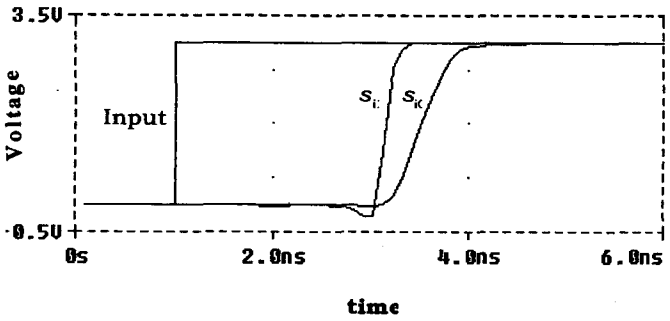

Fig. 6 Transient characteristics of the redundant PD number complement addition circuit

Figure 6 shows a predictable result of the connection between the linear addition of inputs for the intermediate sum output currents in redundant PD number addition circuit.

From the transient characteristics of the maximum discrimination circuit, by the measured results, the average turn-on time becomes about 1.2 [ns].

6. Conclusion

We have realized fuzzy logical operation circuits which are possible to perform the parallel processing by the use of redundantly-represented binary-coded PD numbers in computation of the fuzzy grades of membership functions.

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