A Proposal on Fast Pull-in PLL with Clock Count Type Frequency Detector

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Abstract : In this paper, we proposed a PLL with the clock count type frequency detector, in which the very fast pull-in time can be realized by resetting the VCO at the rising of input signal after charging the capacitor of loop filter with the voltage corresponding to the frequency of the input signal.

1. Introduction

The phase locked loop (PLL) is a circuit to obtain an output signal for which the phase and frequency coincide with that of the input signal. It is applied to various fields such as the demodulation of FSK and FM signals, frequency synthesizers, control of motor's rotation, timing sampling of all sorts of communication systems, and so on [1].

In these applications, the PLL using as the timing sampling circuit in the high-speed digital communication is required for the fast pull-in and the stable operation (low-jitter). Several methods have been proposed for the realization of these two requirements. Switching the time constant of the loop filter or the gain of the phase detector by the pull-in state and the stable state [2], charging the capacitor of the loop filter by sensing the cycle slip [3], and using the frequency-difference-detector are some of those methods [4]. However, since these methods require more than ten periods of the input signal to pull-in, the development of a better fast pull-in PLL is strongly expected.

In this paper, we proposed a PLL with the clock count type frequency detector [5], in which the very fast pull-in time can be realized by resetting the VCO at the rising of input signal after charging the capacitor of loop filter with the voltage corresponding to the frequency of the input signal. Since the proposed PLL is able to perform the pull-in process in first two periods of the input signal and can realize stable operation subsequently, it is very useful as timing sampling PLL in the high-speed digital communication systems.

2. Circuit Configuration And Analaisys of Operation

2.1 Circuit Configuration of Proposed PLL

Fig.1 shows block diagram of a PLL with the clock count type frequency detector. Fig.2 shows the block diagram of the clock count type frequency detector. This frequency detector has constituted by the T-flip flop (T-FF), the gate circuit, the up counter (Up-C), the D/A converter and the comparison circuit as shown in Fig.2. Here the D/A converter contains the memory

circuit within itself. The comparison circuit ratches the number of the fixed clock that passes during each period of the input and the output signals, and if frequency difference occurs between the input and the output signals, it outputs the control signal of the switch Sw and the reset pulse generator (RPG).

2.2 Pull-in Principle of Proposed PLL

If the voltage-frequency conversion function of the VCO in this PLL is $VCO(x)$, then the characteristic function of the VCO is

$$f_{VCO} = VCO(x) \tag{1}$$

If the PLL detects the voltage corresponding to the frequency f_{in} of the input signal and instantly gets the frequency locked, then the input voltage setting of the VCO is

$$V_o^{'} = VCO^{-1}(f_{in}) \tag{2}$$

where $V_o^{'}$ is a input voltage of the VCO for the frequency f_{in} of the input signal and VCO^{-1} is the inverse function of the VCO. If the frequency of the fixed clock is f_x and the number of the fixed clocks that pass during one period of the input signal are N_{in}, then f_{in}, f_x and N_{in} form the following equation.

$$f_{in} \cong \frac{f_x}{N_{in}} \tag{3}$$

From (2) and (3), the input voltage of the VCO corresponding to certain N_{in} is

$$V_o^{'} = VCO^{-1}\left(\frac{f_x}{N_{in}}\right) \tag{4}$$

Hence, if it is given a definition that the function of g is $g(x) = f_x / x$, then (4)

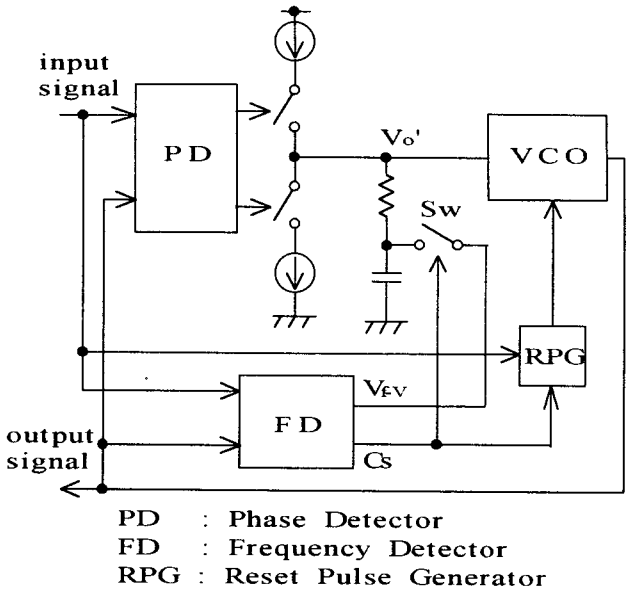

Fig.1 Block diagram of the proposed PLL.

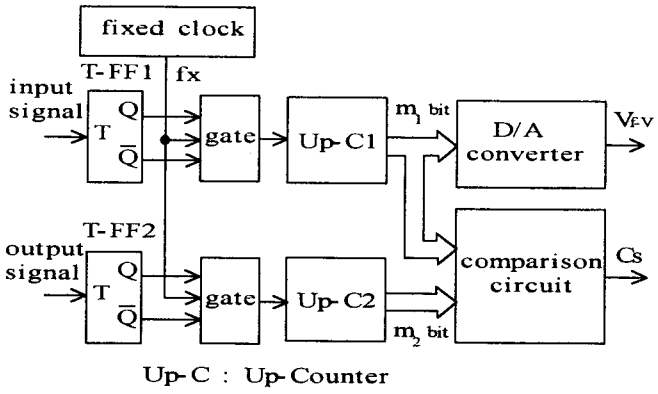

Fig.2 Block diagram of the FD.

becomes

$$V_o^{'} = VCO^{-1}(g(N_{in})) \tag{5}$$

When the combined function of VCO^{-1} and g is H, (5) becomes

$$V_o^{'} = H(N_{in}) \tag{6}$$

Therefore, this PLL can obtain the fast pull-in by memorizing the value that realizes the function H.

2.3 Pull-in Operation of This PLL

Fig.3 shows the waveform of the proposed PLL in case of applying the

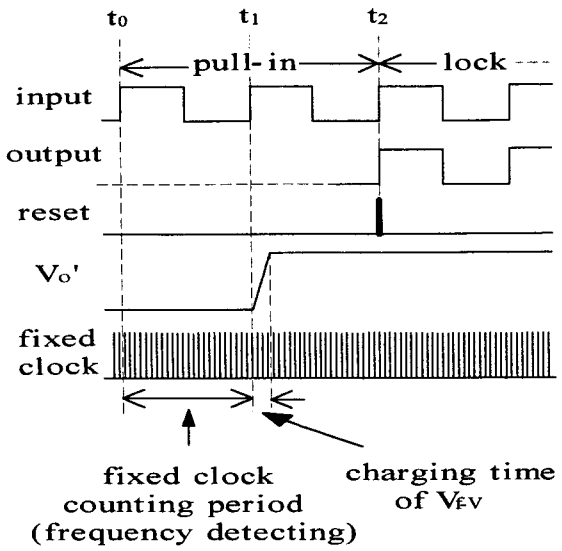

Fig.3 Process of pull-in.

difference input signal. When the input signal enters the PLL at time t_0, the Up-C1 counts the number of the fixed clock that passes during the one period of the input signal. The same the Up-C2 that counts the number of the fixed clock during one period of the output signal. After counting the number of the fixed clock at time t_1, each output value of the Up-C1 and the Up-C2 is transferred respectively to the D/A converter and the comparison circuit. Then, According to the value of the counter, the D/A converter outputs a voltage corresponding to the frequency of the input signal. And when the frequency difference occurs between the input and the output signals, the comparison circuit outputs the control signal. Simultaneously at this point, the loop filter's capacitor is instantly charged by the output voltage of the D/A converter. So, the frequency difference of the input and the output signals get removed at this point of time. Next, after removing the frequency difference, the rising of the next input signal resets the VCO, by which the loop starts to operate with the agreement between the phases of the input and the output signals. Therefore, the input and the output signals get locked state as the phase error between the input and the output signals is removed at time t_2.

In the conventional fast pull-in PLLs, the charging time of the loop filter's capacitor affects the pull-in time of the PLL. But, in the proposed PLL, charging time doesn't affect the pull-in time since the capacitor is charged between the frquency detecting of the input signal and the output of the reset signal.

2.4 Suppressed Effect of Cycle Slip

In the conventional PLL, when the input and the output signals have large frequency error and consequently the phase error exceeds $\pm \pi$, then the phase error causes oscillation. This phenomenon is called cycle slip. The PLL's pull-in time increases very much due to the cycle slip. But, as the proposed PLL performs the pull-in with the frequency detector, so the cycle slip doesn't affect the pull-in time.

3. Simulation results

We confirmed the operation of this loop by using the circuit simulator Pspice. Table.1 shows the condition of this simulation.

Fig.4 shows the simulation result of the proposed PLL in case of applying the difference input signal. It is found that since the proposed PLL finishes the pull-in operation at 2 periods of the input signal, its pull-in time is very fast. After the pull-in operation, it is also found that its operation is very stable.

Fig.5 shows the simulation result of suppressed effect of the cycle slip in the proposed PLL. It is found that when the

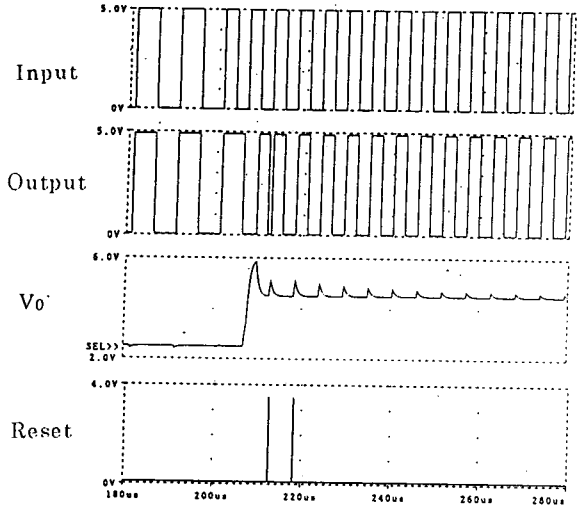

Fig.4 Simulation result of the proposed PLL.

conventional PLL can't finish the pull-in by occurring the cycle slip, the proposed PLL already finishes the pull-in. Hence, the proposed PLL can realize the fast pull-in in case that the input and the output signals have large frequency error.

4. Conclusions

In this paper, we proposed a reset type PLL with the clock count type frequency detector. The pull-in of this PLL is 2 periods of the input signal. Hence, this PLL can realize very fast pull-in time. Also, after the pull-in operation, its operation is very stable. Furthermore, it is confirmed that this PLL is able to suppress the cycle slip.

References

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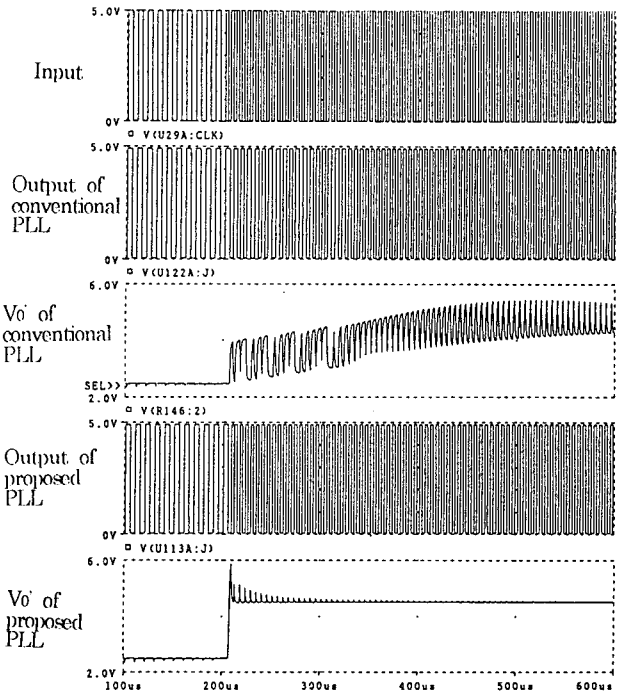

Fig.5 Simulation result of suppressed effect of the cycle slip.

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