Power Supply Circuits with Small size for Adiabatic Dynamic CMOS Logic Circuits

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Abstract: Adiabatic dynamic CMOS logic circuits, which are called ADCL circuits, promise us to implement low power logic circuits. Since the power supply source for ADCL circuits had not been developed, we proposed a power supply circuit for them. It is shown experimentally that by using the power supply circuit, ADCL circuits can work with lower power consumption than conventional static CMOS circuit. In this paper, the power supply circuit is improved so that the power consumption can be reduced. Also, it is shown by some experiments that by using the circuit, ADCL circuits can work with lower power consumption than before improving.

1. Introduction

Since quiescent power consumption of CMOS gates is very low, CMOS gates have been often used in the circuits, for which low power consumption is strongly requested. However, whenever output logic value of a CMOS gate is changed, dynamic supply current will flow to the GND terminal. Thus, some power will be consumed by the supply current at the switching of output logic value. Also, when the output changes from H to L, the charge stored in the load capacitance of the gate will be dissipated since the output of the gate is connected to the GND terminal. As the result, power consumption P of the gate is expressed as $f_{CLK} \cdot Pt \cdot CL \cdot V^2DD$, where f_{CLK} is the frequency of the output change and pt is the probability of the switching.

Many kinds of techniques to reduce the power consumption have been proposed[1-3]. Some practical dynamic CMOS logic gates for adiabatic logic circuits have been proposed [1]. The gates proposed in [2] and [3], which are referred to as "ADL" gates and "ADCL" gates respectively, promise us to implement a large size of CMOS digital circuit whose power consumption is very small.

ADCL circuits require a time variable voltage supply, which generates a sine waveform or triangle one. However, since any supply circuits for such circuits had not been developed, we proposed a power supply circuit for ADCL circuits[4]. Also we showed that by using the power supply circuit, ADCL circuits can work with low power consumption.

The power supply circuit in [4] can be simplified. Since low power circuits are requested for battery operated equipment like celler phone, book sized computer and so on. The equipment requires small size of power circuits. Thus, we attempted to improve it.

In section 2, power supply circuit for ADCL gates are introduced. In section 3, power supply circuits with small size are proposed. In section 4, power supply circuits with small size is evaluated by some experiments.

2. Our Power Supply Circuit in [4]

An ADCL inverter gate is shown Fig.1. Since the output voltage of an ADCL gate synchronize with VDD(t), the speed of ADCL circuits is dominated by the frequency of supply voltage VDD(t). In order to operate in adiabatic mode with high speed, a power supply source is necessary which enables that the energy stored in permissive capacitors(Cp's) between gates will be recycled with high speed. However, any power supply circuits for ADCL circuits had not been proposed. Thus, we developed a power supply circuit for ADCL circuits[4].

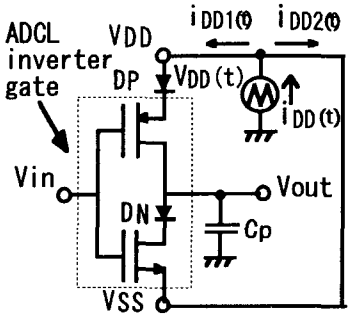


Fig.1 ADCL inverter gate(ADCLINV1)

The proposed circuit is shown in Fig.2. The circuit consists of 5 kinds of Vi sources. By the signals Trgi's (i=1・・・5) generated from the trigger pulse generator in Fig.3, the power supply circuit can generate a pseudo triangle waveform as shown in Fig.3.

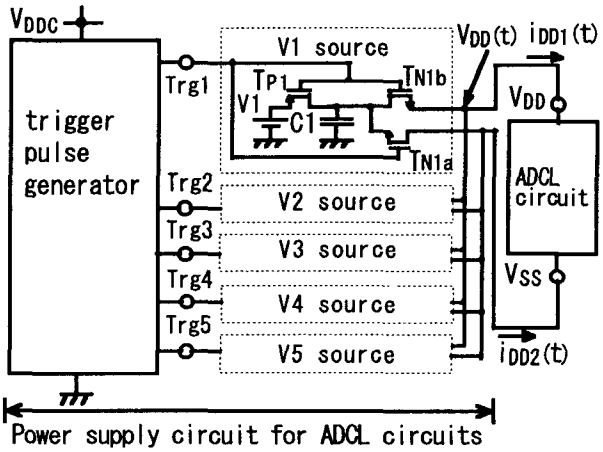


Fig.2 Power supply voltage source for ADCL circuits

Each Vi source is made of MOS transistors, a capacitor "Ci" and a constant voltage source Vi". The MOS transistors are used as switching elements. Charge in Ci is supplied from Vi and is transferred to an ADCL circuit. During the increment of the supply voltage VDD(t), the ADCL circuit will get energy from a Vi source and some energy will be stored in permissive capacitors between ADCL gates. During the decrement of VDD(t), the charge in the permissive capacitors will return to the Vi source in order to recycle the energy stored in the capacitors and realize low power consumption. Since some energy is dissipated in the ADCL circuit, the voltage across "Ci" will be reduced after withdrawing the charge in the circuit. Thus, the pMOS transistor Tpi in the Vi source will be conducted by a trigger signal Trgi and Ci will be charged again by Vi in the next supplement of voltage Vi.

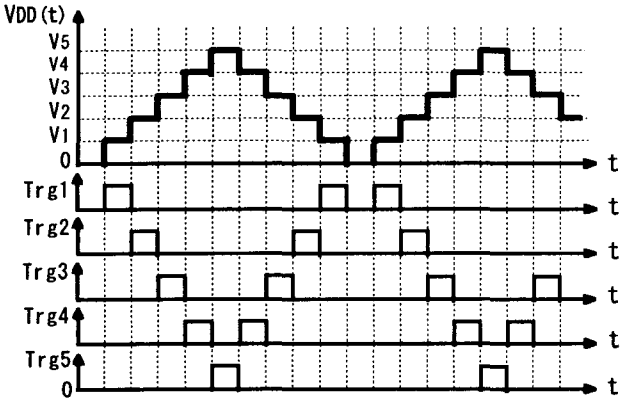
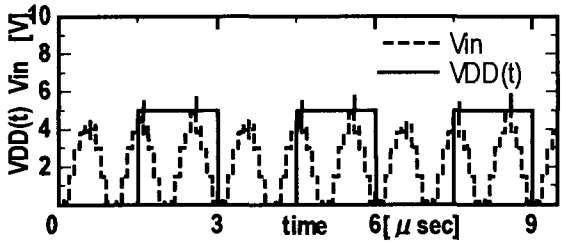
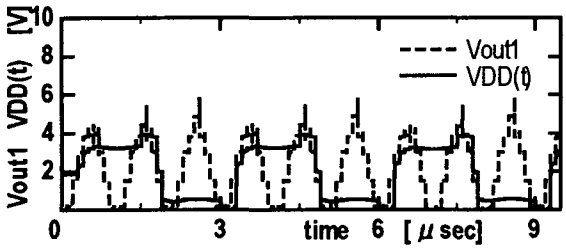


Fig.3 Trigger pulse signals and generated VDD(t).

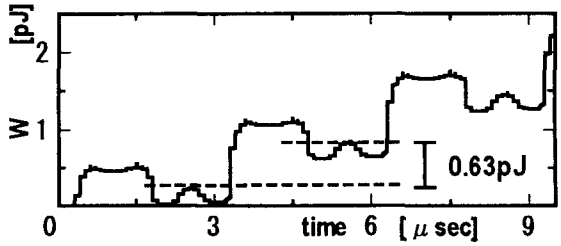
The simulation results obtained by using the power supply circuit in Fig.2 are shown in Fig.4. As shown in Fig.4, ADCL circuits can work as expected and lower power consumption in the circuits can be realized than in conventional static CMOS circuits.



(a) waveforms of input signal and VDD(t)



(b)output waveform



(c)power dissipation

Fig.4 Simulation results of Fig.2 for ADCLINV1

3. Improved Power Supply Circuit

We examined the reason why low power consumption in ADCL circuits can be obtained by some experiments using the power supply circuit in [4]. As the result, we found that it does not stem from adiabatic operation of ADCL circuits but from the removal of the switching current from VDD terminal and VSS one. It means that the number of trigger signals can be decreased. Thus, we improved the power supply circuit in Fig.2 to the one shown in Fig.5. In the improved power supply circuit, only 3 kinds of trigger signals are used.

Furthermore, pMOS transistors Tpi can be removed. As the result, each Vi sources can be simplified as shown in Fig.5. That is, each Vi source can be made of only Ci, Vi and nMOS transistor TNia and TNib.

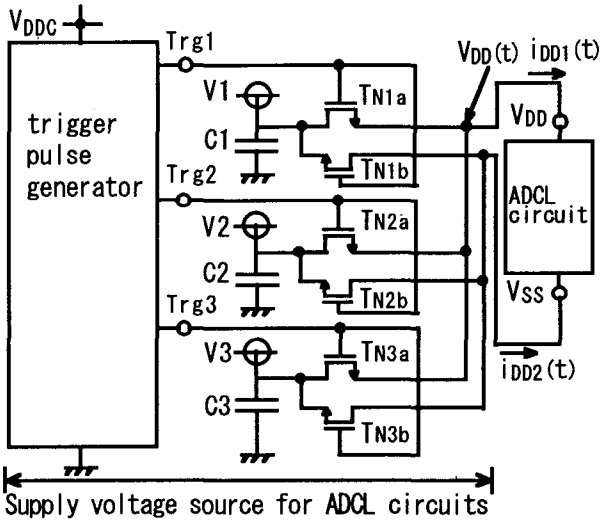


Fig.5 improved power supply circuit

3 kinds of independent voltage sources Vi (i=1,2,3) are required as shown in Fig.5. In battery-operated computer circuits, independent Vi sources occupy large area in the equipment, since batteries are used as independent voltage sources and generally are large size. Thus, we attempted to improve the circuit in Fig.5, so as to decrease the number of independent voltage sources. The improved source circuit is shown in Fig.6. As shown in Fig.6, Ci (I=1,2,3) and VDD are used, instead of V1,

V2, V3 in Fig.5.

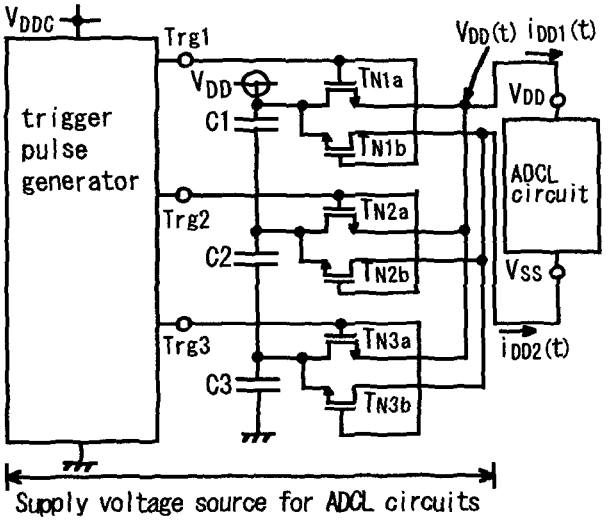


Fig.6 power supply circuit with small size

4. Experimental evaluation

In order to evaluate our improved power supply circuit in Fig.5, the source voltage for the circuits in Fig.1 and Fig.7 is supplied by the source in Fig.5. In our experiments, the following Vi's are used and W(t) is examined: V1=0.5V, V2=2.5V, V3=5V, where W(t) is defined by Eq.(1).

$$W(t)=\int_0^t VDD(t) \cdot IDD(t)\, dt \qquad (1)$$

The results are shown in Fig.8 and Fig.9. As shown in Fig.8 and Fig.9, by using our power source in Fig.5, they can work in adiabatic mode.

In order to compare the power consumption of improved circuits with the power supply circuit in Fig.2, the power consumption of ADCLINV1 and the one of ADCLINV2 are examined by using circuit simulation. The result is shown in Table 1.

As shown in Table 1, the power consumption of the circuit using our power supply source is a little larger than the one using ideal source. However, it is smaller than the one using the circuit in Fig.2. Also. it is extremely smaller than the one of conventional static CMOS circuits.

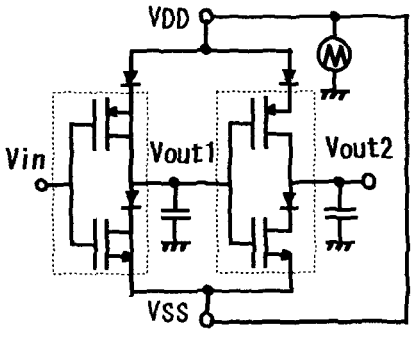
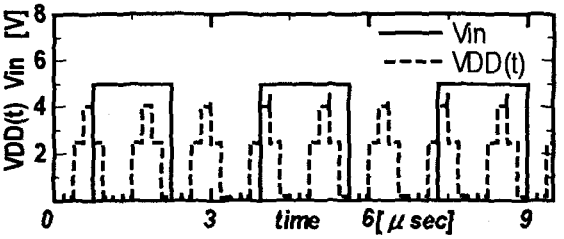
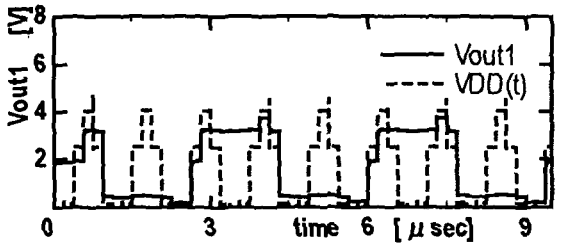


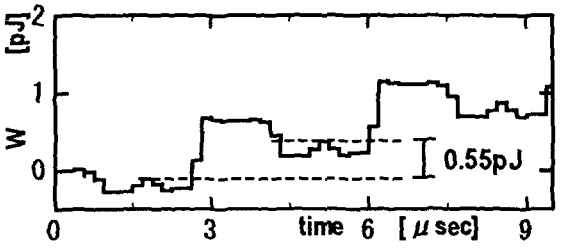
Fig.7 ADCL circuit(ADCLINV2)



(a)waveforms of input signal and VDD(t)

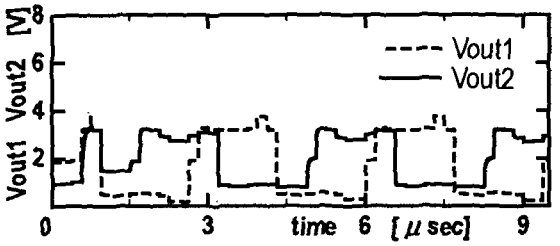


(b)output waveform



(c)power dissipation

Fig.8 Simulation results of Fig.4 for ADCLINV1



(a)output waveform

Fig.9 Simulation results of Fig.4 for ADCLINV2

Table 1 Power consumption W(t)[pJ]

		used power supply source			
type	stage	DC	Fig.1	Fig.2	Fig.5
Static	1	55.3			
	2	93.5			
ADCL	1		0.35	0.63	0.55
	2		0.71	1.45	1.21

5. Consideration

It is expected by using these power supply circuits in Fig.5 and Fig.6, ADCL circuit can work and the power consumption is smaller than the one of conventional static CMOS circuits. We examined it by some

experiments.

In order to compare the power consumption of Fig.2 with the ones of Fig.5, the power consumption of ADCL inverter gates is examined by circuit simulation. The results are shown in Table.1.

As shown in Table.1, the power consumption of ADCL inverter gates supplied by the circuits in Fig.5 is smaller than the one of conventional static CMOS circuits. Also, the power consumption by supplied the circuit in Fig.6 may be larger than the one of Fig.5. However, since the size of power supply circuit in Fig.6 can be smaller than the one of power supply circuit in Fig.5, the power supply circuit in Fig.6 is suitable for mobile computing equipment. Thus, the improved power supply circuit in Fig.6 is more suitable than the one in Fig.5.

6. Conclusion

In this paper, we attempted to improve the size of the power supply circuit for ADCL circuits and examined the power consumption of the ADCL circuits. Our power supply circuit is more simplified than previous one. As the result, it is shown that by using the improved power supply circuit, ADCL circuits can work with low power consumption than conventional static CMOS gates and previous one. It is expected that that by using our power supply circuit such circuits will be implemented and low power consumption will be realized.

References

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