A wide range analog synchronous mirror delay adopting the comparator with inherent systematic offset

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Abstract: A new analog synchronous mirror delay to be used in the wide-bandwidth clocking circuits is proposed to overcome the frequency dependency of the negative-delay values in the conventional analog synchronous mirror delay. The scheme adopts a new dummy-delay compensation technique by adopting the comparator with inherent systematic offset to achieve the enhanced negative-delay range especially prominent at high frequency applications.

1. Introduction

Recently, the demand for the high speed clocking circuit is rapidly increasing in the wide-bandwidth memory systems and communication systems. In order to reduce the skew between data and the system clock, classical phase-locked loop (PLL) and delay-locked loop (DLL) have been used [1]. These closed-loop circuits need sometimes several hundred cycles to recover the locking when they are exiting the shut-off mode.

To insure the fast clock recovery time the digital SMD [2, 3] is introduced. It realizes two-cycle locking by using an open-loop structure. However, it has the drawbacks of large chip area and power consumption in the wide-bandwidth applications.

An analog synchronous mirror delay (ASMD) is recently proposed to remedy the drawbacks [4]. It includes a static comparator which introduces the auxiliary delay during the logic evaluation. To make up for the auxiliary delay, the ASMD uses a modified-pumping scheme. However, the negative-delay time using this scheme reveals frequency dependency.

In this paper, an ASMD is proposed to eliminate the frequency dependency of the negative-delay values by using the new single-way-pumping scheme rather than the conventional modified-pumping scheme. In addition, the wider negative-delay range is obtained by incorporating the systematic offset voltage of the comparator in the new dummy delay compensation technique.

2. Concept of Single-way Pumping Scheme

The timing diagram to depict the basic concept of the single-way pumping for the negative-delay generation is shown in Fig.1. The primary input clock, CK is divided to a pair of complementary clock signals, MT and RT. The pumping control signal in the measure cycle, CLK_M is generated from MTD·MT, where MTD is the delayed signal of MT by the wanted negative-delay value, d. As soon as M finishes charging up at the falling edge of CLK_M, the analog voltage is held in the replica cycle until R charges up to the held voltage with the same pumping slope. When R coincides with M, the pull-up edge of CMPO generates RST which resets M, R and the pumping control signal in the replica cycle, CLK_R. The negative-delayed clock, OUT is observed at the pull-up edge of CMPO. As the up-going slope is observed both in M and in R, the same circuit can be used to facilitate the tracking advantage.

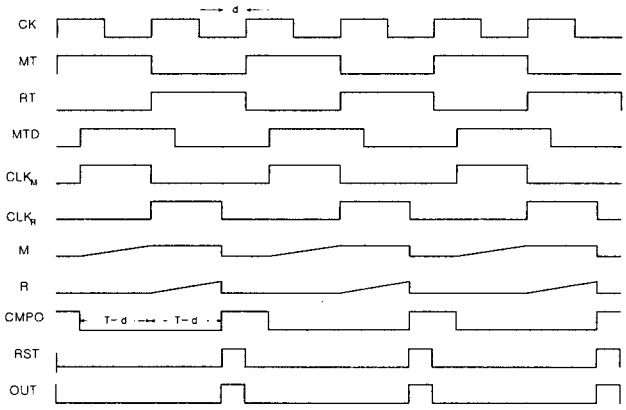

Fig. 1 Timing diagram of the single-way-pumping scheme

3. The Method of Dummy Delay Cancellation

3.1 Conceptual description

The conventional concept for generating the negative delay in SMD [2, 3] is shown in Fig. 2a, where T is the cycle time of the system clock, d is the target negative-delay value and d_{aux} is the auxiliary delay in the comparator. In the first cycle, $(d+d_{aux})$ is delayed in the delay model stage and $T-(d+d_{aux})$ is measured in the measure stage. In the next coming cycle, after the delay of $T-(d+d_{aux})$ in the replica stage and d_{aux} in the buffer stage, the negatively delayed clock advancing by the value of d can be obtained.

The proposed concept of the dummy-delay compensation technique shown in Fig. 2b compensates for d_{aux} in the replica stage but not in the delay model stage. We see that the measuring time, t_i, is restricted to the value of $(T- d_{aux})$ in the conventional scheme, whereas it extends to the maximum value of T in the proposed scheme. Thus the proposed dummy-delay compensation technique obviously offers the wider negative-delay range by a value of d_{aux}.

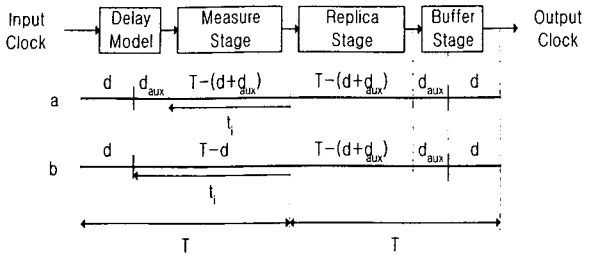

Fig. 2 Conceptual diagram for generating negative delay in two cycles
a Conventional scheme in [4]
b Proposed dummy-delay compensation technique

3.2 Frequency response

The up-down waveform of the conventional modified-pumping scheme is shown in Fig. 3a. The discharging slope in the replica period should be steeper than the charging slope in the measure period so that the time difference Δ will compensate for d_{aux}. We can find some serious drawbacks with this configuration. In Fig. 3a, as the clock frequency increases, compensation time Δ decreases to Δ_1, Δ_2, and Δ_3, respectively. Therefore, d_{aux} in the delay model stage has to be changed to get a constant negative-delay value according to the frequency variations. Moreover, conventional scheme needs both the charge-up pump and the charge-down pump. Usually it is very hard to match the charging and discharging slopes due to the process, supply voltage and temperature variations. To overcome this frequency dependency and up-down mismatch problem, we suggest the single-way pumping with systematic offset as shown in Fig. 3b. To facilitate the tracking characteristics in the measure and replica period, only the charging slope is involved.

After the time delay of d, charging-up proceeds during the measure period and the value is held during the replica period. Another charging waveform continues to go up until it reaches the voltage which is lower than the held voltage of the previous charging waveform by a V_{OFFSET}. At this point the two waveforms are reset. The offset But d_{aux} can be canceled with the systematic offset voltage in the proposed scheme as shown in Fig. 3b. The auxiliary delay can be described by

$$d_{aux} = \frac{V_{OFFSET}}{K} \qquad (1)$$

where K is the charging slope in the replica period. As V_{OFFSET} and K are frequency independent, d_{aux} is voltage usually degrades the performance of the comparator. not the function of frequency in (1). Thus, it is not necessary that d_{aux} should be cancelled in the delay model stage.

3.3 Implementation and results

The circuit-level implementation is shown in Fig. 4. During the charging-up time in the measure period, $\overline{CLK_M}$ is held at LOW to transfer the charge from the current source I_{PUMP_UP} to the capacitance C_M through M_{PM}.

In the replica period, $\overline{CLK_M}$ is kept HIGH causing V_{CM}, the voltage at C_M, to be constant. $\overline{CLK_R}$ is

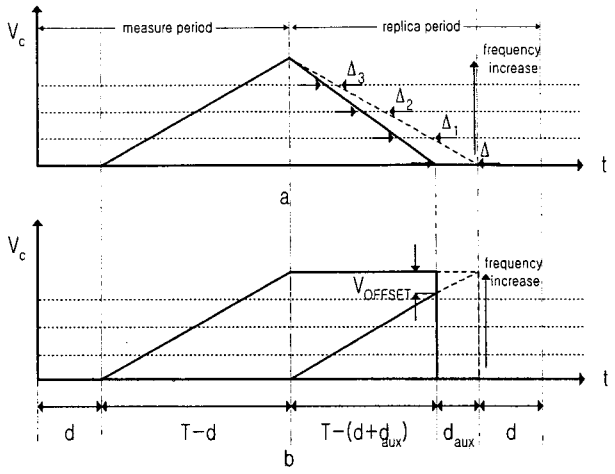

Fig. 3 Pumping scheme
a Conventional modified-pumping scheme in [4]
b Proposed single-way-pumping scheme with inherent systematic offset

held at LOW so that C_R charges up through M_{PR} during another charging-up time in the replica period. When the voltage at C_R coincides with the voltage of $(V_{CM}-V_{OFFSET})$, both the capacitance C_M and the capacitance C_R are reset by a pulse from the glitch generator which is triggered by the rising edge of the comparator output. This reset pulse is buffered to drive external loads. Table 1. shows the experimental d and the calculated d_{max} which is the maximum value of d according to the frequency sweep, when the target value of d is 3ns and the auxiliary delay d_{aux} is 2ns. As can be seen, for the conventional case when the dummy-delay compensation technique is applied, d is varied with the clock frequency changes. However, the constant value of d can be obtained with the proposed single-way-pumping scheme. In addition, from the calculated values of d_{max} according to the frequency variations, it is evident that the proposed dummy-delay compensation technique always provides the wider negative-delay range by a d_{aux} than the conventional scheme in Fig. 2a does.

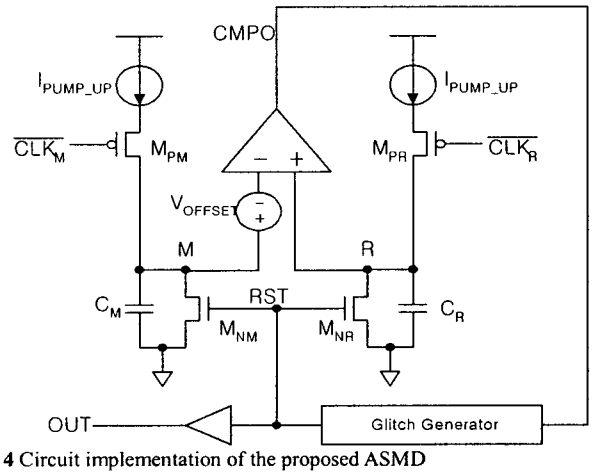

Fig. 4 Circuit implementation of the proposed ASMD

Table 1: Experimental and calculated results for 3ns negative delay when d_{aux} is 2ns

Frequency [MHz]	Experimental d [ns]		Calculated d_{max} [ns]	
	Conventio -nal pumping	Proposed single- way pumping	Conventional scheme shown in Fig. 1a	Proposed scheme shown in Fig. 1b
83	4.2	3.0	10	12
100	3.7	3.0	8	10
125	3.2	3.0	6	8
167	2.6	3.0	4	6
250	2.1	3.0	2	4

4. Conclusions

The new single-way-pumping scheme greatly increases the feasibility of ASMD with respect to the process variations. Using this scheme, the frequency dependency of the negative-delay time can be eliminated. In addition, the new dummy-delay compensation technique in which the auxiliary delay of the comparator is cancelled by incorporating the systematic offset achieves the wider negative-delay range. Both the experimental results and the analytical results show these advantages.

References

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