비선형 디지털 필터를 이용한 최적화된 영상 축소기

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Optimized Image Downscaler Using Non-linear Digital Filter

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Abstract

This paper proposes the optimized hardware architecture for a high performance image downscaler. The proposed downscaler uses non-linear digital filters for horizontal and vertical scalings. In order to achieve the optimization, the filters are implemented with multiplexer-adder type scheme and all the filter coefficients are selected on the order of two's power. The performance of the scaler is also verified by comparing with a pixel drop downscaler. The proposed scaler is designed by using the VHDL and implemented by using the IDEC-C632 0.65um cell library.

I. INTRODUCTION

Image scaler is widely used in multimedia video applications, such as TV, PC video, camcorder, and so on [1-2]. As with one-dimensional sampled data, digital images experience aliasing artifacts when the input image is downscaled (or undersampled). A simple way to the downscaling is a pixel drop, which is efficient for the scaling ratio of 1/(integer). For example, when the scaling ratio is 1/2 the input data in every two pixels (lines) will be dropped. It is shown in Fig. 1(a). When a non-integer scaling ratio like 1/2.4375 is required, the decimal fraction of the ratio is normally rounded towards the nearest integer for easy hardware implementation [3-5]. It is shown in Fig. 1(b). Thereby, the undersampled pixels contain aliasing artifacts that degrade the quality of the scaled image. To improve the downscaler using a pixel drop method, upsampling method is used. Fig. 1(c) shows upsampling method. The upsampling method requires that its pixel clock 32 times faster than one of input image when a scaling ratio is 1/2.4375 since 2.4375=1/32*78, so the very large hardware size is required and its implementation is sometimes infeasible due to the requirement of a very high speed signal processor. This paper proposes the optimized hardware architecture of the high quality downscaler by using non-linear digital filters and optimized filter architectures. Methods of the downscaler are explained in Section II and the experimental results are described in Section III. The conclusions are summarized in Section IV.

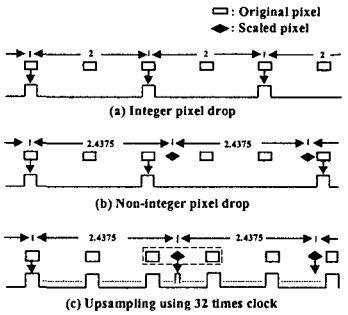


Fig. 1 Simple pixel drops and upsampling method

II. METHODS

The proposed scaler, instead of using the upsampling, obtains the valid scaled pixels (lines) between adjacent pixels (lines) by shifting the group delays of horizontal (vertical) digital filters. Fig. 2 shows the procedure of the proposed downscaler. The role of the filter is similar to an all-pass filter for gain, while the group delay of the digital filter varies according to the scaled points. This can be achieved by changing filter coefficients based on the scaled points

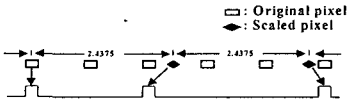


Fig. 2 Proposed methods of downscaling

As shown in Fig. 3, the proposed architecture consists of the following four blocks: line memory, vertical and horizontal scaler, and FIFO memory.

The line memory consists of two horizontal delay memories. The first memory delays the data for a 1 horizontal (H) time that is about 63.5us for NTSC video. The second memory accepts the 1H delayed data and delays the data for additional 1H time. Each memory should contain SRAM cells of 8

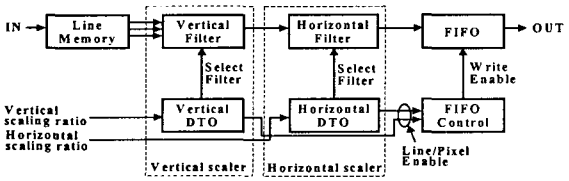


Fig. 3 Block diagram of the proposed downscaler

bits in width and 768 pixels in size to meet the ITU-R recommendation BT. 601 [6]. The operating pixel clock is 13.5MHz in frequency. The input, the 1H, and the 2H delayed data will be used in the following vertical scaler.

The vertical scaler consists of the vertical filter and the vertical discrete time oscillator (DTO) and performs the vertical scaling. The vertical filter consists of 3-tap 16-phase digital filter. The gain factor is 1/64. The vertical DTO generates the control signal for the vertical filter and uses the vertical scaling ratio and vertical active and horizontal active signals to input. The other scaling methods of the vertical scaler are the same with following horizontal scaler.

The horizontal scaler performs horizontal scaling and is composed of the horizontal filter and the horizontal DTO. The horizontal filter consists of a 5-tap 32-phase digital filter. The Matlab computes the 32 phases, each having the 5-tap coefficient, to provide the precision of a 1/32 pixel in horizontal scaling. The characteristics of the filter are shown in Fig. 4 and Fig. 5. Fig. 4 shows the frequency responses of the horizontal filter. The 3dB point is about 3.6MHz in frequency that is good enough since most of video signals are located below the frequency [6]. Fig. 5 shows the corresponding group delays, which have 32 phases. Notice that the delays are located within ±0.5 clock centered at 2 clocks.

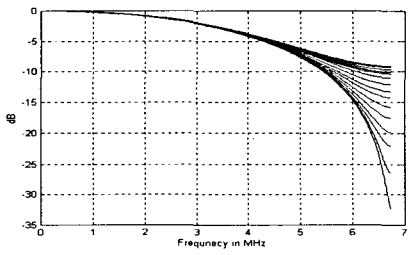


Fig. 4 Frequency responses of the horizontal filter

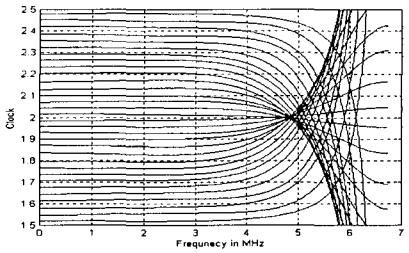


Fig. 5 Group delays of the horizontal filter

Thus, the 1/32 pixel precision in the horizontal scaling is achieved. The filter coefficients are listed in Table I. The gain normalization factor of the filter is 1/256 to maintain unity gain and for easy implementation.

Table I Horizontal filter coefficients

No.	Tap1	Tap2	Tap3	Tap4	Tap5
1	-2	126	133	-1	0
2	-4	122	139	0	-1
3	-4	116	143	2	-1
4	-6	111	149	4	-2
5	-6	105	153	6	-2
6	-6	99	157	8	-2
7	-6	93	161	10	-2
8	-6	88	164	12	-2
9	-6	82	168	14	-2
10	-6	76	172	16	-2
11	-6	69	176	19	-2
12	-6	64	176	25	-3
13	-6	59	178	29	-4
14	-6	54	180	32	-4
15	-5	48	182	35	-4
16	-4	44	180	40	-4
17	-4	40	180	44	-4
18	-4	35	182	48	-5
19	-4	32	180	54	-6
20	-4	29	178	59	-6
21	-3	25	176	64	-6
22	-2	19	176	69	-6
23	-2	16	172	76	-6
24	-2	14	168	82	-6
25	-2	12	164	88	-6
26	-2	10	161	93	-6
27	-2	8	157	99	-6
28	-2	6	153	105	-6
29	-2	4	149	111	-6
30	-1	2	143	116	-4
31	-1	0	139	122	-4
32	0	-1	133	126	-2

Fig. 6 shows the horizontal DTO block. The DTO is to generate a 1bit En_h and 5bit Sel_h signals for the horizontal filter. The 17bit Scale_h represents the horizontal scaling ratio, e.g., 1/2.4375. The En_hin denotes the horizontal valid area in the incoming image. The En_h that tells the current pixel is valid or not is generated by the ScaleD_a

and ScaleD through the XOR. The Bit Slice block chooses the upper 5 bits from the ScaleD except the polarity bit, which select one filter among the 32 horizontal filters.

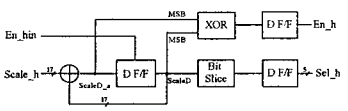
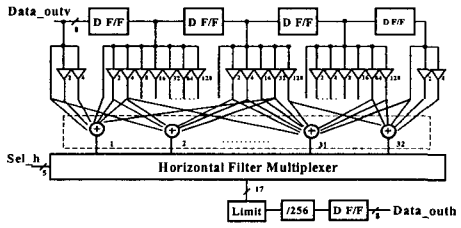


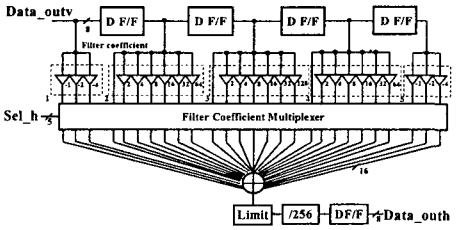
Fig. 6 Horizontal DTO

Fig. 7 shows the architecture of the horizontal filter. The Data_outv is the vertical scaler's output. When one designs digital filters, each filter output is first calculated and is, then, selected based on the scaling ratio through multiplexers (called Archit 1). It is shown in Fig. 7(a). Notice that the Archit 1 uses thirty-two full adders and one 32-to-1 multiplexer. In general, the cell area of a 1bit full adder is about two times bigger than that of a multiplexer. Thus, an optimized hardware needs to be developed to reduce the number of used full adders. An approach is that the filter coefficients are multiplexed based on the scaling ratios and the outputs are, then, summed to produce the scaled data (called Archit 2). It is shown in Fig. 7(b). Notice that the archit 2 uses only one full adder and one (5 coefficient sets)-to-1 multiplexer. Thus, one may expect that the archit 2 will require a much smaller hardware.

The FIFO stores only valid-downscaled data in the right side of the buffer. The FIFO also provides more flexibility for system builders since it can get rid of clock ambiguity generated by different systems. In the proposed downscaler, a 256*16 bits



(a) Adder-multiplexer type (Archit 1)



(b) Multiplexer-adder type (Archit 2)

Fig. 7 Architectures of the horizontal filter

synchronous FIFO is used.

III. RESULTS

For a performance evaluation of proposed downscaler, a diagonal pattern image is used. The scaled image by the proposed method is compared with the image using the pixel drop method. The frequencies of the used input images are 1MHz (3.34kHz), 2MHz (6.67kHz), 3MHz (10kHz), 4MHz (13.34kHz), and 5MHz (16.67kHz) to the horizontal (vertical) direction. 96 scaling ratios scale the input image. The evaluation is performed by comparing the signal-to-noise ratio (SNR) of the proposed downscaling image with that of the pixel drop image after the possible scaling ratios is applied for the one of the input images. Fig. 8 shows the sample images and the power spectrum. The frequency is 5MHz (16.17kHz) to the horizontal (vertical) direction.

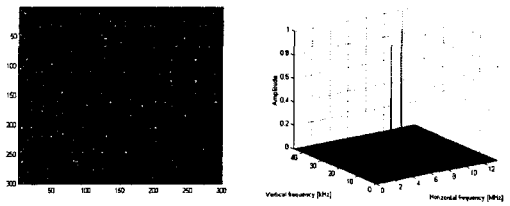


Fig. 8 Input image and the power spectrum

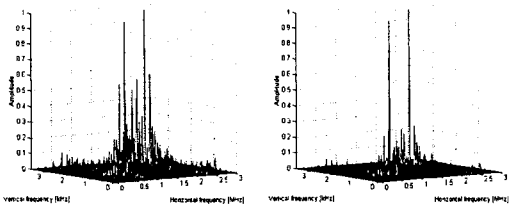
Table II shows the SNRs of the pixel drop and the proposed downscaling. The data shows that the proposed downscaler is better than pixel drop downscaler.

Table II SNR comparisons

Frequency of Input Image (horizontal/vertical)	Pixel drop [dB]	Proposed downscaler [dB]
1MHz/3.34kHz	60.95	62.26
2MHz/6.67kHz	55.52	57.03
3MHz/10kHz	51.53	53.41
4MHz/13.34kHz	47.79	50.00
5MHz/16.67kHz	44.89	47.97

Fig. 9 show the power spectrum of scaled image whose input image has the frequency of 5MHz (16.67kHz) and scaling ratio is 1/2.0625. Fig. 9(a) shows the power spectrum of pixel drop image that has much noise. Fig. 9(b) shows the power spectrum of output image obtained by using proposed downscaling method. In Fig. 9 the noise reduction is obvious.

The scaler is modeled by using the VHDL and the models are verified by using the Synopsys simulator. After the verifications are done, the models are synthesized into gates by using the Synopsys with the IDEC-C632 0.65um cell library.



(a) Pixel drop method (b) Proposed downscaled method

Fig. 9 Power spectrum

Each block of the scaler is synthesized in gates and the results are, then, listed in Table III. The first column lists the top modules of the scaler and the second column lists the submodules in the design. The memories (SRAM1, SRAM2, and FIFO) are not compared since one uses macro cells generated by the memory compiler in real IC implementation. The third column represents the cell area of each submodule by using the Archit 1 and the fourth column represents the cell area by using the Archit 2. As one can see, the Archit 2 reduces the cell area[1] of the vertical filter from 23,901.6 to 9,912.0 that is 58.53% reduction in the hardware complexity. It is caused by the reduction of the number of used full adders from 16 to 1. The total cell area is also reduced from 176,090.8 to 51,722.2 that are 70.63% reduction. Therefore, Table III reveals that the Archit 2 represents the optimized hardware architecture for the downscaler.

Table III Comparison of hardware complexity

		Submodule	Archit 1	Archit 2
Top module	Time alignment	-	2,640.0	2,640.0
	MACRO	SRAM1	-	-
		SRAM2	-	-
		FIFO	-	-
	Vertical scaler	SRAM control	2,144.2	2,144.2
		Delay	2,880.0	2,880.0
		Vertical DTO	3,456.0	3,456.0
		Vertical filter	23,901.6	9,912.0
	Horizontal scaler	FIFO control	499.2	499.2
		Horizontal DTO	3,854.4	3,854.4
		Horizontal filter	136,715.4	26,336.4
Total cell area (except macro cell area)			176,090.8	51,722.2

Fig. 10 shows the layout of the proposed downscaler. The synthesized scaler is placed and routed by the Mentor IC Station. The chip master is provided by the IDEC and fixed in size by 4500 *um* ×4500 *um*. The active layout area of the proposed scaler is 2120 *um*×3055 *um*.

1) The cell area of 7.2 in the IDEC-C632 0.65um cell library is equivalent to one gate in general ASIC libraries.

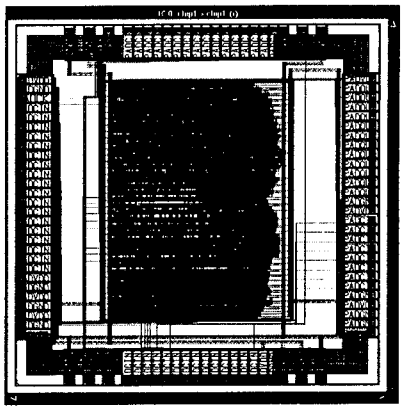


Fig. 10 Layout of the proposed downscaler

IV. CONCLUSIONS

The proposed downscaler extended the precisions of the scaler to 1/16H and 1/32 clock in vertical and horizontal directions. The scaler also reduced the hardware complexity by using the multiplexer-adder type architecture. The proposed scaler was synthesized into gates by using the IDEC-C632 0.65um cell library, resulting in the cell area of 51,722.2 that was equivalent to 7,184 gate count in general ASIC libraries. The active layout area was 2120 *um*×3055 *um*

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