Development of Giant Magnetoresistive Random Access Memory (GMRAM) For Space and Commercial Applications

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Korean Magnetic Society 10th Anniversary Symposium
Sept. 29, 2000

Outline

- Honeywell's nonvolatile magnetic memories
- GMRAM operation principals
- GMRAM manufacturing challenges
- Embedded GMRAM development
- Summary

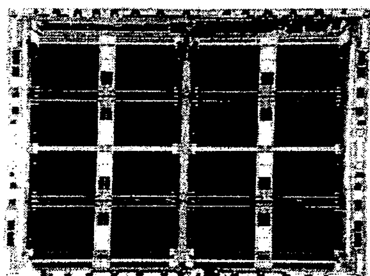
Honeywell's Three Generations of Nonvolatile Magnetic Memory

Plated Wire Memory (1962 -)

4K (x 32) Plated Wire Memory

- Inductive Memory Cells
- 11 lbs.
- 13.5 x 5.8 x 2.8 in^3
- Power
  - ° 14 W Standby
  - ° 25 W Write
  - ° 17 W Read

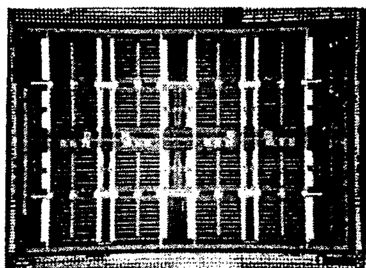
Magnetoresistive Random Access Memory (MRAM) (1984 -)



16K AMR MRAM

- Anisotropic MR Cells
- Over 100 fold improvement
  - weight
  - size
  - power consumption

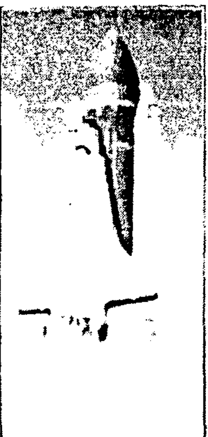
Magnetoresistive Integrated Circuit (MagIC™) (1998 -)

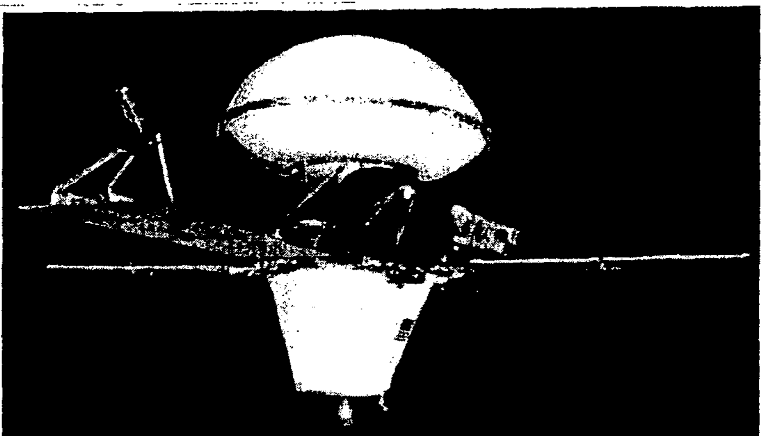


1M GMRAM

- GMR Memory Cells
- Over 100 fold improvement
  - density
  - speed

Memory of Necessity for Space and Strategic Programs





- Nonvolatile and Reliable Data Storage
- Immune to Radiation Effects
- Unlimited Write / Read Cycles
- Non Destructive Read Out
- Critical Program Storage
- Dynamic Reprogrammability
- Rapid System Reconfigurability

1Mbit GMRAM Development Chip

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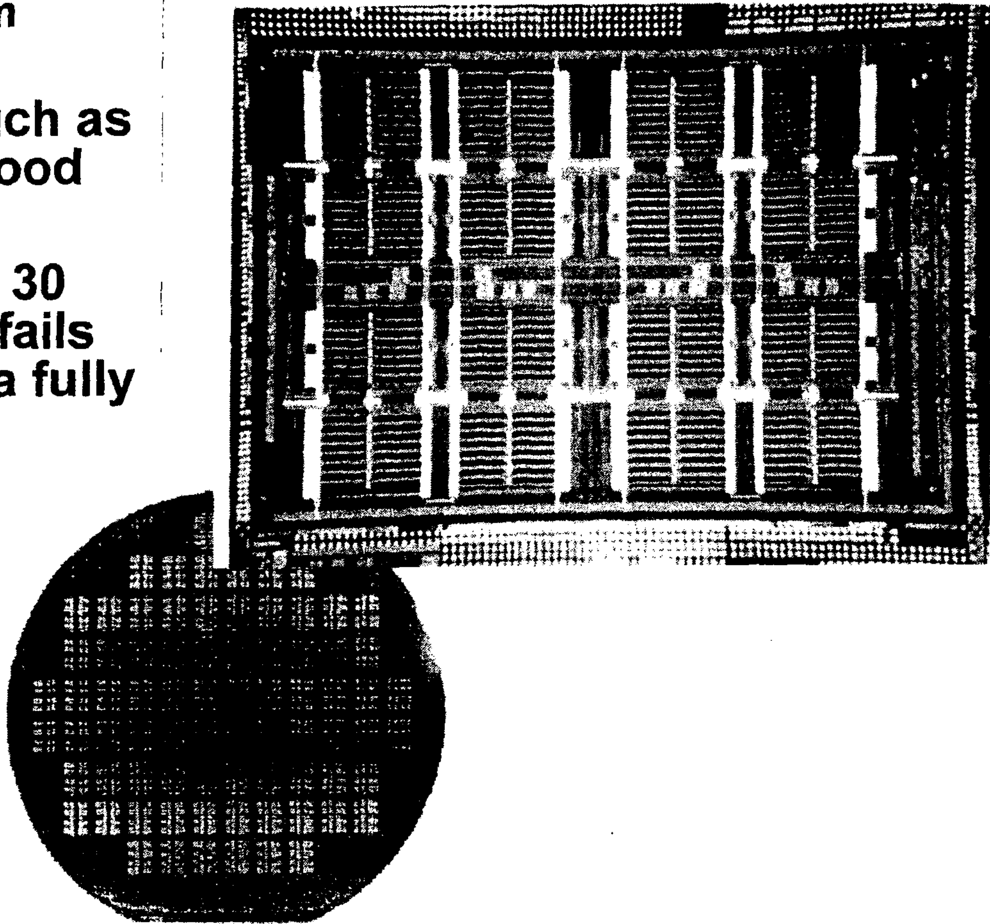
- Approximately 100 million GMR bits per wafer
  - –O ver 5 billion GMR bits per wafer anticipated using sub 0.2 μm technology
- Competitive technologies such as flash routinely yield > 80% good die per wafer
- With redundancy, typically < 30 out of 1,048,576 random bit fails can be tolerated to produce a fully functional chip
- Manufacturing challenges
  - Maturity
  - Simplicity
  - Compatibility
  - Robustness
  - Yield



Mature and Simple Memory Cell
Pseudo Spin Valve

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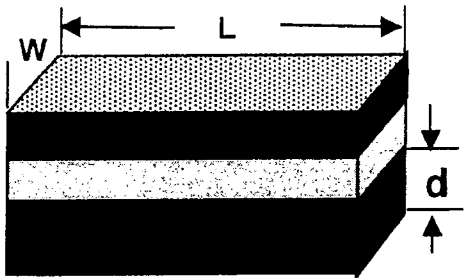
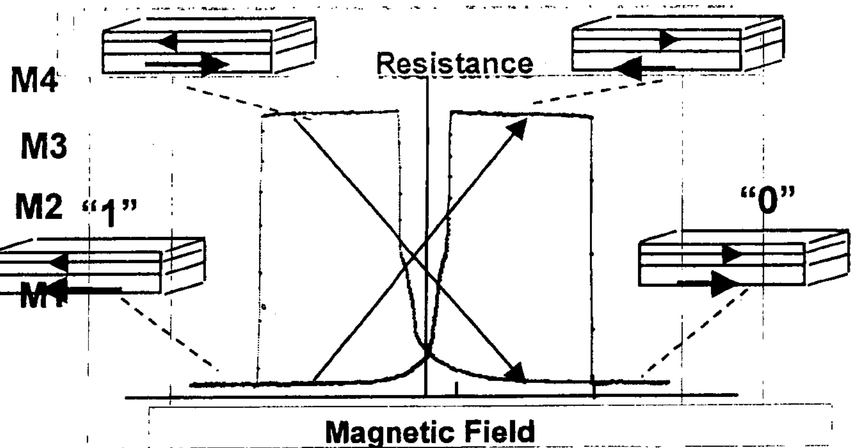
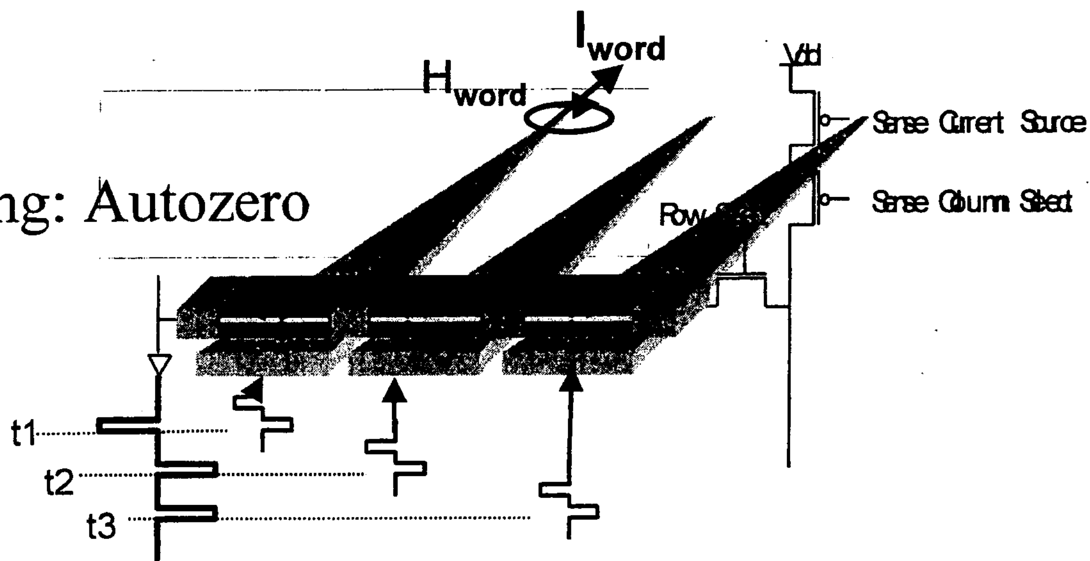
Sensing layer
NiFeCo 3 nm
Cu ~ 3 nm
Storage layer
NiFeCo 6 nm



$$H_{switch} = c\ d/ W$$



Robust Sensing: Autozero



1Mbit GMRAM Process Overview

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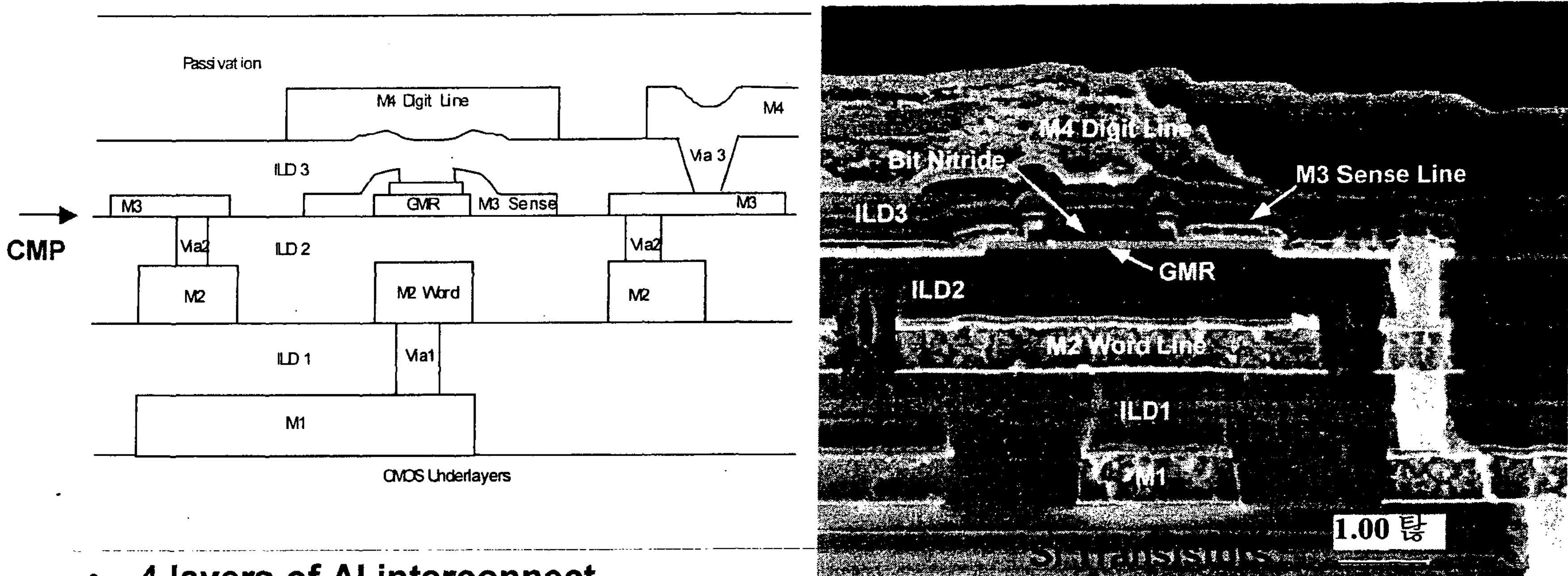

- 4 layers of Al interconnect.
- Standard CMOS processing through via2
- CMP to prepare smooth starting surface for GMR stack deposition
- GMR specific steps are inserted between via2 and metal3.
  - 4 deposition steps (seed layer, GMR stack, mask layer, bit dielectric layer)
  - 2 photo steps (GMR bit cut, bit contact cut)
  - 3 etches (mask layer, GMR stack, bit contact)
- GMR-on-top compatible to Si process

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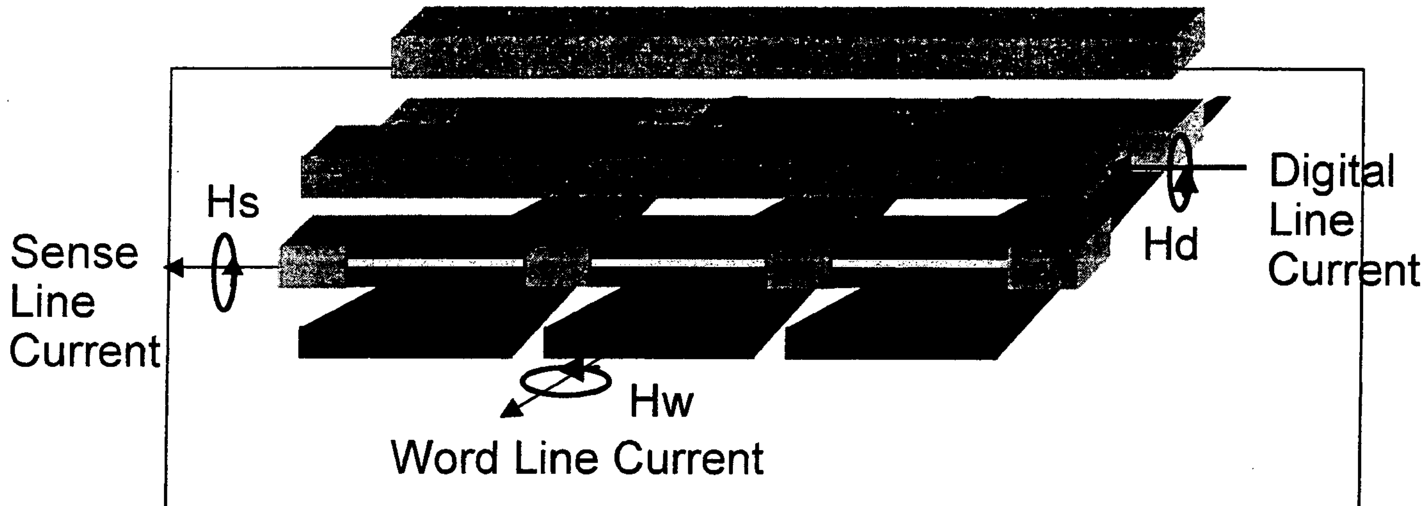
Robustness against spatial and temporal variations



$$H = \begin{cases} 0, & \text{data retention} > 10 \text{ years;} \\ H_S + H_D, & \text{no switch}^* > 10^{15} \text{ cycles;} \\ H_W, & \text{no switch}^* > 10^{15} \text{ cycles;} \\ H_W + H_S + H_D, & \text{switch}^* > 10^{15} \text{ cycles;} \end{cases}$$

* < 30 bits out of 1,048,576

Spatial (bit-to-bit) Variations

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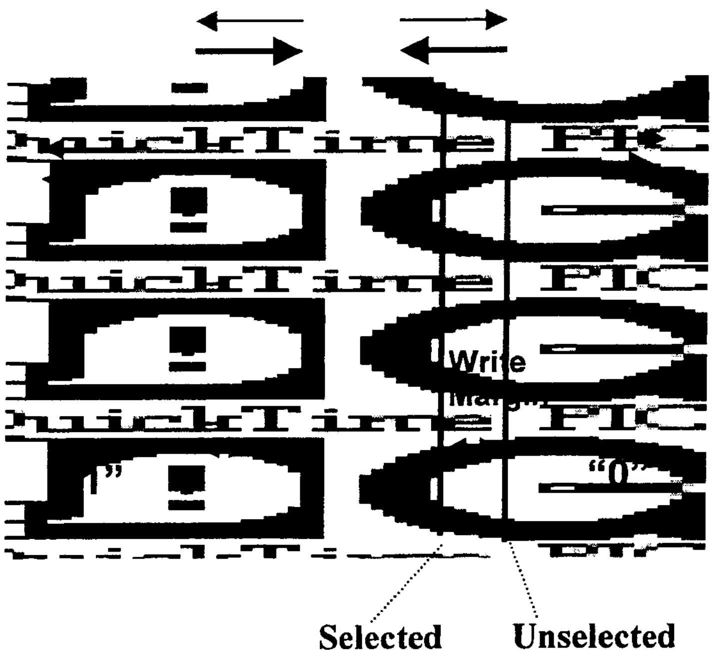
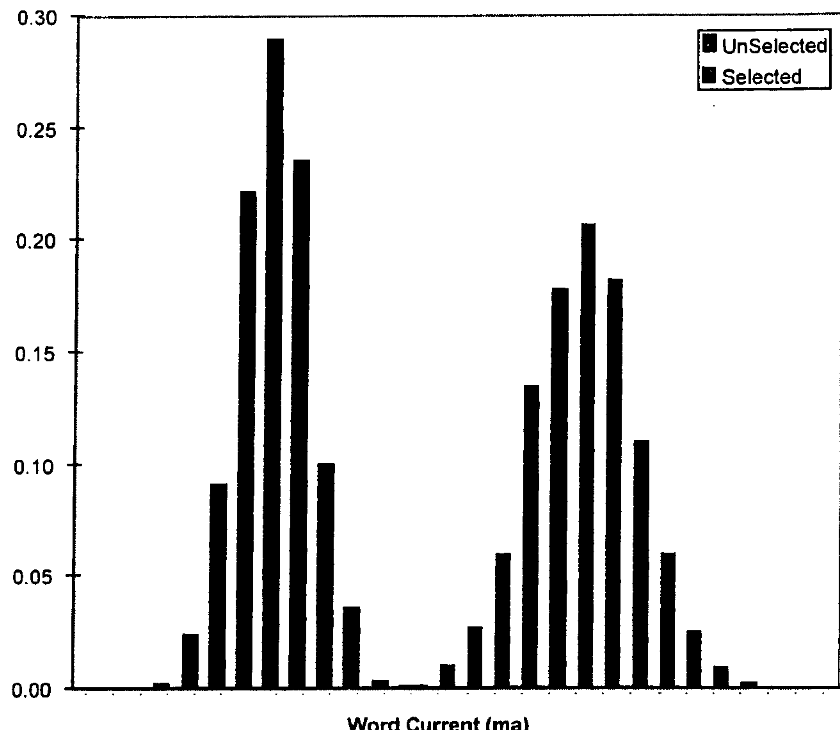
WRITE OPERATION





Causes for Nonuniformity

- GMR film (deposition)
- Bit line width (lithography)
- Bit patterning (ion milling)

Patterning of Submicron Dimension Memory Elements

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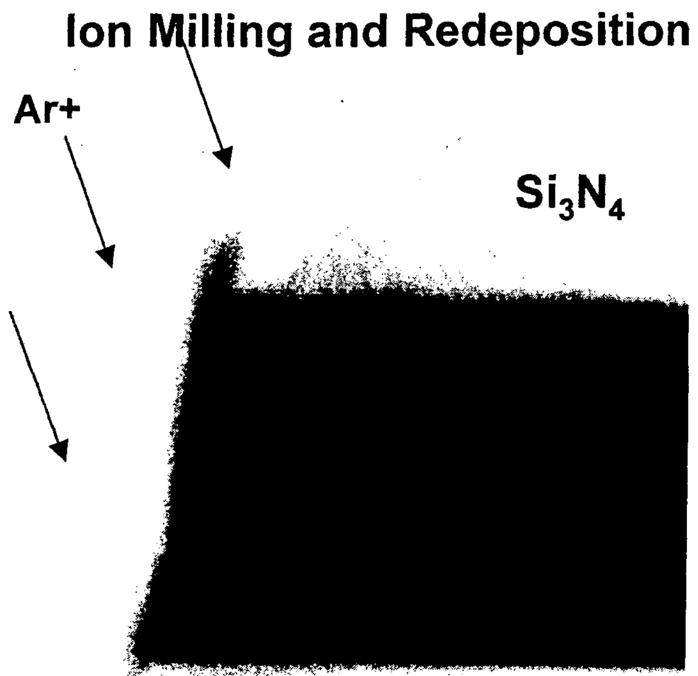
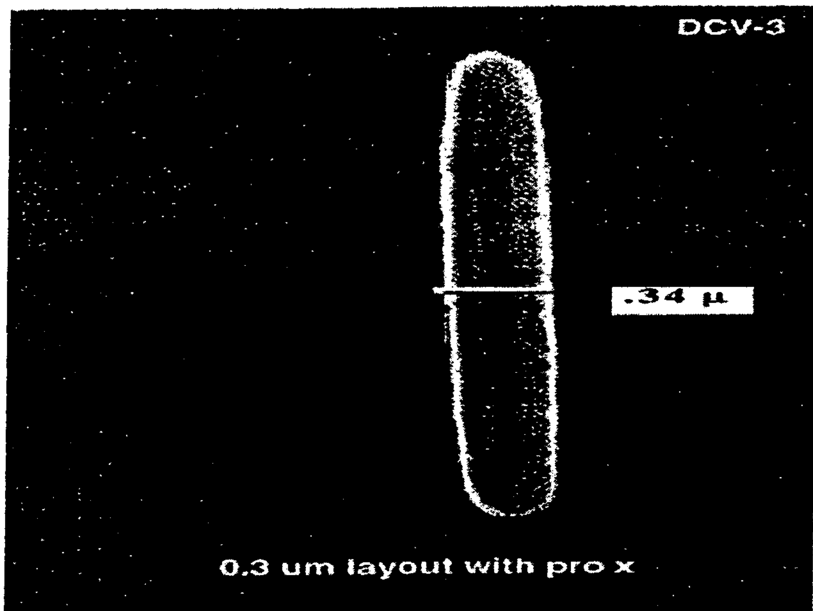
Ion Milling and Redeposition





Implications for a Memory Write Operation

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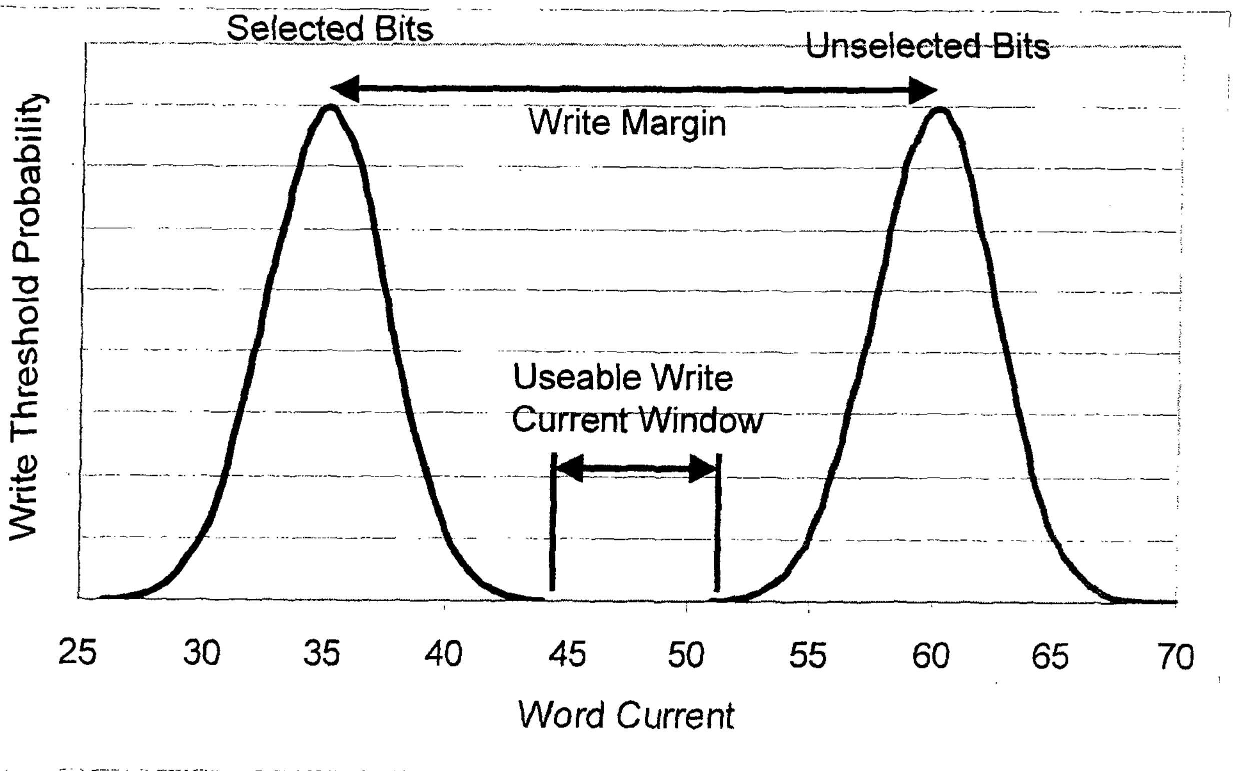
- Sufficient current must be applied to write every bit in the memory when it is selected, but not write any of the bits in the array when they are not selected.



It is clear that a useable write current window can be achieved in two ways:

1. **Increase Write Margin**
2. **Decrease the Selected and Unselected Threshold Standard Deviation**

Write Margin vs Standard Deviation

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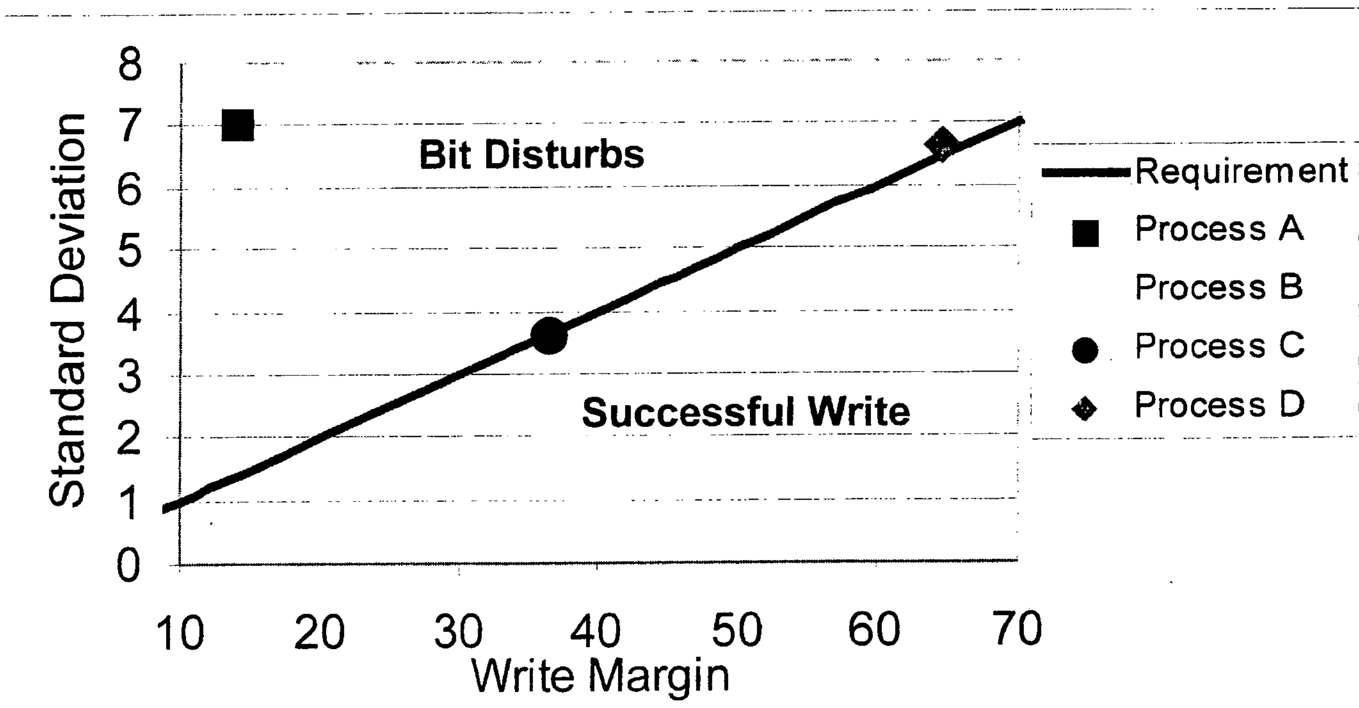
- True memory operation requires 100% write assurance with no bit disturbs.
- As previously discussed, this implies a required write margin and threshold distribution (as measured by the standard deviation).
- This tradeoff is critically dependent on material properties and process integration.
- Some examples of this dependence is shown below.



Edge Soliton and "S" State Magnetic Reversal

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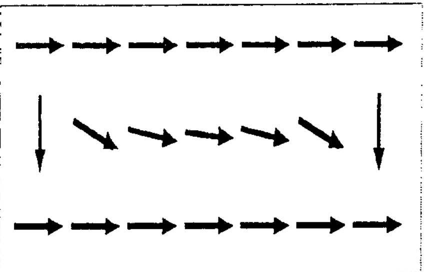
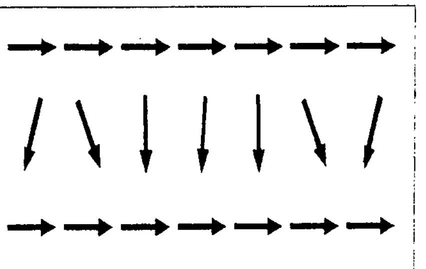
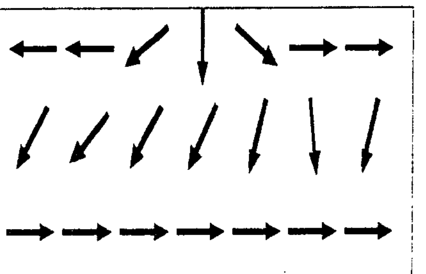
S STATE

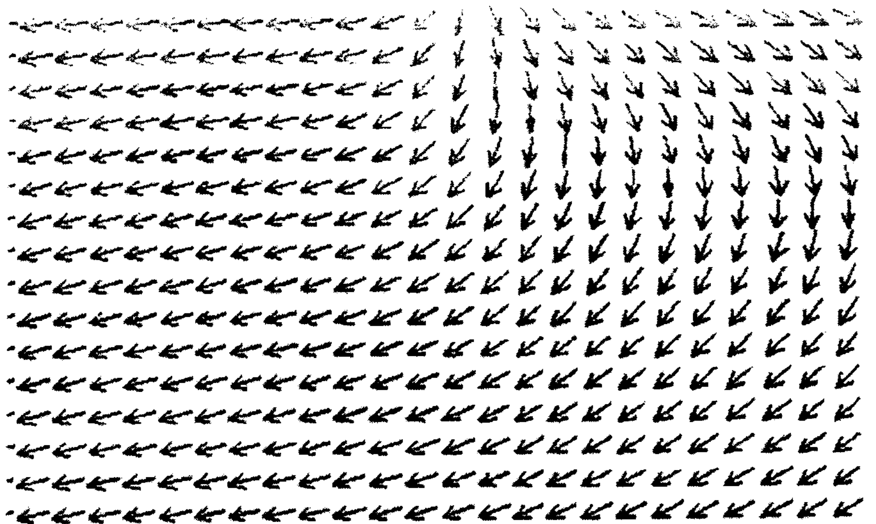


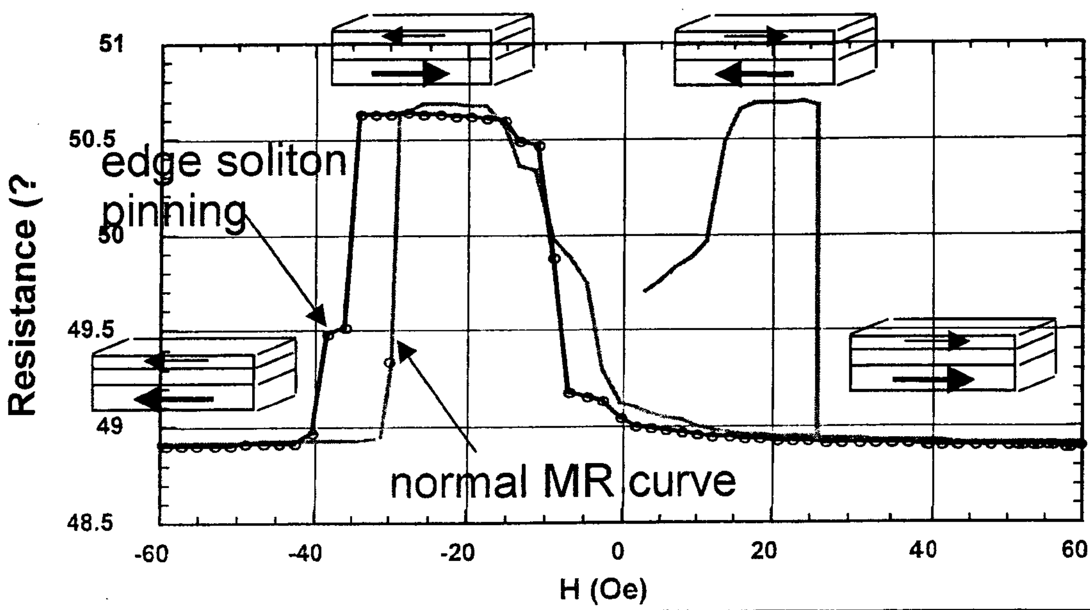
S STATE WITH CENTER I



S STATE WITH EDGE SOLIT(







360° Domain Wall and "C" State Magnetic Reversal

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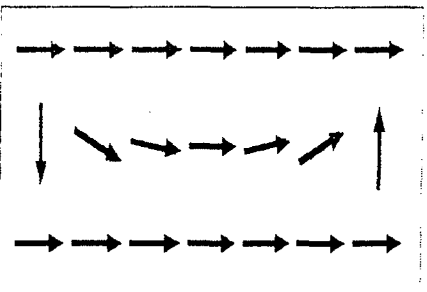
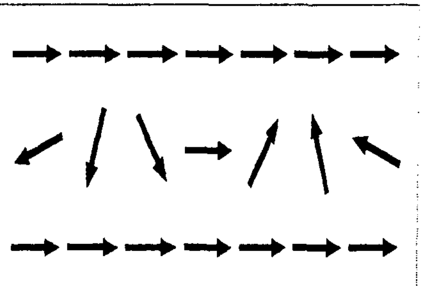
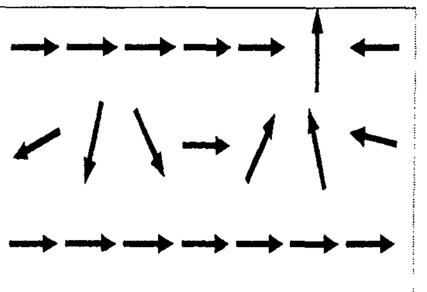
C STATE

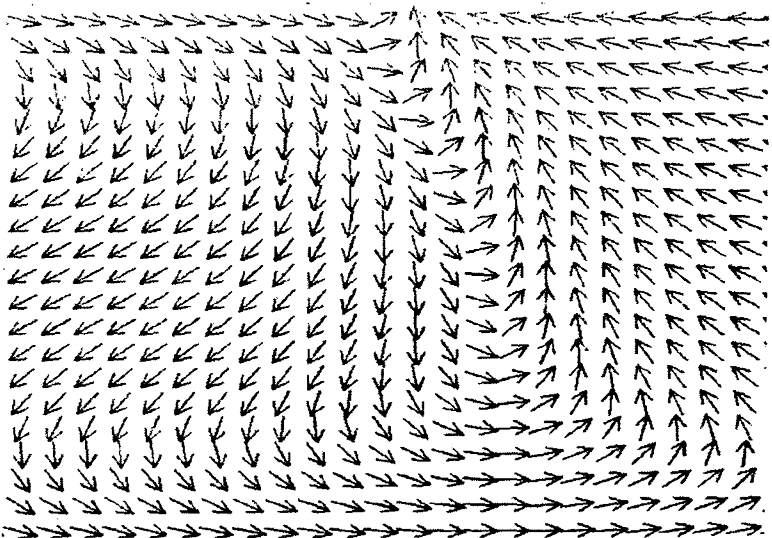


C STATE WITH CENTER

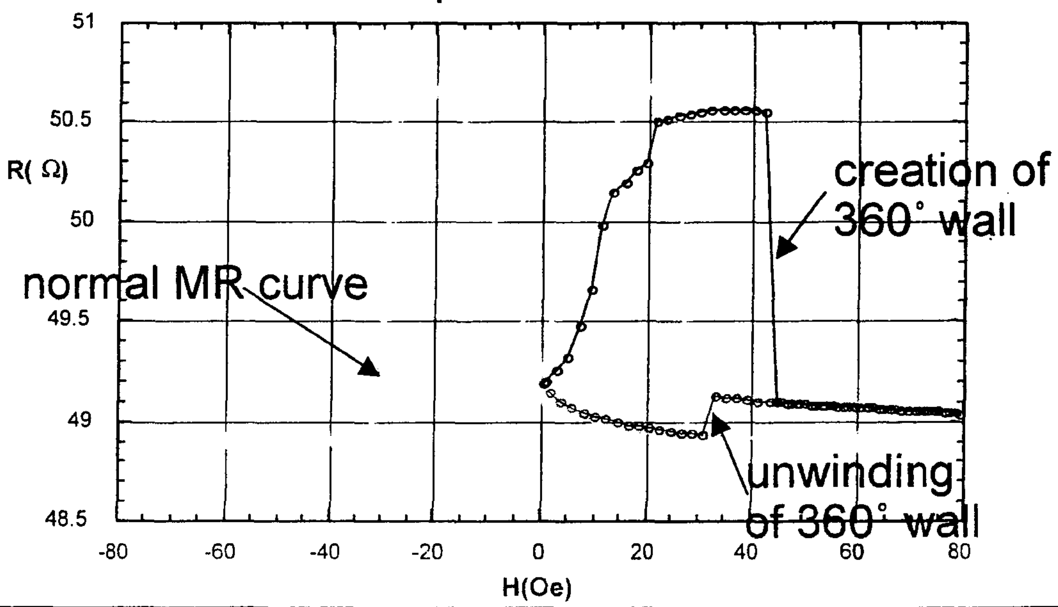


C STATE WITH EDGE SOLI





C state produces 360?wall



Temporal (cycle-to-cycle) Variations

Bit Repeatability

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- The existence of a write probability distribution requires higher write currents to assure no errors for the life of the device.
- The plots below show how the write threshold increases to assure 0 errors for an increasing number of write/read cycles.

Word Current

Digit	34	37	40	43	49	53	55	60
0	65536	65536	65536	65536	65536	65536	65536	65536
10	65536	65536	65536	65536	13295	4	1	0
20	65145	41713	99	0	0	0	0	0
30	24199	470	0	0	0	0	0	0
40	5207	214	0	0	0	0	0	0
50	3839	208	0	0	0	0	0	0
55	7409	261	0	0	0	0	0	0

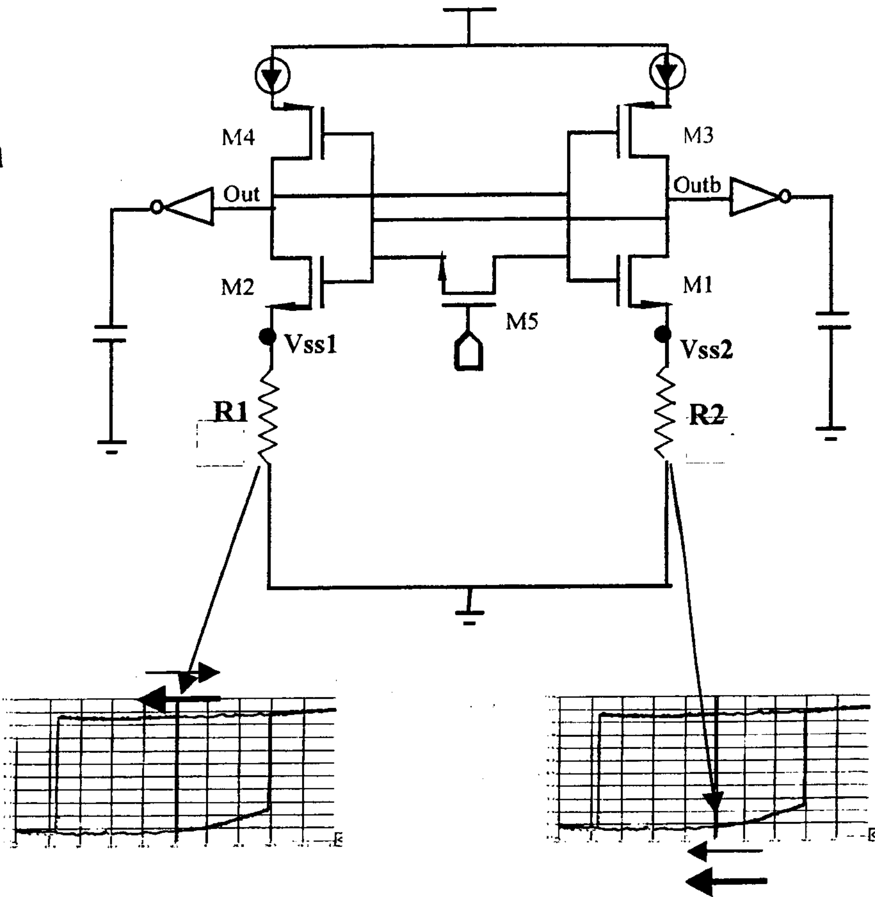
Word Current

Digit	34	37	40	43	49	53	55	60
0	6.55E+08	6.55E+08	6.55E+08	6.55E+08	6.55E+08	6.55E+08	6.55E+08	
10	6.55E+08	6.55E+08	6.55E+08	6.55E+08	2664754	65731	23178	1163
20	5.92E+08	17553189	267567	520	0	0	0	0
30	334398	4016	201	10	1	0	0	0
40	733734	2340	147	2	0	0	0	0
50	1373839	9096	670	0	0	0	1	0
55	7022652	13585	730	46	17	16	6	1

- # of write/read fails vs word and digit current for a single bit in the 1M array.The area in green shows the write currents to achieve 100% write success.
- 65K write/read cycles
- 655M write/read cycles

GMR Latch Memory Architecture

- Operation Principle
  - Two complementary GMR memory elements integrated to a 5T latch cell
    - » M5 for latch state reset
    - » Two matched p-MOS (M3 & M4) providing equal sense currents
    - » Two complementary GMR resistors (e.g., R1 > R2) leads Vss imbalance and latches the data
- Nonvolatile SRAM
  - Shift registers
  - Cache memory



GMR Latch Simulation and Test Results

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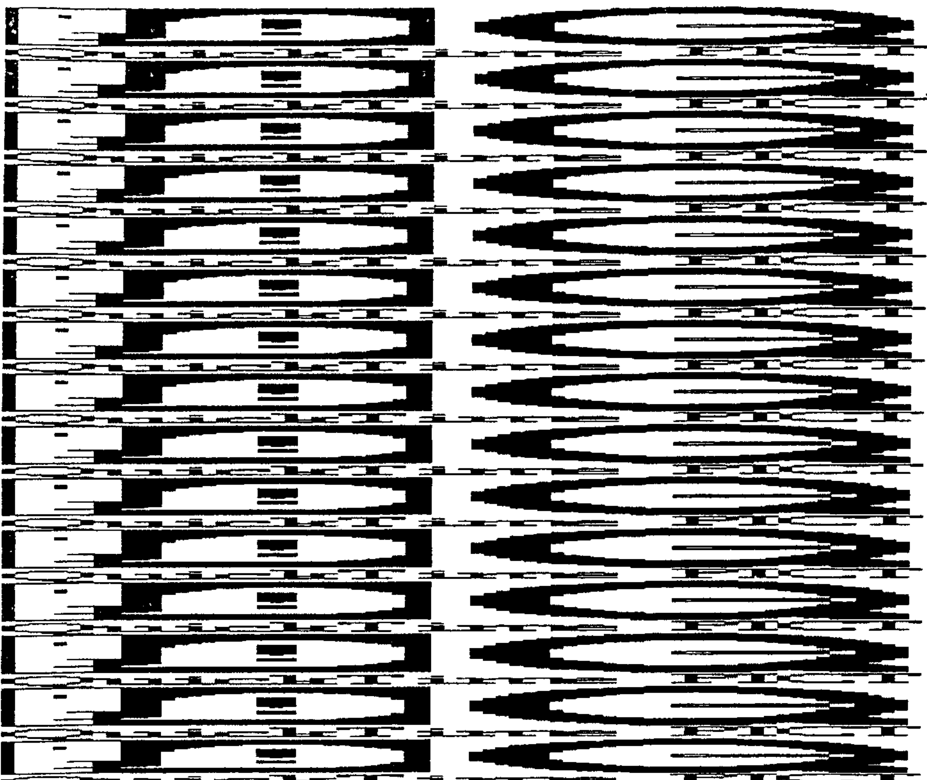
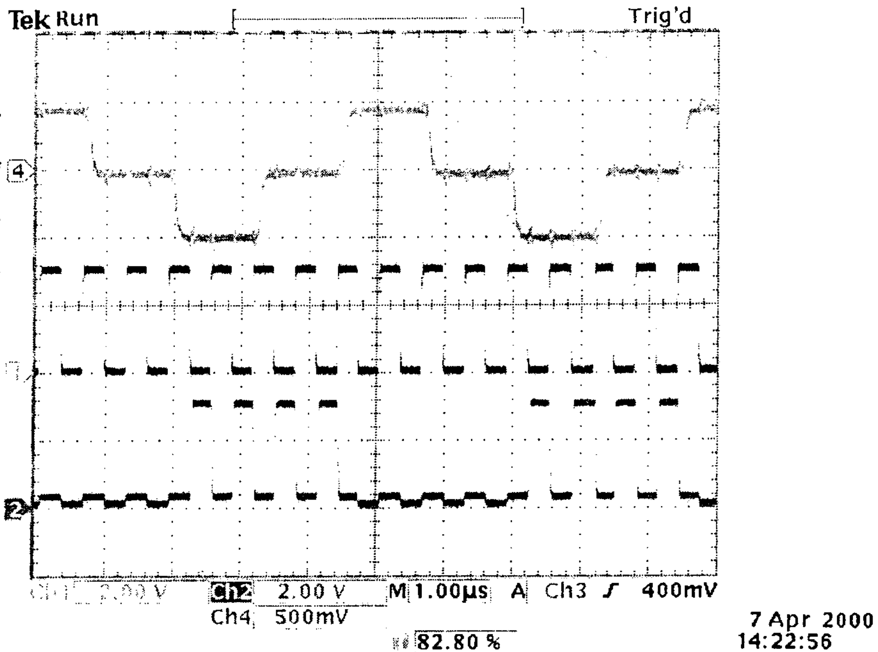


• GMR latch read consists track phase and latch phase

- track time < 1.5 ns
- latch time < 5 ns



• **Measured read access time (track + latch) < 40 ns with sense current 50µA**

Demonstration of Two GMR Memory Architectures

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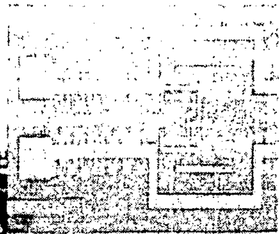
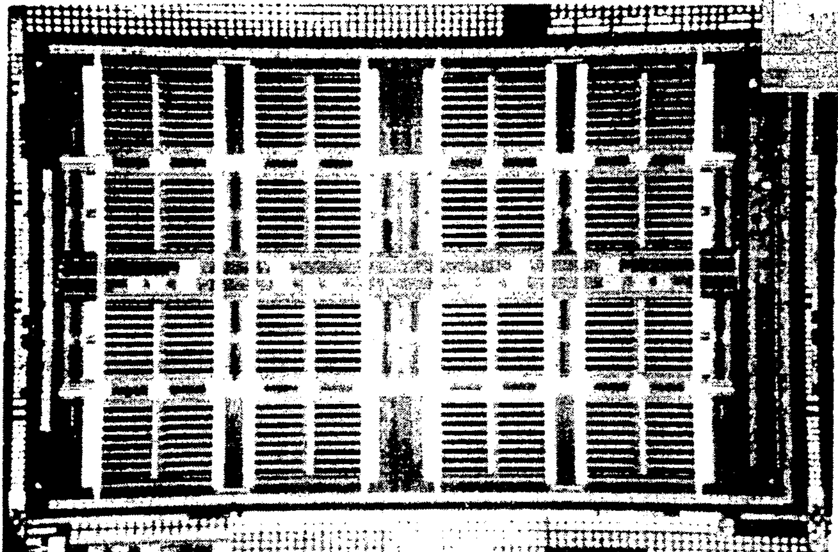
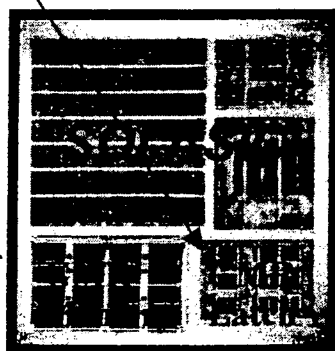


- Functional GMR latch cells
- 2R/5T GMR architecture
  - Projected performance
    - » < 20 ns read access
    - » > 200 λ^2 density

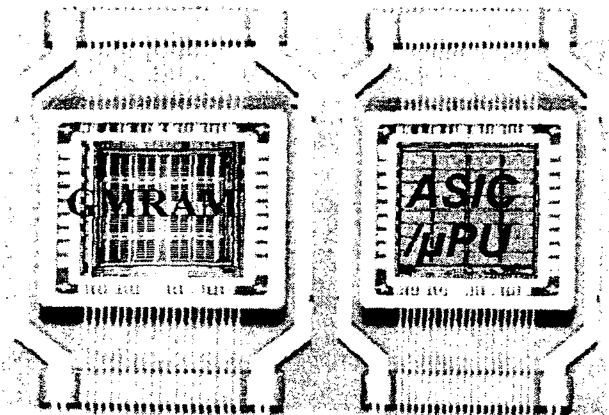


- Functional 1Mbit GMRAM
- 1R/0T GMR architecture
  - Projected performance
    - » 50 - 100 ns read access time
    - » 12 - 21 λ^2 density



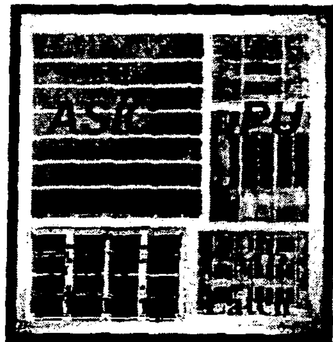
Stand-alone vs. Embedded Nonvolatile Memory Honeywell

Stand Alone GMRAM



- Large amount nonvolatile memory capacity
  - Date storage
  - Critical programs
- Disadvantages in system cost, speed, & weight
  - External interface and I/O
  - Bonding pads
  - Package inductance & wiring
  - External board wiring

Embedded GMRAM



- Smaller amount nonvolatile memory capacity
  - Instructions
  - Codes
  - Registers
- Ideal applications
  - Dynamic Reprogrammability
  - Rapid System Reconfigurability
  - Code modification in flight

Honeywell GMR Technology

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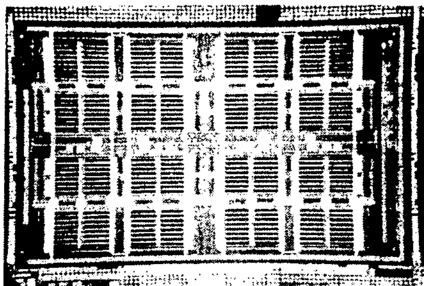
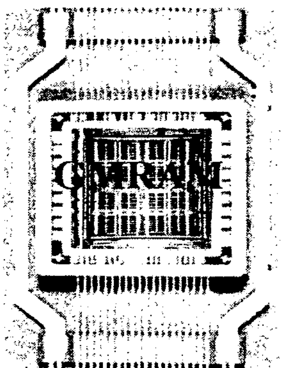
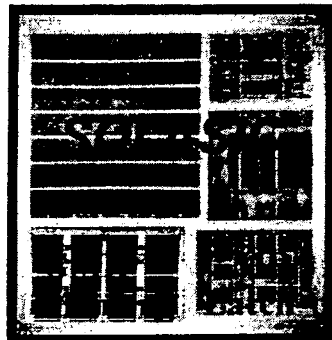
1 Mbit GMRAM Demo Chip



Stand Alone Rad Hard GMRAM
- 1Mbit GMR memory



Embedded Rad Hard GMRAM
- ASIC embedded GMR memory



- GMRAM technology has been demonstrated at Honeywell
- Product developments currently underway
  - 1Mbit Radiation Hard GMRAM (using rad hard SOI CMOS underlayers)
  - Rad Hard Embedded GMR with SOI ASIC

Summary

- Developed two GMR memory architectures
  - 1R/0T for high density applications
  - 2R/5T for high speed applications
- Embedded GMR technology shall offer rad hard community
  - Dynamic Reprogrammability
  - Rapid System Reconfigurability
  - Code modification in flight
- Embedded GMR technology is promising for commercial applications